MEPTEC Semiconductor Packaging Technology Symposium

Advanced Packaging's Interconnect Technology Process Shift and Direction

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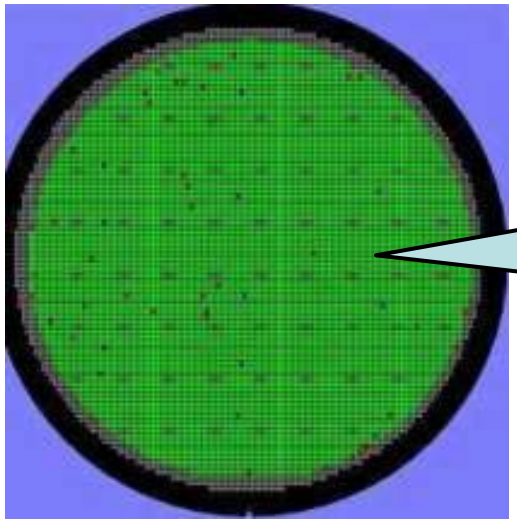
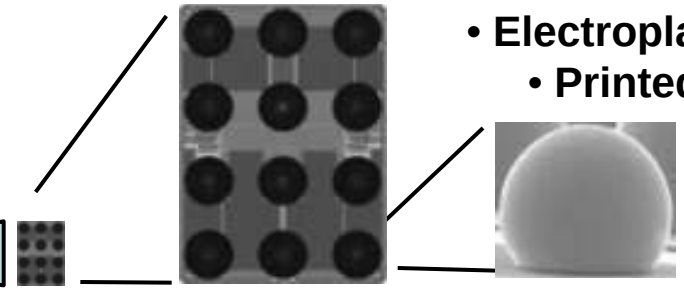
Chip Scale Packaging (CSP)

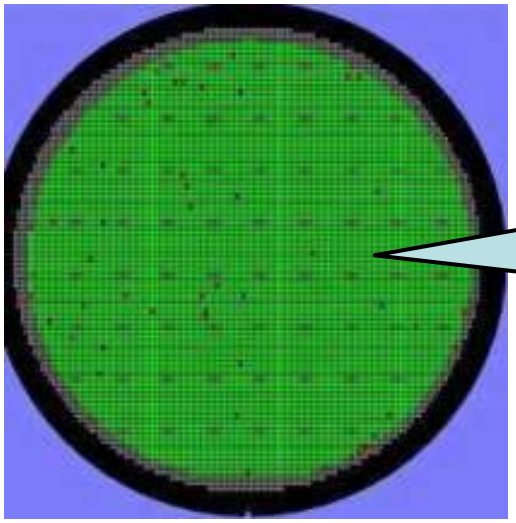


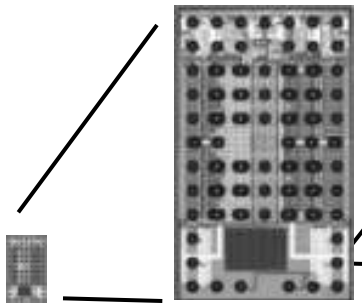


Solder Bumps
- **Ball drop**
- **Electroplated**
- **Printed**

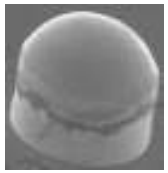
Wafer Bumping → Back Grind → Wafer Probe → Backside Coat → Laser Mark → Dicing → Optical Inspection

Flip Chip (FC) into Package

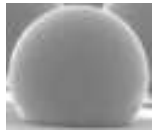




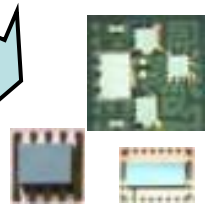
Copper Pillar Bump



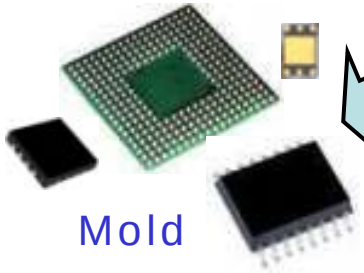
Electroplated Solder Bump



Wafer Bumping → Back Grind → Dicing



Flip Chip (FC)
Laminate or Leadframe



Mold → Final Test

History of Bumping and Process Types

The first bumping process was the C4 process (Controlled Collapse Chip Connection)

1. This was developed by IBM in the early 1960s.
2. It uses and evaporative process depositing both a Cr/Cr-Cu/Cu/Au UBM and a singular or binary element solder alloy through a molybdenum shadow mask.
3. The mask is manually aligned and clamped to the wafer. TCE changes/warpage are difficult to manage especially on larger wafer sizes. The mask has limited use – after 6 wafers it has to be re-worked by etching. A very expensive process ($>300/wafer)
4. After the UBM is applied, the first solder is evaporated (Pb), then a second solder(Sn), then both solders are reflowed to combine the two which blends the PbSn solder and allows the Sn to form an intermetallic compound with the Cu from the UBM.

History of Bumping and Process Types cont.

The FOC Process (Flex on Cap) now called the SFC (Standard Flip Chip) Process

1. In the 1960's Delco Delphi developed the FOC Process using a sputtered UBM to overcome some of the limitations of evaporated and electroplated bumps.
2. The UBM uses a sputtered Al/NiV/Cu or Ti/NiV/Cu. Solder is deposited by printing solder paste onto the UBM by an in-situ stencil (photo imageable resist), and reflowing the solder paste.
3. This is less costly than the evaporated processes and comparable in cost to electroplating.
4. Solder paste gives good control of the bump composition due to the powdered metal process.
5. This easily allows a variety of alloys to be used such as a single, binary, ternary or quaternary solder alloys.
6. The SFC (FOC) Printed solder bumps can also achieve very close spacing (70um pitch)
7. Solder voiding is the primary concern with customers today for the solder paste process

Bumping Process Types

Sputtered UBM with an Electroplated Solder Bump

1. The UBM may be a blanket layer of TiW/Cu or TiCu/Cu
2. Resist is applied, patterned and developed leaving an in-situ stencil with apertures for the plating of thick Cu and solder
3. Pitches of 50ums can be processed using electroplated solder depending on bump height
4. Bump heights are typically 125um or below
5. Electroplating has become especially popular for high bump count (>3,000) chips because of its small feature size and precision
6. Plating bath solutions and current densities must be carefully controlled to avoid variations in alloy composition and bump height across the wafer
7. Plating of solder is limited to single or binary alloys

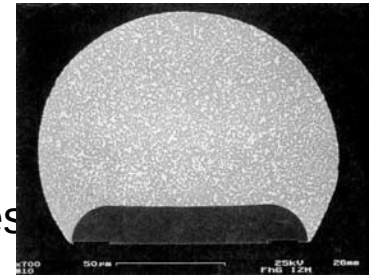
Additional Process Types cont.

Au stud bump

1. It's a serial bumping process, useable for small die, low I/O count per die and per wafer, or engineering prototype samples

2. Challenged on big die or high I/O count due to co-planarity and Thermo-compression bonding difficulties

ENIG and ENEPIG UBM



1. ENIG - Electroless Ni/Immersion Au Process (+ Tall Ni)

2. ENEPIG - Electroless Ni/electroless Palladium/Immersion Au Proces

3. Electroless process continues to grow Ni can easily grow to 50um's tall and 48um's wide

4. Immersion process is self limiting – Au thickness self limits at 800A to 1200A

5. This is the lowest cost UBM process

6. All wet batch chemistry process-can process 25-50 wafers at a time in typically 1 hour for 5um tall UBM. Many use 2 or 3 um's these days.

Additional Process Types cont.

ENIG and ENEPIG UBM cont.

8. Limitations to use this process:
   a) Metallurgy or Al pad must have 0.5% Cu
   b) Pad should have 1.0um thick Al/Si/Cu or Al/Cu
   c) Step coverage issues or passivation pin holes of exposed Al will plate up
   d) Pad size and passivation opening size must be correct for bump height
   e) No exposed PCM's or test structures in street that will affect sawing
   f) There is no mechanical or chemical bond between the passivation and the Ni. This interface can be a moisture and corrosion path.
   g) There can be preferential plating due to electrical potentials that cause some pads to plate while others will not. Typically of memory devices.

9. Solder deposited by mechanical stencil, FOC solder process, ball drop, solder jet.

Additional Process Types cont.

Plated thick Cu UBM with Sphere drop

1. The UBM is usually a blanket layer of Ti/Cu seed layer, followed by a plated Cu
2. Resist is applied, patterned and developed leaving an in-situ stencil with apertures for the plating of thick Cu
3. Typical customer requests today are for 5-12um's of plated Cu
4. Bump heights are typically 165um and up.

Why is this so popular today?

Why Cu UBM today?

- Sputtered metal versus Cu plating rates @ 1.5 to 2um/minute
- Cost – Thick plated Cu UBM is comparable to Sputtered UBM
- Majority of IMC growth occurs in first reflow and quickly plateaus leaving sufficient Cu UBM for a long interconnect life
- Thick Cu (Ti/Cu/Cu) has a longer MTTF than “thin” sputtered Cu (Al/NiV/Cu) regardless of temperature and current density
- Increasing use of Cu pillars provides for finer pitch and higher current density
- Cu Pillar typically allows for over-molding to be used instead of underfill

Copper Pillar versus Solder Bumps

1. Physical properties

Material	Resistivity (10^{-6} Ohm-m)	Thermal conductivity (W/m-K)
Cu	0.017	385
Sn	0.115	63.2
Improvement (Cu over Sn)	***6.7X***	***6.1X***

2. Current carrying capability

Material	Estimated current carrying capacity at 10 Deg C temperature rise
200um Cu pillar diameter	1.2 A
200um SAC ball	0.35 A
Improvement (Cu over Sn)	***3.4X***

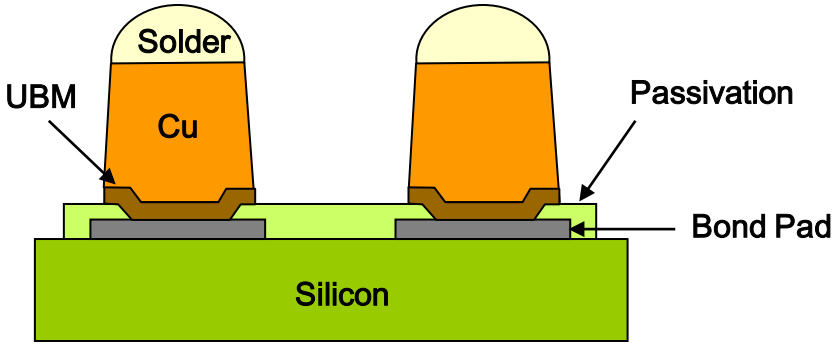
3. Advantages of copper pillar bumps

Standoff and spacing remain intact after reflow (copper pillars do not collapse like solder after reflow).

As a result,

1. Copper pillar bumps can achieve a smaller pitch and height.
2. It is easier to underfill copper pillar bumps compares to solder bumps of the same pitch and height.

Process Types cont.



Cu Pillar

1. Typically the seed layer is a Ti/Cu

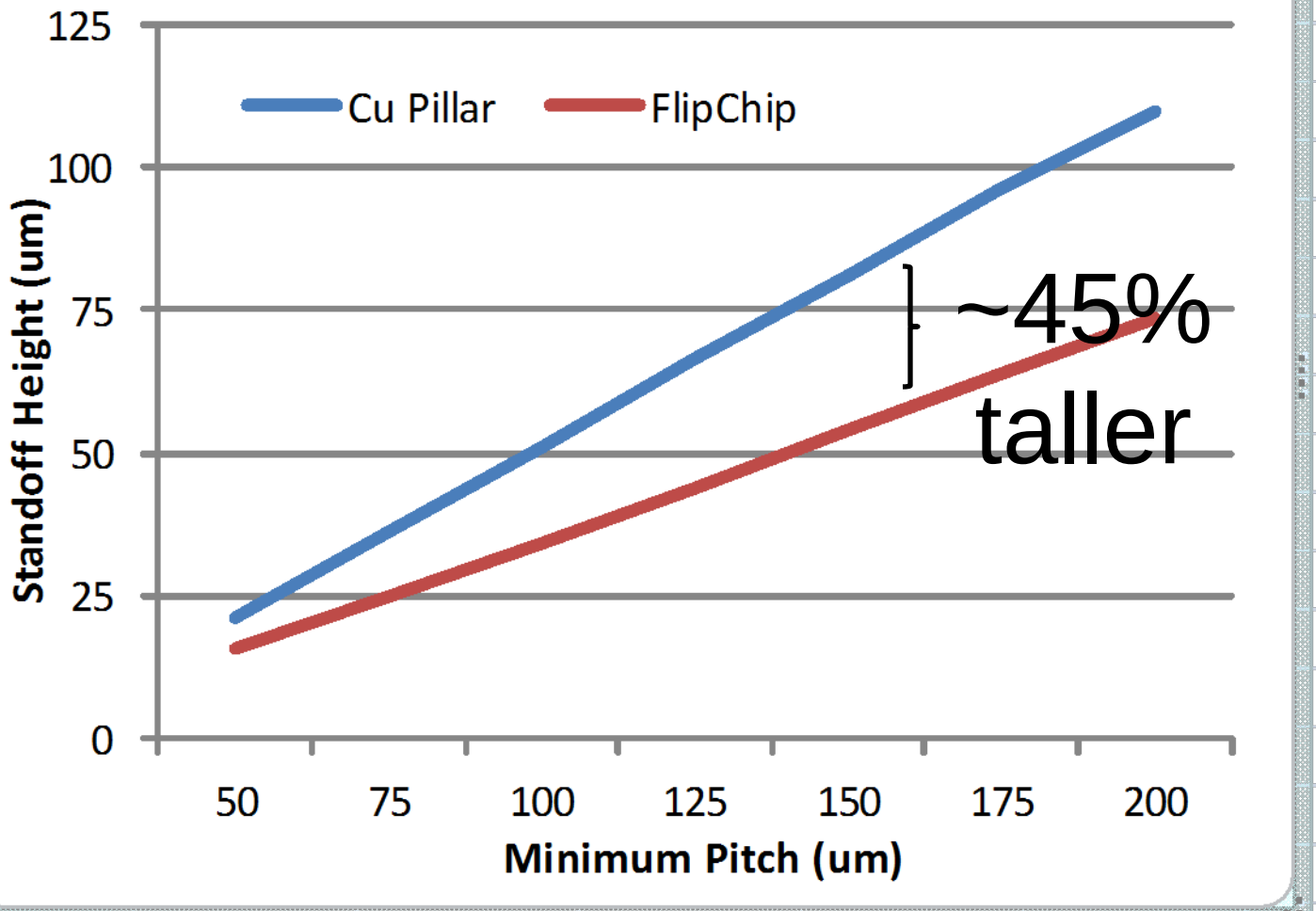
2. A photo-imageable resist (either a dry film or spin on) is used to define where Cu will plate up

3. Solder can then be applied through a paste or electroplated process

4. The resist is then stripped, excess seed layer material is etched and then the solder may be reflowed

5. Primary benefits are:
    1. Controlled standoff
    2. Improved Electrical performance
    3. Current carrying capability and resistance to Electromigration
    4. Thermal dissipation benefits

Cu Pillar stand off height benefits

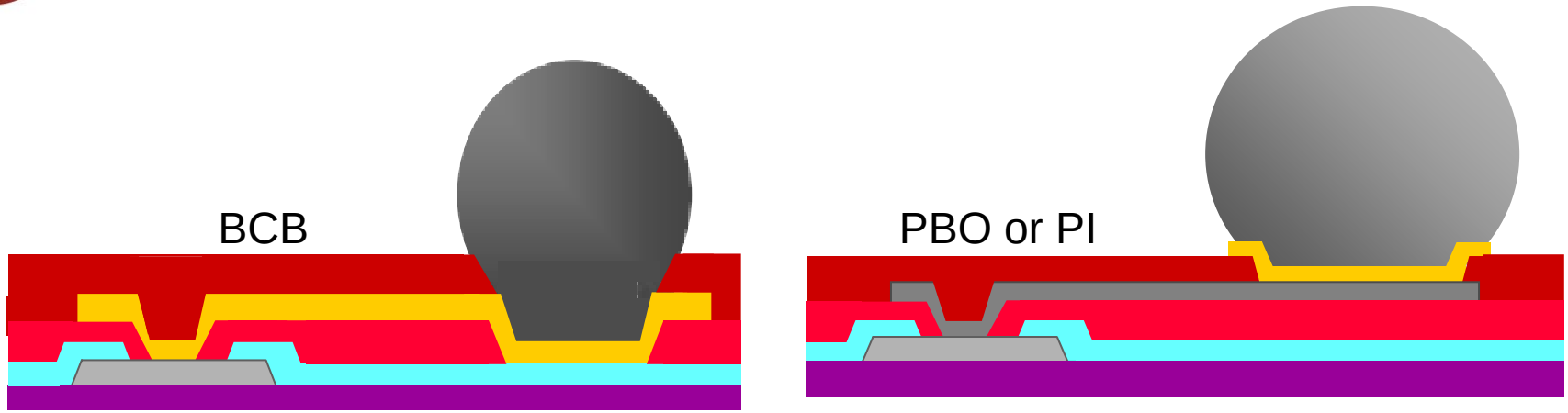


Why is Cu Plated RDL the choice today?

- All of the benefits for plated Cu RDL from the previous slide apply- reduced resistance, increased current carrying capability, improved thermal transfer

- Plus line and space and thickness advantages-
- Ti/Al/Ti RDL provides a minimum of 25um line and 12um space with a thickness of 2um's
- Plated Cu RDL provides a minimum of 12um line and 8 um space for a thickness of 3-5um's plated Cu
- OR plated a thicker Cu RDL provides a minimum 20um line and 30 um space for a thickness of 10-12um's of plated Cu

Polymer choices today



RDL redistribution 1 metal layers and polymer differences

1. RDL maybe sputtered Ti/Al/Ti or Ti/Cu seed layer with plated Cu
2. PBO/PI provides for better electrical isolation than BCB because it will reside on top of the first dielectric layer and BCB must be anchored on the native passivation

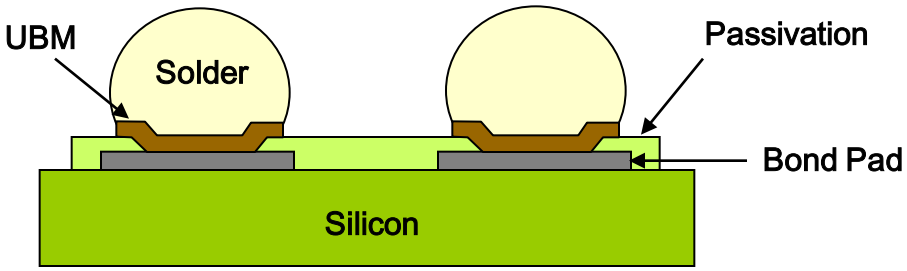
Repassivation Materials and Properties

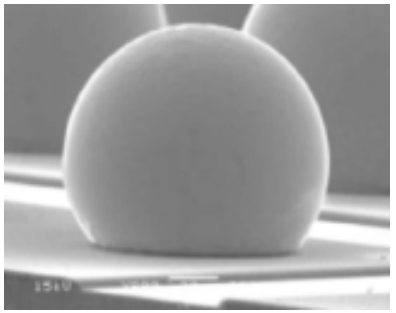
	BCB benzocyclobutane	PBO Polybenzoxazole	Polyimide HD4110
Dielectric Constant	2.65	2.97	3.2
Curing Temperature	250C 1 hr	320C ½ hr	375C 1 hr
Dissipation factor	0.0008	0.01	0.003-0.008
Glass transition Temperature Tg °C	>350°C	284°C	285°C
CTE (T<Tg)	52	31	55
Tensile Strength (Mpa)	87	148	215
Young's Modulus (Gpa)	2.9	2.8	2.5
Density (at room temp) g/cm³	~1.6	~1.4	~1.4
Elongation %	8	56	85
Water Absorption	0.2	0.3	1.08

Differences between plated and solder paste

Plated Solder	Solder Paste
• Begins plating from “0” height and is suitable for smaller pitches • Preferred for high I/O count devices • Limited to single or binary alloys • Height uniformity influenced by current densities across the wafer/die for both Cu and the solder (amplified) • Less susceptible to voiding • Bath must be adjusted to provide consistent alloy %’s as plating occurs at different rates	• Pitch slightly larger than plated bumps • Ternary and quaternary alloys are used • Alloy changeover is very easy offering a huge selection of solder pastes • Voiding is more prevalent • Missing bump more likely than plated • More suitable for lower I/O count devices • The solder Ingot process provides for excellent metallurgical alloy control

Solder Bump Process options at Unisem





Re-passivation
- Polyimide
  - HD4100
  - HD4110
- PBO
  - Spheron
- HD8820 pending
- BCB (UAT only)
  - 4022

UBM
- Ti-Cu-Ni
- Ti-Cu
- Ti-NiV-Cu
- Al-NiV-Cu

Solder
- Plated SnAg
- Plated Sn
- Ball drop SAC
- Printed SAC
  - Resist UC & UAT
  - Stencil UC

RDL-runners
- Ti-Cu
- Ti-Al-Ti

Pitch
- Plated: >150µm
- Ball drop: >200µm
- Printed: >150µm

Bump height
- Plated: 40 - 100µm
- Ball drop: 70 - 280µm
- Printed: 63 - 125µm

Thank You!

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