Thermal Characterization and Modeling: a key part of the total packaging solution

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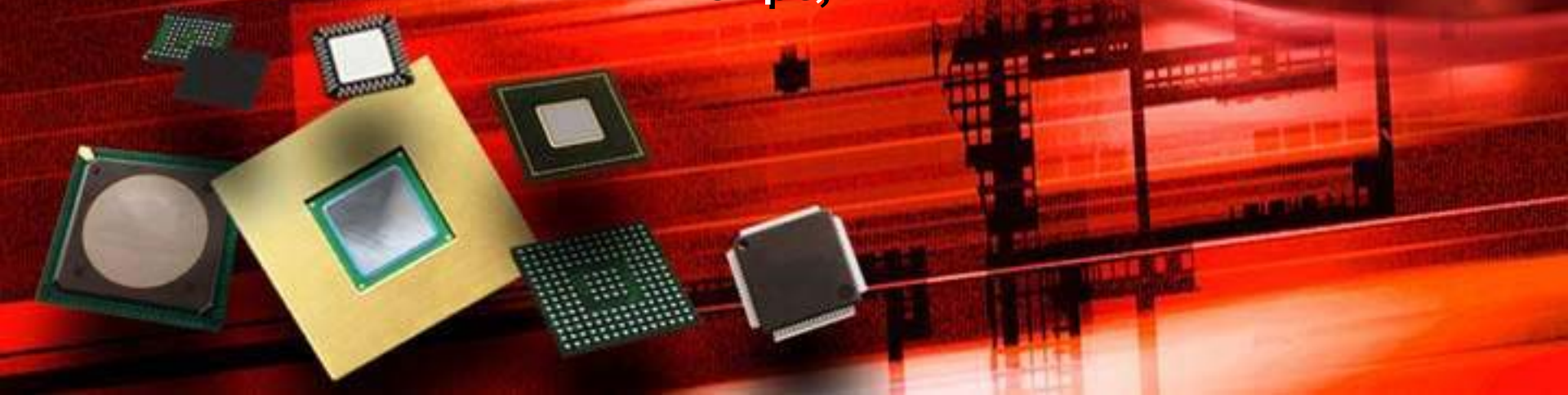

Outline:

- Introduction
- Semiconductor Package Thermal Behavior
  - Heat Flow Path
- Stacked Die and SiP/MCM
- Early Thermal Simulation
  - Simplified Package Models
- System Level Design
  - Using Compact Models
- Other Thermal Challenges To Watch For
- Summary

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Introduction:

Anything can be cooled for a price

- Packaging solutions must meet several requirements
  - Mechanical, Electrical, and Thermal
- Finding the best thermal packaging solution among those available
  - meets thermal requirements (and all the others)
  - lowest cost
  - reliable/high volume capable
- Early Simulation
  - Make changes early, avoid costly design rework and/or tooling costs
  - Must consider full thermal picture, from die to system

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Semiconductor Package Thermal Behavior

- Initial package selection places limits on thermal capabilities
  - How easily can the heat move away from the die and spread to a larger area?
  - Once heat has moved away from the die vicinity, are there enough low resistance paths to get it out of the package?
  - Does the package respond well to addition of heat sink or other cooling enhancements?
- Understanding the overall thermal requirements and using early simulation allows best initial selection of package family.

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Semiconductor Package Thermal Behavior

- Local Issues
  - Die size, power density, interconnection,
  - Materials in contact with die
- Package Issues
  - Lead/Ball count, size constraints, layers, thermal enhancements (drop-in spreaders, exposed pads, thicker copper layers, ...)
- Global Issues
  - Environment- airflow and ambient temperature
  - Enclosure- overall size, vents, fans, other heat sources

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Semiconductor Package Thermal Behavior:

Materials

- Die Attach-
  - thickness, conductivity (be cautious of manufacturers data)
- Soldermask
  - adds significant thermal resistance in low resistance packages and those with high power density
  - openings can help thermally but can also effect reliability
- Molding Compound
  - usually not to important unless the key heat flow path includes it
- Drop-in Heat Spreaders
  - heat must pass through mold compound to enter spreader
  - most effective for smaller die in large package
  - very good for 2 layer array packages with otherwise poor heat spreading in x-y directions

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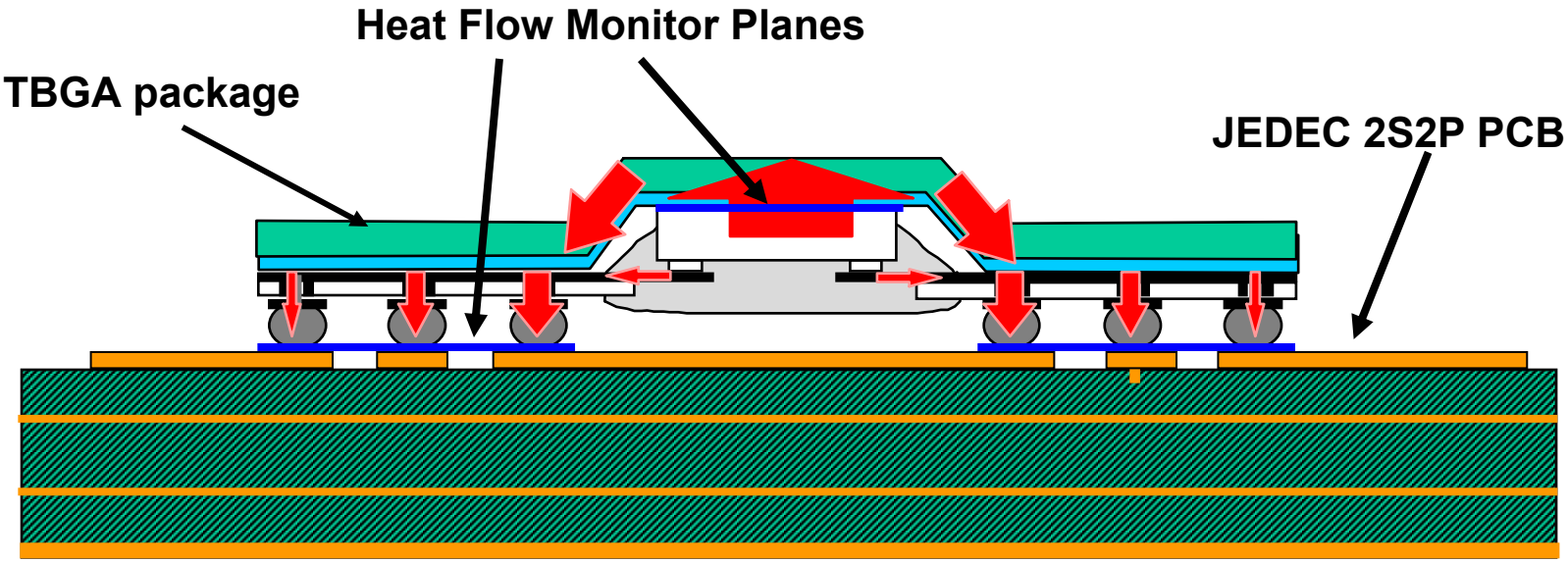
Semiconductor Package Thermal Behavior:

Key Heat Flow Paths

- Understanding heat flow paths allows correct thermal structure models that maintain thermal flow
- Software monitors heat flow across user defined planes



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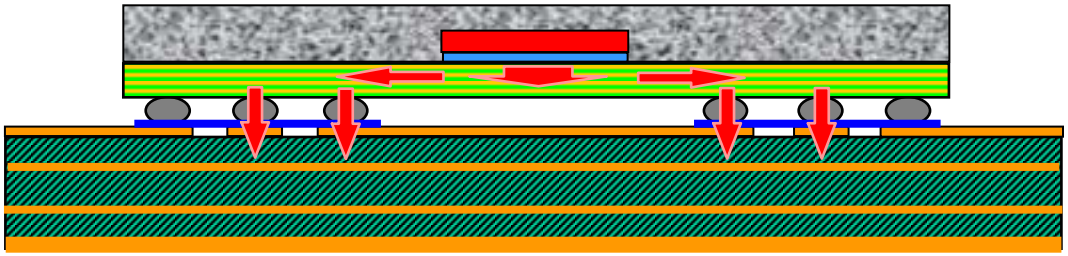
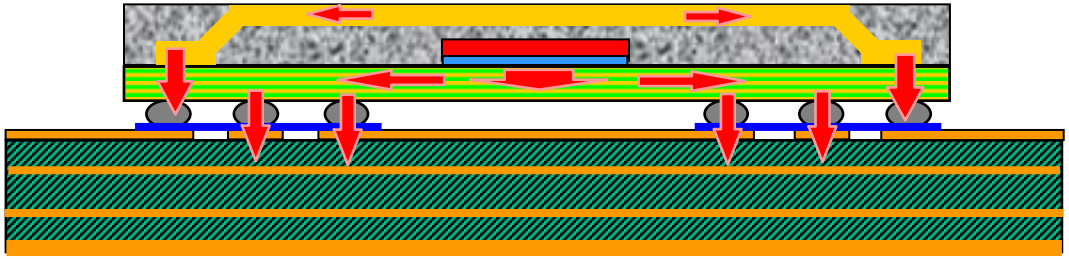
Semiconductor Package Thermal Behavior:

Key Heat Flow Paths

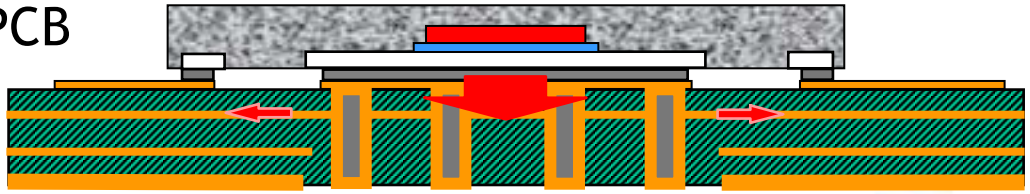
- PBGA-
  - individual molded
  - matrix molded



- PBGA-Heat Spreader
  - enhanced x-y spreading



- Exposed Pad Lead-Frame Based
  - direct thermal path to PCB



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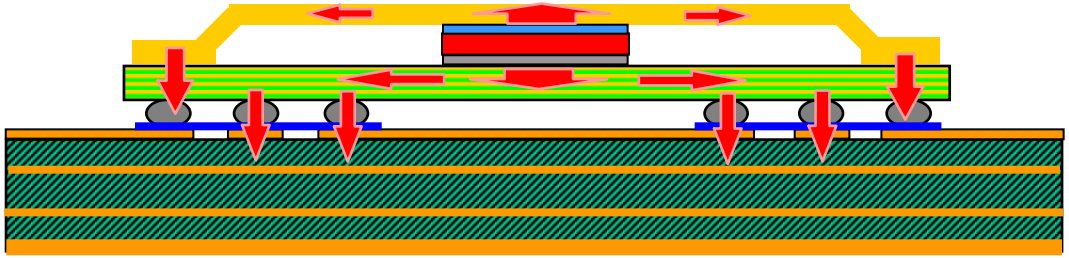
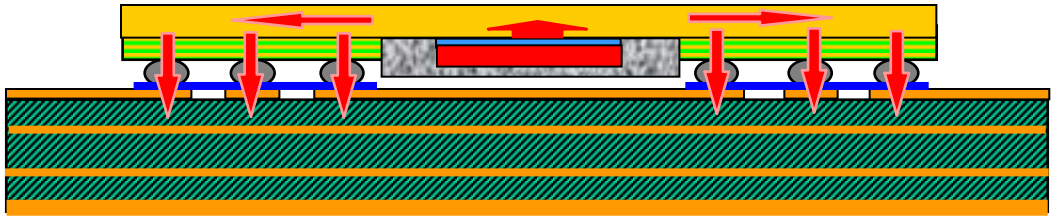
Semiconductor Package Thermal Behavior:

Key Heat Flow Paths

- Flip chip PBGA-



- Wire Bonded EBGA



  - Both of these respond well to heat sink addition

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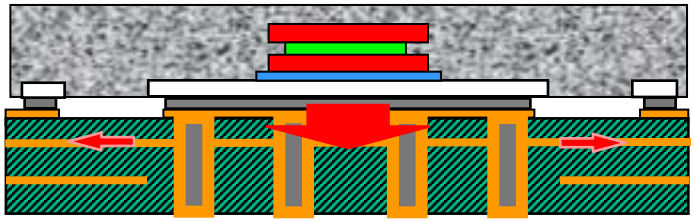
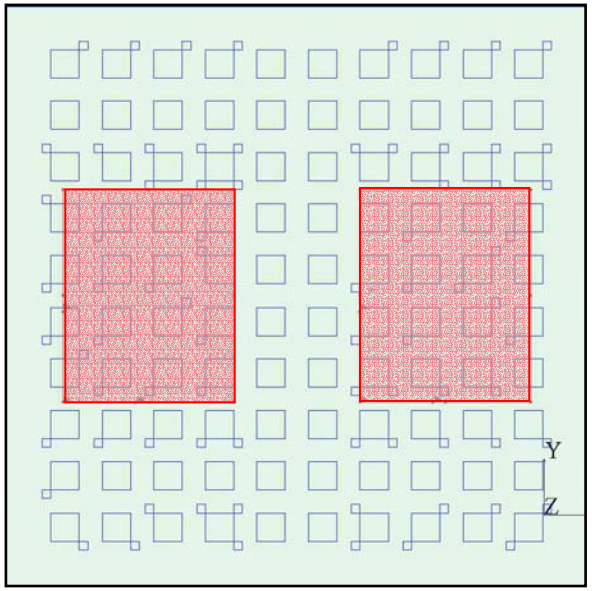
Stacked Die and SiP/MCM Systems

- Added geometric complexity
  - No modeling problems when full geometry is used
- Potential change in critical heat flow path
- Effect on thermals varies
  - can be good or bad...



Same size die stack,
poor conductivity spacer between

No problem if top die is low power
Big problem if top die is high power



9x9mm PBGA with side-by-side Die

Lots of die area to move heat down, which is good for overall thermal resistance

But if enough power is added to the package, it can still get too hot.

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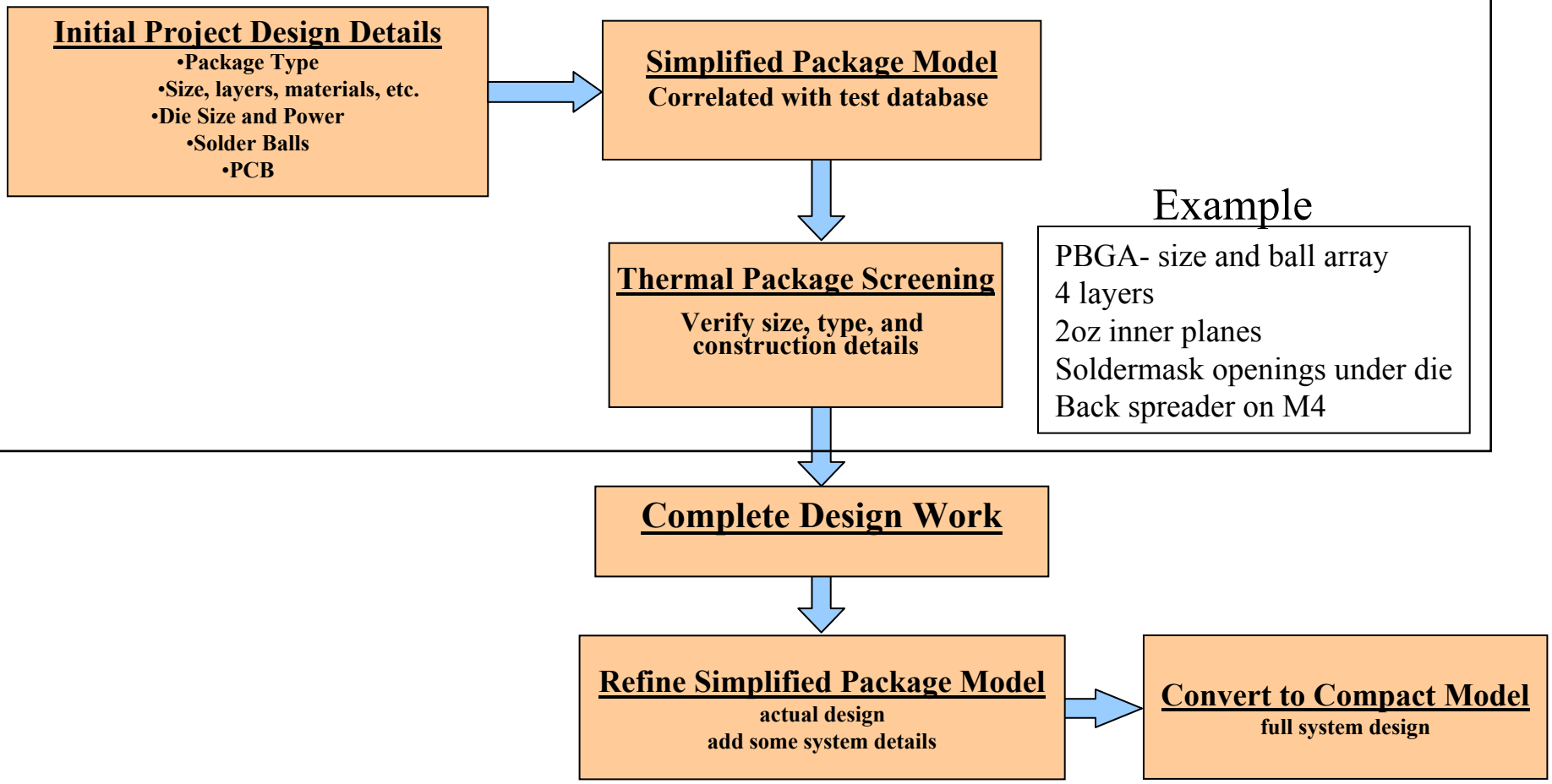
Early Thermal Simulation



Ideally, the same modeling approach can be carried through entire process, from feasibility to system design

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Early Thermal Simulation

- Simplified Package Model-
  - Still a detailed 3D model but not an exact copy of the geometry or design
  - Several ways to accomplish this-
    - Limited design information through to Full design
    - Good accuracy at first, better as design details are confirmed
    - Full 3D geometric model, just simplified internal structures
    - Initial work on JEDEC defined test board, moving to custom board if/when details become available
- Initial Goals:
  - Narrow the range of packaging choices
  - Eliminate those that will not work
  - Early guidance if thermal additions are or might be required
    - heat sinks, PCB vias, cold plates, etc...

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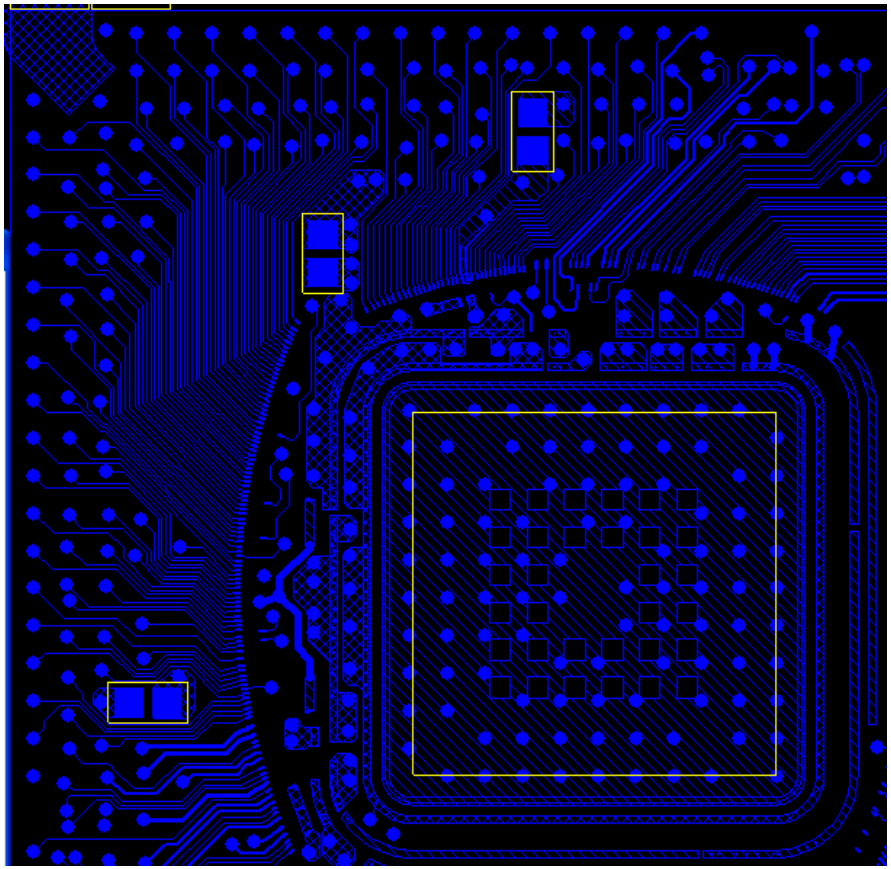
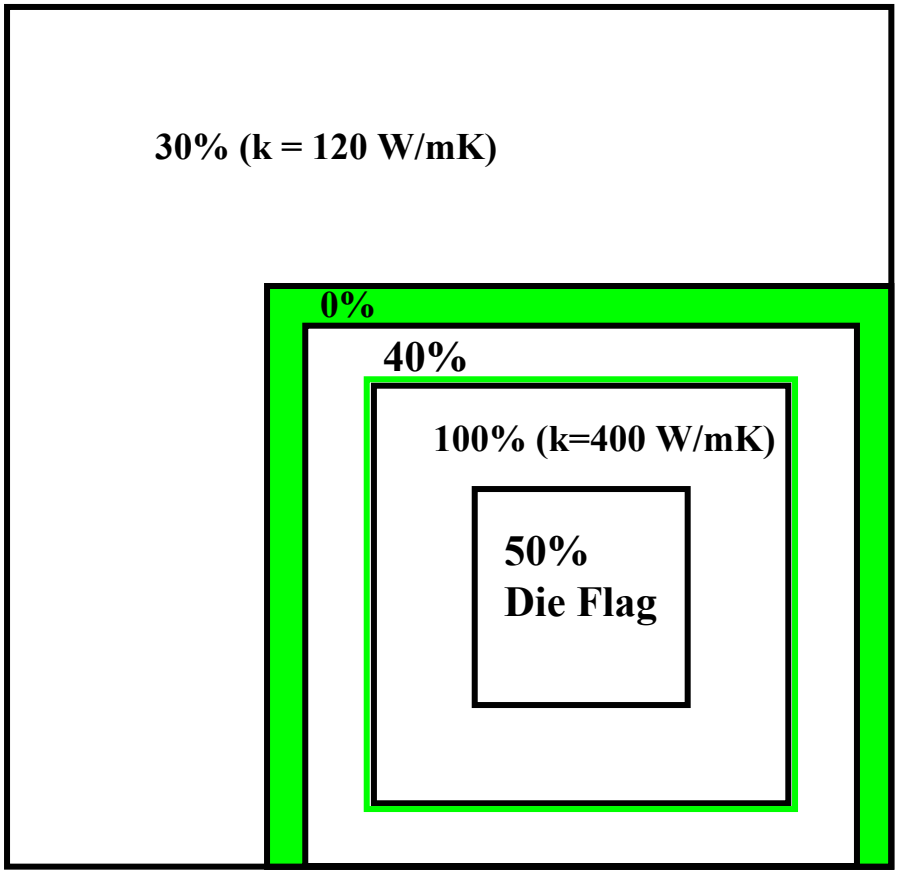
Early Thermal Simulation:

Large 4 Layer PBGA Example

- Top Metal Layer





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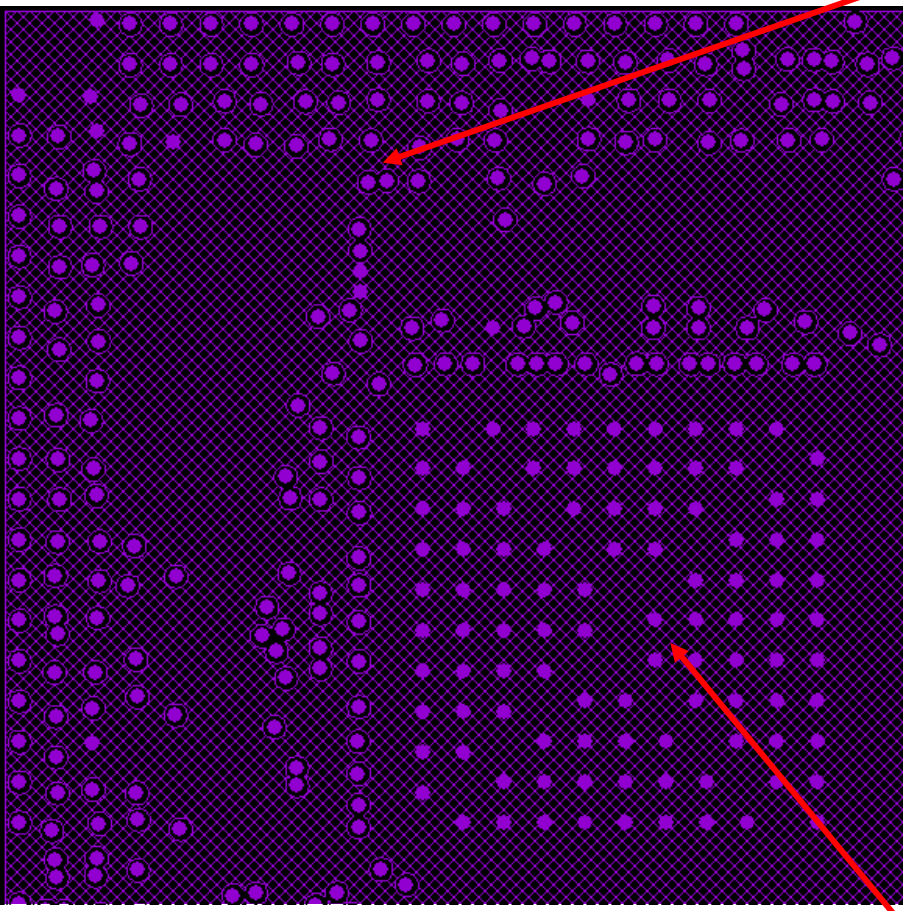
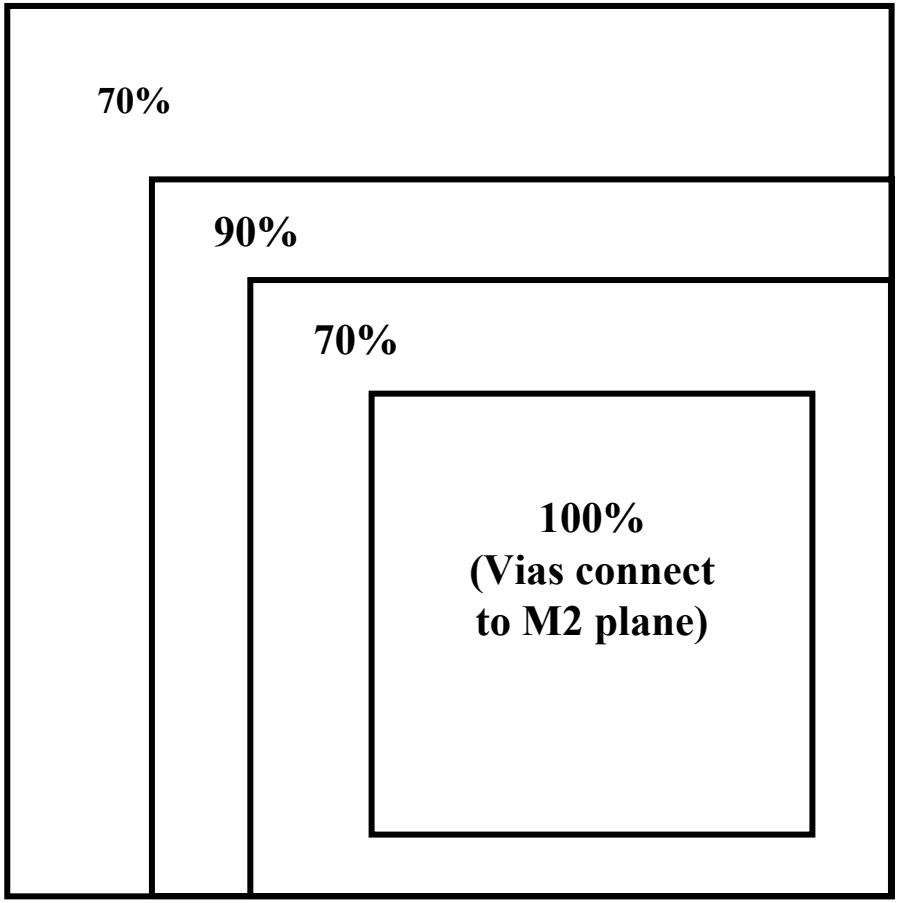
Early Thermal Simulation:

Inner Planes

Signal vias: do not connect to M2 plane
reduce their conductivity





Thermal vias: connect to M2 plane

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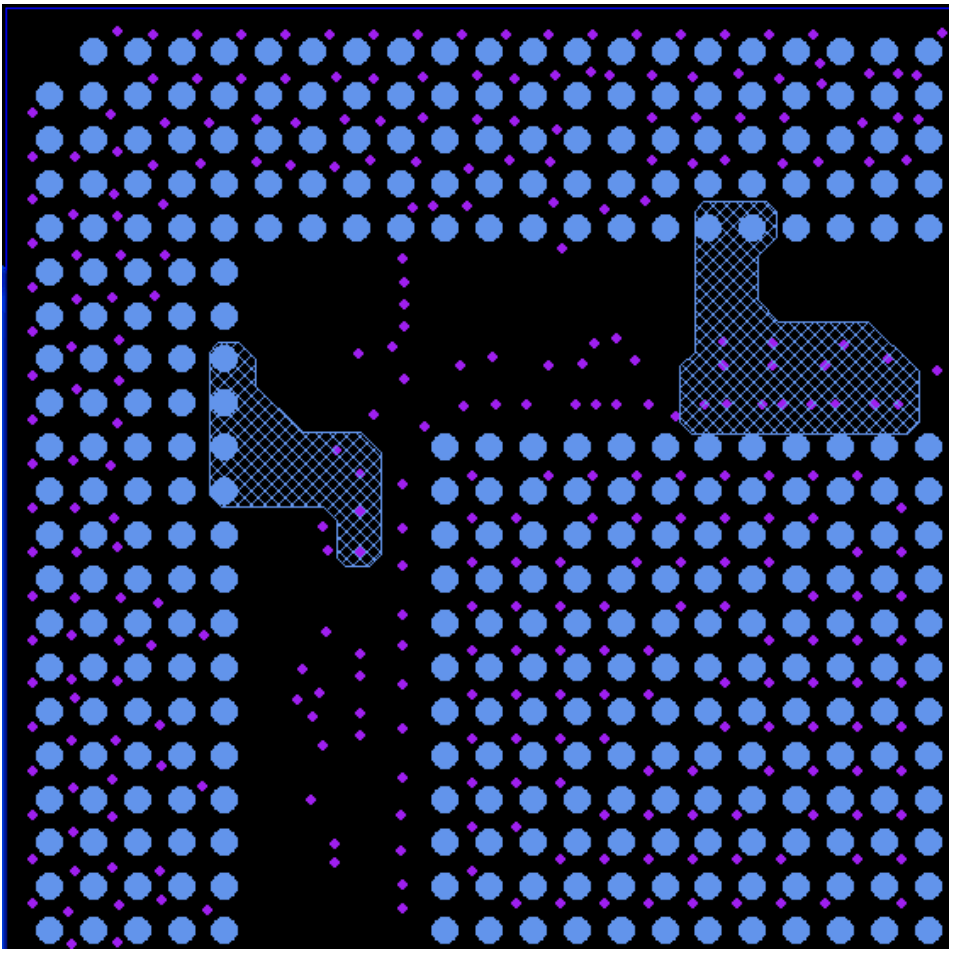
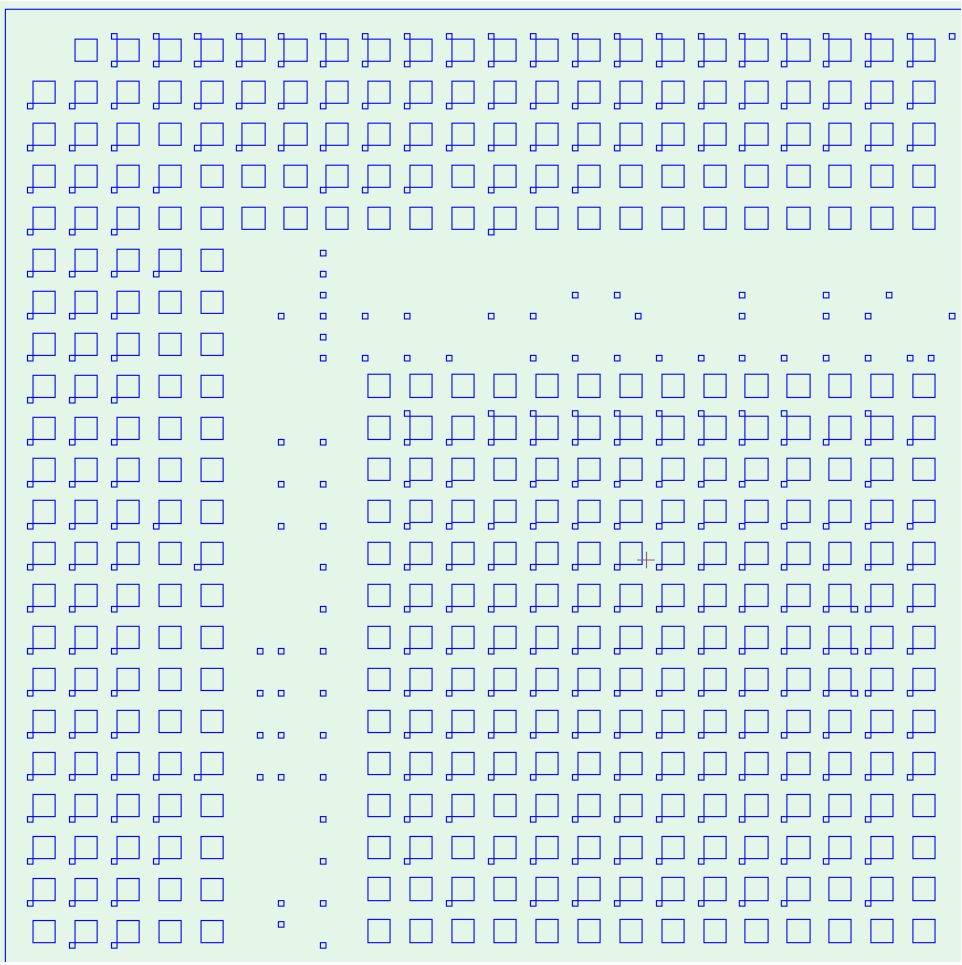
Early Thermal Simulation:
Solderballs and Vias

If no design information is available, assume 1 via per solder ball





Solder balls: 0.5mm diameter = 0.44mm square

Vias: 0.15mm diameter = 0.133mm square

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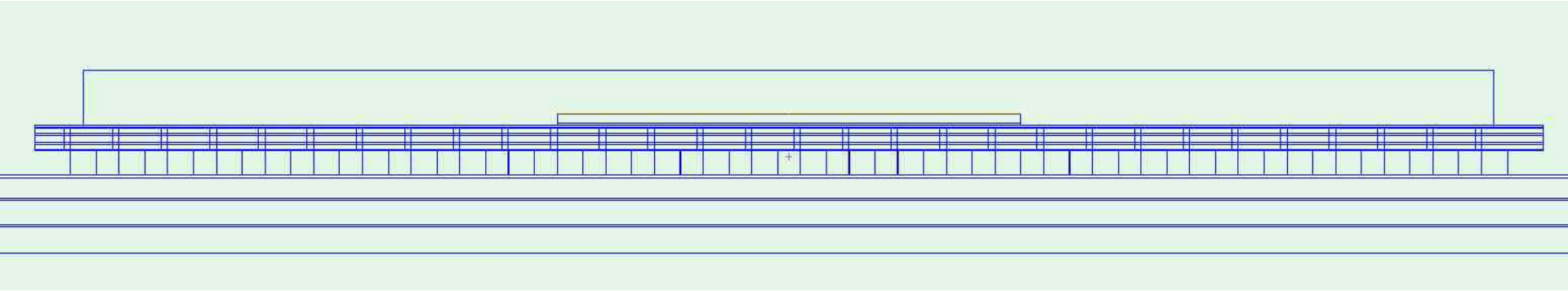
Early Thermal Simulation:

Summary

- Side view of simplified package model



- Focus on important heat flow paths
- Compare results to test data on similar structures
- Make conservative compromises when minimal design information is available
- Θja error goals/results:
  - pre-design: -0% to +20%
  - design available: -0% to +10%
  - design and package structure (actual part cut-up): -0% to +5%

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System Level Design:

Compact Package Models

- Much larger modeling domain
  - full PCB boards
  - many packages/devices
  - fans
  - enclosure/vents
- Even simplified package models contain too much geometrical details
- Move to a Delphi type compact model
  - Resistor network
  - Boundary Condition Independent

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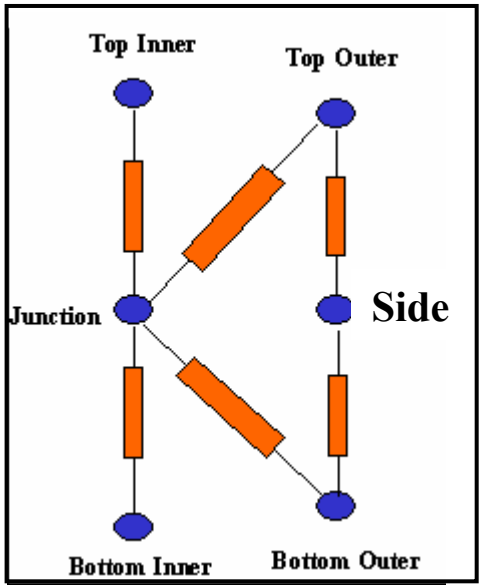
System Level Design:

Compact Package Models

- Convert Accurate Package model to a resistor network
- Optimize resistors and block sizes to obtain best fit based on a matrix of 44 sets of boundary conditions.



Heat Transfer at boundaries in W/m2

5, 1, 5, 100
5, 10, 5, 1000
5, 50, 5, 1000
5, 50, 5, 4000
5, 100, 5, 1000
5, 100, 5, 500
15, 1, 15, 100
15, 10, 15, 1000
15, 50, 15, 1000
15, 50, 15, 4000
15, 100, 15, 1000
15, 100, 15, 500
30, 5, 30, 500
30, 30, 30, 3000
30, 200, 30, 10000
30, 500, 30, 2000
80, 5, 8, 500
80, 30, 30, 3000
80, 200, 8, 10000
80, 500, 8, 2000
200, 5, 20, 500
200, 30, 20, 3000
200, 200, 20, 10000
200, 500, 20, 2000
25, 1, 5, 100
25, 10, 5, 1000
25, 50, 5, 1000
25, 50, 5, 4000
25, 100, 5, 1000
25, 100, 5, 500
75, 1, 15, 100
75, 10, 15, 1000
75, 50, 15, 1000
75, 50, 15, 4000
75, 100, 15, 1000
75, 100, 15, 500
150, 5, 30, 500
150, 30, 30, 3000
150, 500, 30, 2000
150, 200, 30, 10000
500, 5, 20, 500
500, 500, 20, 2000
500, 30, 20, 3000
500, 200, 20, 10000

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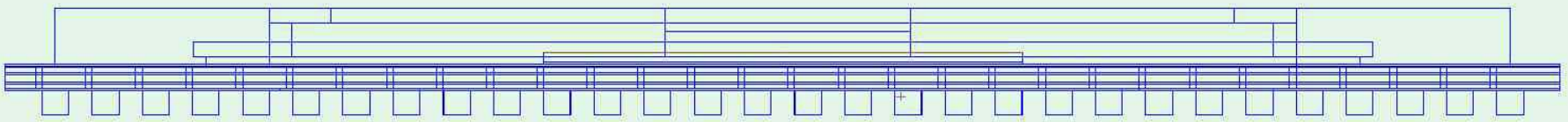
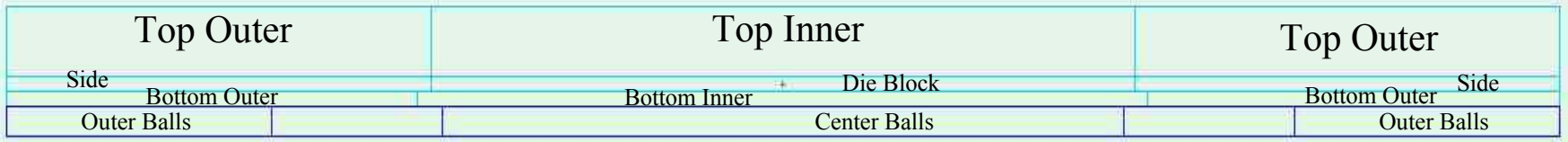
System Level Design:

Compact Package Models

- Example Simplified Package Model: PBGA with Heat Spreader:



- Compact Model:



- Blocks are connected by thermal resistors (°C/W)

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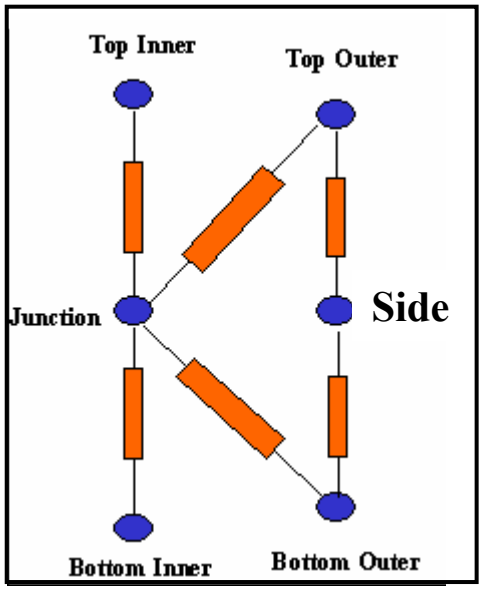
System Level Design:

Detailed versus Compact results



Example Resistor Network

	Top Inner	Bottom Inner	Top Outer	Bottom Outer	Side
Junction	5.02	6.81	6.21	108.02	**Infinity**
Top Inner		24.74	**Infinity**	**Infinity**	**Infinity**
Bottom Inner			**Infinity**	14.86	134.82
Top Outer				1.54	3.46
Bottom Outer					**Infinity**

Power (W)	PCB Size (mm)	PCB Layers	PCB Copper (M1 & M6)	PCB Via Block	Heat Sink	Θ_{JA} ($^oC/W$) Detailed	Θ_{JA} ($^oC/W$) Compact	% error
5.2	60 x 95	6L	60%	Yes	No	9.80	9.75	0.5 %
5.2	62 x 93	6L	60%	Yes	Yes	8.85	8.75	1.4 %
3.0	JEDEC	4L	20%	No	No	11.45	11.25	1.7 %

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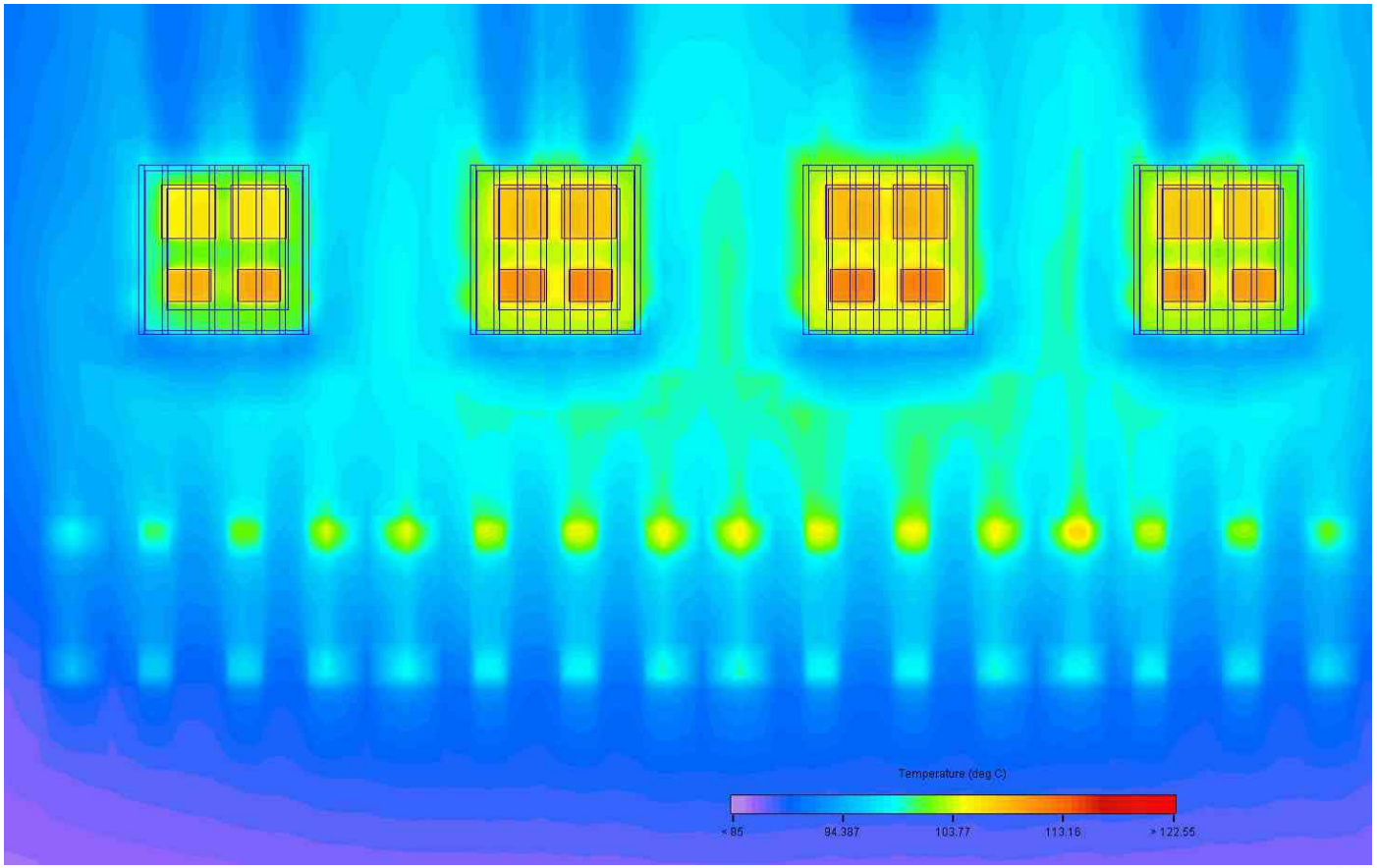
System Level Design:

Large PCB Example

4 PBGA packages with heat sinks,
forced convection: 1 m/s
32 Exposed Pad No Lead Packages, all with PCB vias



200mm x 360mm 10 layer PCB

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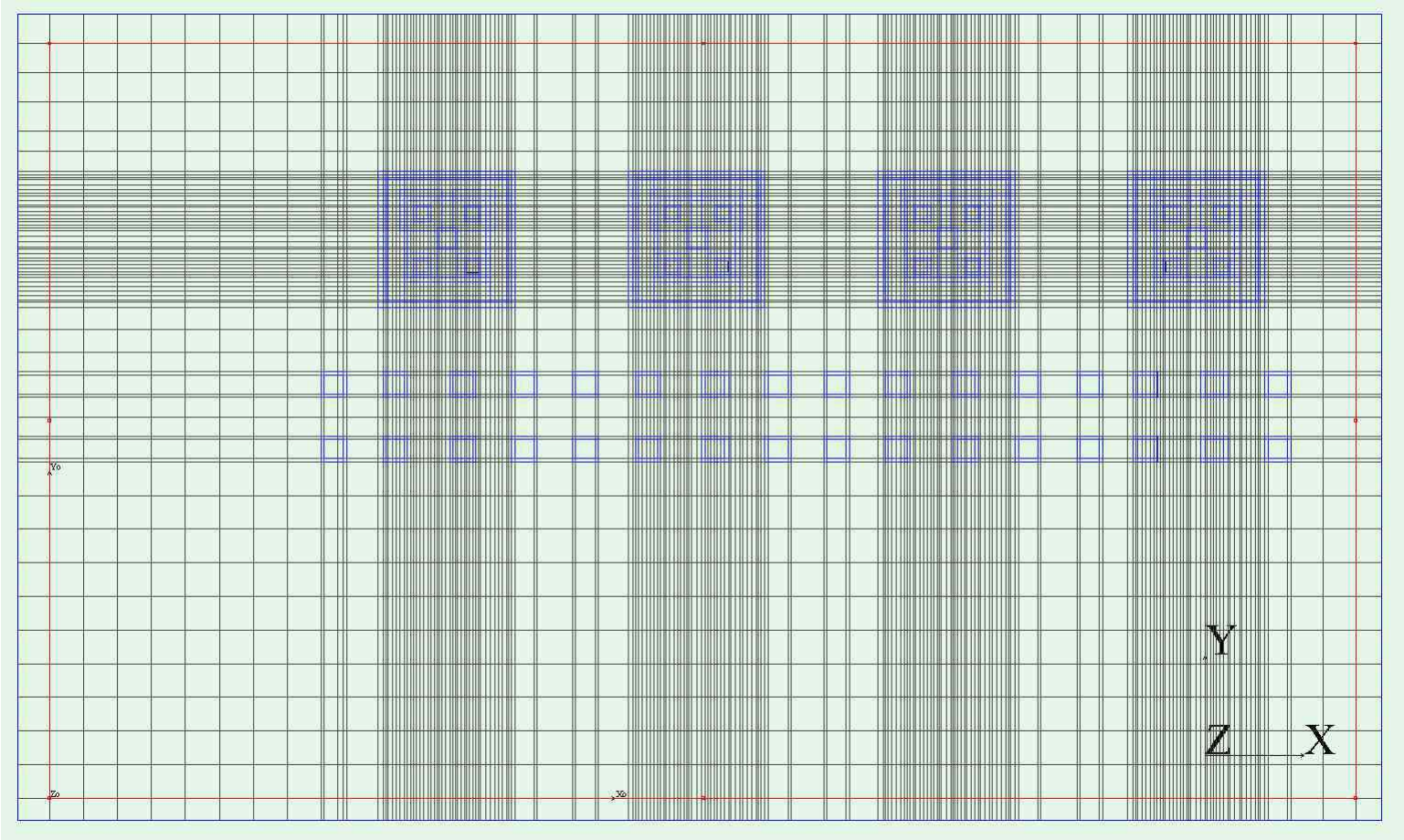
System Level Design:

Large PCB Example

Using simplified models >1M grid cells



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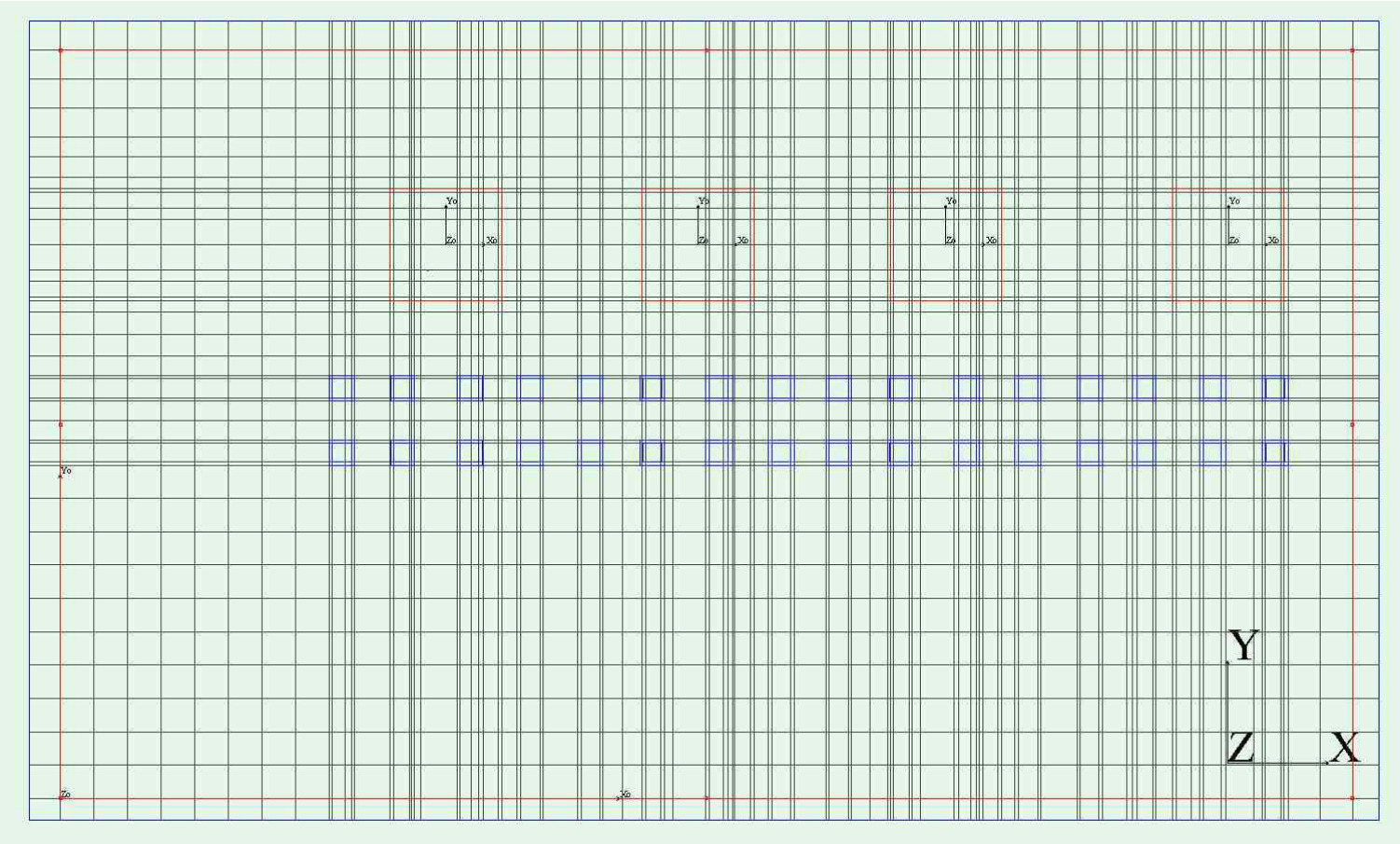
System Level Design:

Large PCB Example

Using compact models <200K grid cells



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Other Thermal Challenges To Watch For

- Increased Ambient Temperatures
  - 40°C (desktop/telecom), 70°C, 85°C, 105°C (automotive)
  - With a 125°C Tj limit, these give available die temperature increases of: 85°C, 55°C, 40°C, and 20°C
- Reduced Junction Maximum Temperatures
  - 105°C can totally change overall approach
- Increased Total System Power Dissipation
  - Transition from passive to active heat removal
  - Significant cost issue for some systems, can be a show stopper
- Die Size Reductions
  - Smaller die size with same power gives an increased power density
  - Everything thermal gets more difficult

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Summary

- Consider Thermal as early as possible
  - keep maximum options open
- Use Simulation early in the process
  - no need to wait for exact design details
- Select Package type carefully
  - don’t get trapped in the wrong package family
- Extend Simulation through to final system design
  - Simplified package models using full geometry can go far
  - Compact Delphi models for the most challenging systems

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