1. IC PKG Trends & Issues

2. Organic Interposer of 2.5D Packaging

3. Key Challenges
1. IC PKG Trends & Issues
Cost Trend

Micro System Level Module Packaging could lead the higher packaging cost, and the packaging cost could be concerned on business plan.

※ Source: Freescale Semiconductor (2007)
Performance Bottleneck

Interconnect on chip would be a serious factor for IC Performance

※ Source: EMC-3D Japan/Korea Technical Symposium April 23-27, 2007
Wide I/O Memory could be appeared soon, and it would be applied on mobile first with increasing the Bandwidth dramatically.

Bandwidth Requirement

※ Source: 3-D Integrated Circuits Workshop 2012
Wide I/O Memory needs a fine pitch interconnection with high I/O: Could PKG substrate be responded for the fine pitch interconnection?

<table>
<thead>
<tr>
<th>Mobile Processor</th>
<th>2011</th>
<th>2012</th>
<th>2013</th>
</tr>
</thead>
<tbody>
<tr>
<td>GFX</td>
<td>Single-Core 400MHz</td>
<td>Multi-Core 500MHz</td>
<td>Multi-Core 800MHz</td>
</tr>
<tr>
<td></td>
<td>0.5 Gby/s</td>
<td>3 Gby/s</td>
<td>&gt; 6 Gby/s</td>
</tr>
<tr>
<td>Display</td>
<td>qHD60 + 1080p30</td>
<td>1080p60 + 1080p30</td>
<td>4M60 + 1080p60</td>
</tr>
<tr>
<td></td>
<td>1 Gby/s</td>
<td>2 Gby/s</td>
<td>&gt; 4 Gby/s</td>
</tr>
<tr>
<td>Total</td>
<td>1.5 Gby/s</td>
<td>5 Gby/s</td>
<td>&gt; 10 Gby/s</td>
</tr>
<tr>
<td>DRAM Configuration and Bandwidth</td>
<td>Single Channel LPDDR2 @ 400MHz</td>
<td>Dual Channel LPDDR2 @ 533MHz</td>
<td>Quad Channel Wide I/O</td>
</tr>
<tr>
<td></td>
<td>3.2 Gby/s</td>
<td>8.5 Gby/s</td>
<td>12.8 Gby/s</td>
</tr>
<tr>
<td>DRAM sub-sys’ Power/Bandwidth</td>
<td>80 mW/Gbyps</td>
<td></td>
<td>40 mW/Gbyps</td>
</tr>
<tr>
<td>Pin</td>
<td>194</td>
<td>194</td>
<td>1128</td>
</tr>
</tbody>
</table>

※ Source: 2011 ST ERICSSON
An interconnection gap between IC to PCB is increased due to the current PCB technology limit not matched for IC interconnection scale down, and so on.

※ Source: Yole 2010, 3D silicon and glass Interposers
Packaging Interconnection

Proposed roadmap of package architecture transitions to address the memory bandwidth challenge [Intel 2007]

Embedded PCB Overview

- Any (active/passive) components can be embedded in PCB core layer.
- Interconnections can be formed thru conventional laser drilling and Cu plating technology.
- Low profile MLCCs are used for embedding.

![Diagram of Embedded PCB](image)

- **Via**
- **Bump**
- **Core**
- **Stack Via Available**
- **Active Component**
- **Solder Resist**
- **Active IC embedded**
- **Passive embedded**
- **MLCC**
- **Chip Resistor**
Embedding technology is especially for small form factor. The sizes of packages, modules and boards can be reduced via embedding technology.

- **Size reduction for modules**

  - Conventional module: 10.0x8.0 (80mm²)
  - Embedded passive module: 10.2x5.0 (51mm²)
  - 36% reduction
  - 75.76mm² saving

- **Function addition**

  - Passive components (132ea) embedded
  - Additional functional block

- **Embedded System-in-Package**

  - 3 packages (144.4mm²)
  - 44% reduction
  - 1 package (81mm²)
Decoupling capacitors are commonly used to stabilize the power supply voltage levels.

Embedded decoupling capacitor provides a lower Interconnection inductance affected to the noise value of power and ground network.
Embedded PCB shows lower junction temperature because of short path of heat flow from chip to mother board

Thermal simulation of power amp module (4-chip PKG, z-plane cut view)

Tj : Die max. temperature (Assume that Mother Board Temp. is 25 °C)
The interconnection and Package structure could be considered with IC thermal dissipation and performance.

### 3D (Vertical Stacking)

- **Advantage**: Minimization of Package Size
- **Disadvantage**: Difficult Thermal Dissipation
- **TSV/Chip Stacking Technology**

### 2.5D (Interposer Stacking)

- **Advantage**: Easier Thermal Dissipation
- **Disadvantage**: Increase Package Size
- **Chip Mounting Technology**

※ Source: http://prohardver.hu/hir/amd_integracio_rogos_utja.html
IC Power Consumption

It is important to consider the power consumption of ICs in application: GPU power consumption will be bigger.

<table>
<thead>
<tr>
<th></th>
<th>Desktop</th>
<th>Notebook</th>
<th>Ultrabook</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU (TDP)</td>
<td>35~77W</td>
<td>25~57W</td>
<td>15~17W</td>
</tr>
<tr>
<td>GPU (TDP)</td>
<td>140~250W</td>
<td>60~100W</td>
<td>14~35W</td>
</tr>
<tr>
<td>Battery capacity (Wh)</td>
<td>-</td>
<td>60~95Wh</td>
<td>36~54Wh</td>
</tr>
</tbody>
</table>

TDP: Thermal Design Power

<table>
<thead>
<tr>
<th></th>
<th>Smartphone</th>
<th>iPad/GalaxyTab</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mobile AP</td>
<td>~2W</td>
<td>~3W</td>
</tr>
<tr>
<td>Battery (Wh)</td>
<td>~6Wh</td>
<td>~25Wh</td>
</tr>
</tbody>
</table>

* Tablet PC Battery Life Target: 7~10 hours

※ Source: www.wikipedia.org
Si Interposer

An electrical interconnection structure used between a silicon integrated circuit die and package, test jig, or other die that enables a reduced contact pad pitch on the Si interposer.

※ Source: Yole development, Aug 2010
2. Organic Interposer of 2.5D Packaging
2.5D Packaging

Looks multi-dies system module packaging, and the performance of module is count on the electrical interconnection quality between devices.

- Interposer should provide a good electrical, thermal-mechanical properties such as handling, low warpage, and so on.
- Interposer should provide cost competitiveness as well.

※ Source: www.amkor.com (2012)
### Si Interposer

<table>
<thead>
<tr>
<th>Feature</th>
<th>Spec</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSV Size</td>
<td>10 μm</td>
<td>Dia.</td>
</tr>
<tr>
<td>TSV Depth</td>
<td>100 μm</td>
<td></td>
</tr>
<tr>
<td>Metal 1</td>
<td>1 μm</td>
<td>L / S / T</td>
</tr>
<tr>
<td>Metal 2 &amp; 3</td>
<td>2 μm</td>
<td>L / S / T</td>
</tr>
<tr>
<td>Metal 4</td>
<td>4 μm</td>
<td>L / S / T</td>
</tr>
<tr>
<td>Metal to Metal</td>
<td>1~2 μm</td>
<td>Spacing</td>
</tr>
<tr>
<td>Via</td>
<td>1~2 μm</td>
<td>Dia.</td>
</tr>
</tbody>
</table>

### Example of Design Conversion

- **Organic Interposer Design**
  - 3+3 or 2+2+2 layer (6-layer),
  - Line & Space : 5/5um
  - Via/Pad : 30/50um, Pad pitch 40um
  - Si TSV 5,590 ea → TCV 1,128
Low CTE Core Materials are being developed with a low CTE and a high Tg with a high modulus.

Property Trends

Measured Data

- Inorganic option
  - 50nm Size Filler
  - High Tg Resin (240 → 270°C)
- G/C Upgrade (E-glass → T-glass)
- Organic Option
  - 10ppm/°C
  - 6ppm/°C
  - 4ppm/°C
  - 2ppm/°C
Symmetric structure and Various thickness of core could be used → Warpage controllable compared to silicon interposer

**Organic Interposer structure**

- Core
- TCV
- Metal layer
- Passivation layer

**Proto Sample (6L)**

- Core
- TCV
Electrical Performance Modeling

**Structure Comparison**

- **Silicon Interposer** *

- **Organic Interposer**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Silicon</th>
<th>Organic</th>
</tr>
</thead>
<tbody>
<tr>
<td>Via Diameter</td>
<td>10um</td>
<td>100um</td>
</tr>
<tr>
<td>Via Height</td>
<td>100um</td>
<td>220/300/450um</td>
</tr>
<tr>
<td>Via Wall Thickness</td>
<td>-</td>
<td>12um</td>
</tr>
<tr>
<td>Plugging Material</td>
<td>Cu-Fill Plating</td>
<td>Ink</td>
</tr>
</tbody>
</table>

**Modeling Result**

- **Via S-21 (Loss) dB**

- **Via Resistance, mOhm**

*Source: Qinghu Chin, Xin Sun, Yunhui Zhu, et.al "Design and Optimization of RDL on TSV interposer for High Freq. Applications", 2011 ICEPT–HDP*
New organic interposer provides bare IC to be attached directly with using a low CTE and high modulus core organic material.

<table>
<thead>
<tr>
<th>Si Interposer</th>
<th>Organic Interposer</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Wafer</strong></td>
<td><strong>Core Substrate Type</strong></td>
</tr>
<tr>
<td>Silicon (3ppm/K) 100µm</td>
<td>Core Material (CTE) Core Thickness</td>
</tr>
<tr>
<td>1µm</td>
<td>Line Width</td>
</tr>
<tr>
<td>Asymmetry (n+1)</td>
<td>Structure (Top+Bottom)</td>
</tr>
<tr>
<td>Dry Etch</td>
<td>Core Through Hole</td>
</tr>
<tr>
<td>PECVD + PVD+Cu Plating (Semiconductor Process)</td>
<td>Through Hole Filling</td>
</tr>
<tr>
<td>Wafer Thinning</td>
<td>Total Thickness Control</td>
</tr>
<tr>
<td>801ea/m² (12 inch)</td>
<td>Net Die (25 x 25mm²)</td>
</tr>
</tbody>
</table>
Process of Organic interposer

- Sputtering
- Coating
- Photo
- Develop
- Cure
- Plating
- Etching
- Sawing
Though Core Via Filling

Two Options are available for TCV filling of organic interposer
- Less than Aspect Ratio 1.5:1 → Cu fill plating
- Above than Aspect Ratio 1.5:1 → Ink or Cu Paste Plugging,

<table>
<thead>
<tr>
<th>AR 1:1</th>
<th>Cu Fill Plating (A/R 1.5:1 ↓)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core 0.1t</td>
<td></td>
</tr>
<tr>
<td>Via Φ0.1</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>AR 2:1</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Core 0.2t</td>
<td></td>
</tr>
<tr>
<td>Via Φ0.1</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>AR 3:1</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Core 0.3t</td>
<td></td>
</tr>
<tr>
<td>Via Φ0.1</td>
<td></td>
</tr>
</tbody>
</table>
Via interconnection

Laser Via Technology has a smaller Via Size limit. New technology is needed for the high dense interconnection.
Resolution Result

Define 5μm via open diameter (Taper angle 55°)
Fine Pattern  _  PR Development

PR Pattern for 4µm is available for the fine line & space 5µm on this feasibility test

Test Pattern (Side View)

- Line Width 3.7µm
- Space  6µm
- Thickness 14µm T

FIB Analysis

Proto Sample (Top View)

- Pt Treatment
- Cu/Ti seed
- Dielectric Layer
Line & Space 5μm is shown with wet etching method on this feasibility test:
Undercut less than 0.3μm also is acceptable.

Test Pattern (Side View)

- Line Width 4.9μm
- Space 4.7μm
- Thickness 7.6μm

Proto Sample (Top View)

- Plated Cu
- Cu/Ti seed
- Pt Treatment
- Dielectric Layer

FIB Analysis
3. Key Challenges
Key Challenge _ Metallization/Adhesion

Adhesion Promotion
DE → Cu seed
Cu → DE

Desmear (Wet & Dry)
Roughness variation
Via btm cleanliness

Via Integrity & Fine Patterning

Quick Etching
Improve Selectivity

Seed Metal
Thin e’less seed
Sputtered seed

※ DE : Dielectric Material
Key Challenge _ Fine Pattern L/S 3μm

- **As-Is**
  - Substrate
  - DFR Pattern
  - Cu Plating
  - Isotropic Chemical Etching

- **To-Be**
  - Substrate
  - DFR pattern
  - Cu Plating
  - Anisotropic Etching

**To-Be Benefits**
- Thin Seed layer (Minimizing metal etch)
- Non-Contact
- High Resolution
- Minimized contamination
- High etch uniformity
- Clean process
Feasibility Study  Fine Pattern L/S  5μm

Line & Space 5μm is available on this feasibility test
☞ DFR foot
☞ Strip residue
☞ Etching bias control

<table>
<thead>
<tr>
<th>5/5um</th>
<th>DFR Development</th>
<th>Cu Plating and DFR Strip</th>
<th>Seed Etching</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td><img src="image1" alt="Image" /></td>
<td><img src="image2" alt="Image" /></td>
<td><img src="image3" alt="Image" /></td>
</tr>
<tr>
<td>L/S</td>
<td>3.7/6.1</td>
<td>6.1/3.9</td>
<td>4.9/4.7</td>
</tr>
<tr>
<td>Thickness</td>
<td>14.1</td>
<td>7.8</td>
<td>7.6</td>
</tr>
<tr>
<td>Note</td>
<td>-</td>
<td>Fully Strip</td>
<td>Minimization of Undercut</td>
</tr>
</tbody>
</table>
Feasibility Study_ Fine Pattern L/S 3μm

Line & Space 3μm is shown on this feasibility test

Strip

Etching
**Key Challenge — Adhesion**

Reliability (Thermal Cycle, HAST) test result:
No observed any layer delaminated until HAST 192 hours

<table>
<thead>
<tr>
<th></th>
<th>Before Reliability</th>
<th>TC 500 cycle (-65°C/125°C)</th>
<th>HAST 192hr (130°C/85RH%)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Dielectric</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Organic Core</td>
<td><img src="image1" alt="Image" /></td>
<td><img src="image2" alt="Image" /></td>
<td><img src="image3" alt="Image" /></td>
</tr>
<tr>
<td><strong>Ti/Cu (φ30um)</strong></td>
<td><img src="image4" alt="Image" /></td>
<td><img src="image5" alt="Image" /></td>
<td><img src="image6" alt="Image" /></td>
</tr>
<tr>
<td><strong>Dielectric</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Organic Core</td>
<td><img src="image7" alt="Image" /></td>
<td><img src="image8" alt="Image" /></td>
<td><img src="image9" alt="Image" /></td>
</tr>
<tr>
<td><strong>Cu Foil</strong></td>
<td><img src="image10" alt="Image" /></td>
<td><img src="image11" alt="Image" /></td>
<td><img src="image12" alt="Image" /></td>
</tr>
</tbody>
</table>
Key Challenge _ Via integration quality

Reliability of Photo Via after TC 1500 cycle test result:

: Resistivity change ratio < 2%

< TC Via Resistivity Test (-65°C/150 °C) > [Unit : Ω]

<table>
<thead>
<tr>
<th>Cycle Via Dia</th>
<th>0</th>
<th>100</th>
<th>300</th>
<th>500</th>
<th>1000</th>
<th>1500</th>
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<tbody>
<tr>
<td>20</td>
<td>1.42</td>
<td>1.417</td>
<td>1.434</td>
<td>1.441</td>
<td>1.44</td>
<td>1.449</td>
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<tr>
<td>30</td>
<td>1.374</td>
<td>1.373</td>
<td>1.388</td>
<td>1.398</td>
<td>1.398</td>
<td>1.402</td>
</tr>
<tr>
<td>40</td>
<td>1.334</td>
<td>1.335</td>
<td>1.352</td>
<td>1.357</td>
<td>1.357</td>
<td>1.362</td>
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<tr>
<td>50</td>
<td>1.257</td>
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<td>1.272</td>
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<td>1.238</td>
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<td>1.198</td>
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<td>1.219</td>
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<td>1.159</td>
<td>1.173</td>
<td>1.177</td>
<td>1.173</td>
<td>1.182</td>
</tr>
</tbody>
</table>

Condition: Daisy Chain, Via 30EA, Line Width 30um, Pad Dia.= Via Dia.+30um
Key Challenge _ Solder on Pad

New Bumping method and alternative technology are needed as a low cost solution.

- **SP Printing**
- **BSP**
- **Metal post**

<table>
<thead>
<tr>
<th>Year</th>
<th>Bump Pitch (um)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2007</td>
<td>180</td>
</tr>
<tr>
<td>2008</td>
<td>150</td>
</tr>
<tr>
<td>2009</td>
<td>130</td>
</tr>
<tr>
<td>2010</td>
<td>110</td>
</tr>
<tr>
<td>2011</td>
<td>90</td>
</tr>
<tr>
<td>2012</td>
<td></td>
</tr>
<tr>
<td>2013</td>
<td></td>
</tr>
<tr>
<td>2014</td>
<td></td>
</tr>
<tr>
<td>2015</td>
<td></td>
</tr>
</tbody>
</table>

Advanced u-ball

N-SOP (Peripheral)

Cu Post
Key Challenge: Qualification/Interconnection

- **Qualification**
  - Silicon Device (Ultra Low K)
  - Organic Interposer

- **Interface**
  - Method

- **Material**

- **Equipment**

- **Process**

※ Source: PRISMARK, Dec 8 2011
Three kinds of Supply Chain could be available.
Which one is reasonable with considering the current SCM?

→ Issues: Simple, Stability of supply, Responsibility on quality etc.

**Model1: Foundry Plus**
- Semi Provider: Device, Interposer & Package Design
- Foundry: Device & Interposer Manufacturing
- PCB House: Substrate Manufacturing
- Assembly & Test: Wafer prep/bump, die prep, final assembly & test
- In House Test Option: Final Test option at Semi Provider

**Model2: OSAT Plus**
- Semi Provider: Device, Interposer & Package Design
- Foundry: Device & Interposer (TSV, BEOL only) Mfg
- PCB House: Substrate Manufacturing
- Assembly & Test: Bump, interposer BSF finish, die prep, final assembly & test
- In House Test Option: Final Test option at Semi Provider

**Model3: Third Party**
- Semi Provider: Device, Interposer & Package Design
- Foundry: Device Fabrication
- PCB House: Interposer Manufacturing
- PCB Supplier: Substrate Manufacturing
- Assembly & Test: Wafer prep, die prep, final assembly & test
- In House Test Option: Final Test option at Semi Provider

※ Source: ETRI, Technical Trends of Interposer for 2.5D integration (Feb, 2012)
Summary

[Environment and Issues]
- A packaging cost is increasing while IC performances are increasing
- Fine Pattern Technology for Wide I/O Memory is strongly needed
- Interconnection Gap between IC and PCB is increasing every year

[Solutions]
- 3D and 2.5D packaging could be alternative PKG solutions
  - In terms of thermal dissipation and cost, 3D packaging has a limitation
- A Si Interposer is still concerned in terms of Manufacturing Cost as well
- An Organic Interposer is needed as a low cost solution without changing the current supply chain
Thank you