Morphing the Semiconductor Outsourcing Business Model: Wafer Level Packaging

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Fundamental Shifts Driving the Industry

- Convergence
  - Applications
  - Manufacturing
- Proliferation of Specialized Applications
  - Internet of Things
- Big Data and the Cloud
  - Integrated data: Social, Business, and Government

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Fundamental Changes: Semiconductor Demand

- Electronic industry now more pervasive and is more affected by macro-economy
  - Electronic and semiconductor industries are maturing
  - End market electronic equipment sales are more than ever tied to individual consumer spending
- Diversification of electronic equipment drivers:
  - No single “killer app” or market, but need everything connected
- Value chain migration puts increasing value into both system and software
- Supply chain management model requires rapid response

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Implications for Semiconductor Manufacturing: Demand Side

- Time pressures: Must be profitable now!
  - Early entry into market requires higher price/margins
- Quick response to changing demand critical to overall profitability
  - Short lead times for equipment and materials
- Speed to implementation more critical
  - Time to market
  - Time to higher yields and lower costs
- New technology key to success
  - Higher performance/features must command better margins
- Shorter production-ready products times
  - Market pressures drive acceleration of Moore's law

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Fundamental Changes: Semiconductor Supply

- Long term revenue growth rate of Semiconductor Industry has slowed to single digits
  - Competitive advantages key to success
- Processed silicon is becoming specialized as outsourcing grows
  - Availability of advanced processes in the hands of a few
    - Foundries and SATS
    - Equipment manufacturers
- Manufacturing fades as competitive differentiator (Samsung, TSMC)
  - **Market value moving to IP: System/device design; software**
  - Outsourcing is on the rise
- Increasing concentration of manufacturing capacity in the hands of a few companies
  - Increasing risk as fab cost rise - 450mm, FinFET
- Foundry model separates design value from manufacturing value

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Implications for Semiconductor Manufacturing: Supply Side

- Time/Cost pressure on profitability increased
  - Speed up the yield curve
  - Improve cost reductions
- Tight process control required to achieve high yields of highest performing parts.
  - Design for Manufacturing
  - Design for Test
- New technology key to success – WLP, 3D/TSV
  - Smaller features
  - New materials
  - More complex structures and packages -- *smaller, lighter, faster, thinner* -- still continues on

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Net Effect on Industry Cycles

- Demand-side requires fast response to meet changing conditions
- Supply-side requires rapid response to changing conditions
  - Decreasing fab ramp times makes capacity available on shortened time scale
- Equipment industry speed of response is competitive advantage
  - Ability to respond quickly to provide rapid capacity increases
- Effect on business cycles:
  - Cycles still occur
  - Challenge is to be able to successfully manage your business within cycles

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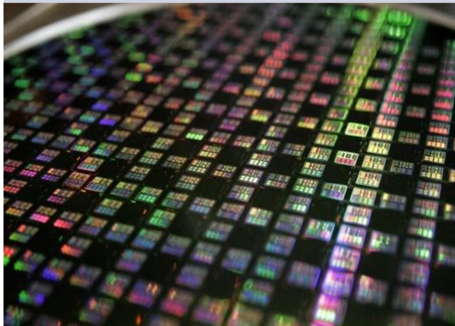
Semiconductor Manufacturing: Critical Uncertainties

Outsourcing Service Providers	Capital Equipment Vendors	Semiconductor Materials Vendors
• How to differentiate? • What new services? • To do 3D, or not? • To design, or not? • Where is my niche?	• Who will be my clients in 2017? • How fast do I need to invest in 450mm? • Which adjacent markets? • Merge with whom?	• Which client survives? • Which new technology? • Where is my ROI? • Merge with whom? • Exit semiconductors?



How to maintain and grow profits?

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Semiconductor Manufacturing: Increasing Costs Bring Fundamental Changes

1. Increasing R&D costs and Technology Challenges
   - New technologies needed to continue Moore’s Law through decade
   - Increasing R&D costs force collaboration
   - Increasing risks that needed technologies won’t be available in time forces search for expensive alternatives.
2. Increasing fab costs:
   - Reduces the number of semiconductor manufacturers who can afford to stay at the leading edge to a handful of companies
   - Increases fab size, reduces the number of fabs being built.
   - Increases pressure for cost reduction through 450mm initiative
3. Increasing design costs:
   - Makes the current pace of Moore's Law economically questionable for leading edge manufacturing except for the biggest vendors with highest volume parts.
   - Increases the need to find lower cost design and manufacturing solutions.

Key Question: Can the fundamental economics of the industry continue?

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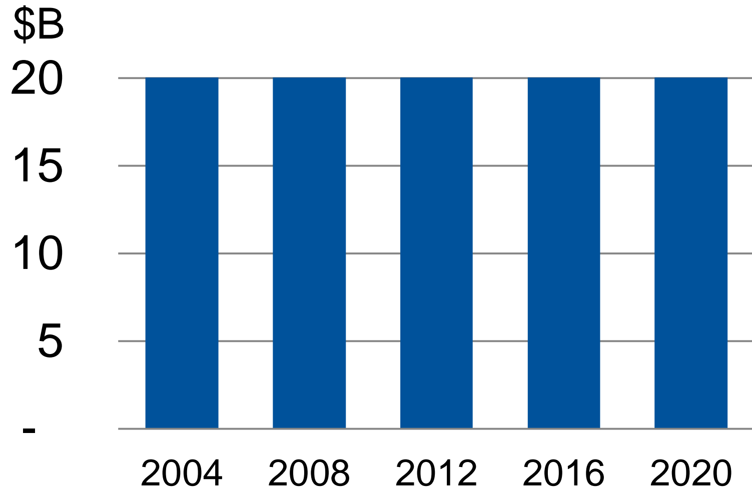
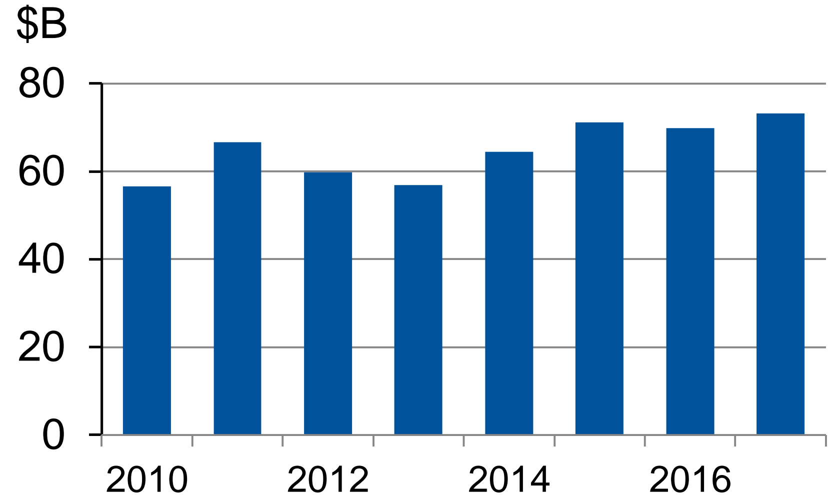
Semiconductor Manufacturing: Overall Situation and Key Trends

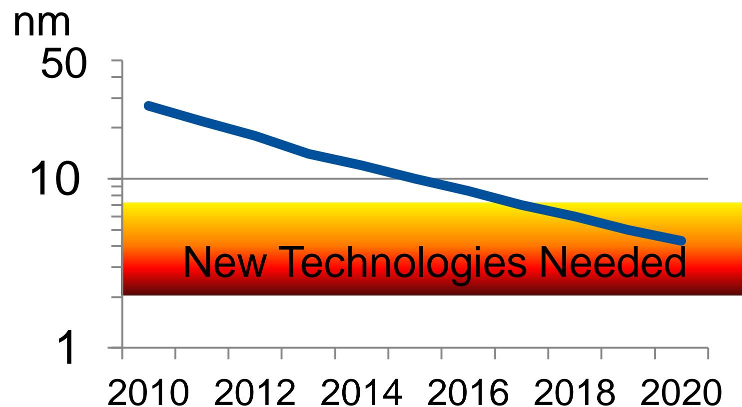
Fab Costs Surge…



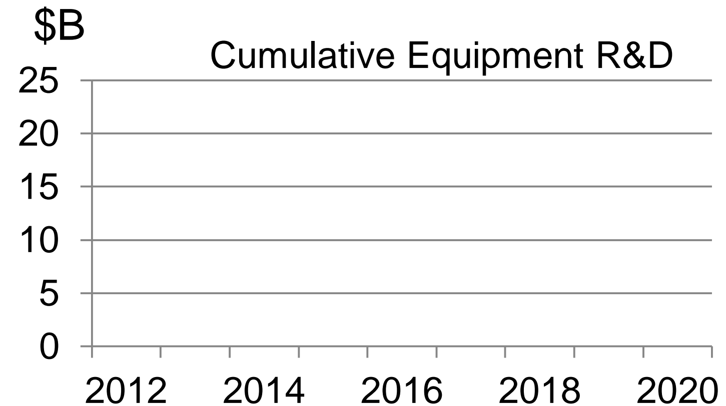
… While Capex Growth Slows



… Moore's Law drives mfg



… and 450mm R&D Breaks the Bank



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Semiconductor Business Models Must Adapt to the Changing Markets

- Greater reliance on R&D partnerships
- Multi-sourcing
- Consolidation of fabless and IDM companies
- Foundry manufacturing: more cost-competitive
- SATS manufacturing: supply chain value added vs. costs
- More design services from foundries and SATS
- Market segmentation
  - Leading-Edge
  - Mainstream
  - Trailing edge

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Semiconductor Manufacturing Models

- **IDM**
  - Large Internal Fab Capacity
  - Use Foundry/SATS as Capacity Buffer
- **Asset-Light IDM**
  - Internal Fabs for Technology Development and Early Production
  - Foundries and JV Fabs for Volume Production
  - Internal and SATS for Back-end Packaging/Test
- **Transition IDM**
  - Foundries are Primary Source of Production Capacity
  - May Employ JV Fabs for Capacity Assurance
  - Divesting Back-end to SATS
- **Fabless**
  - Rely on Foundries/SATS for All Production Needs

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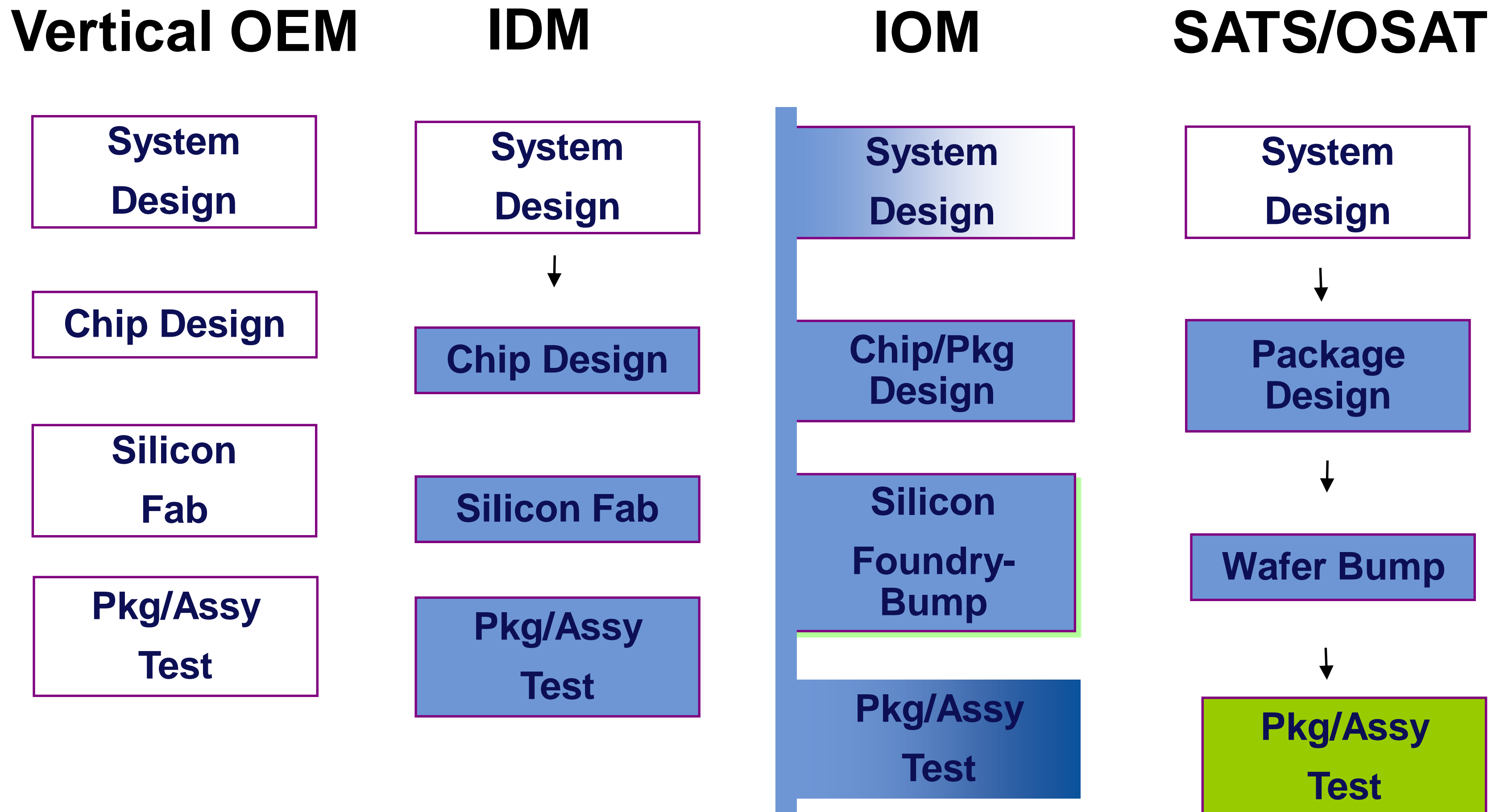
Wafer Level Packaging – Driving the Integrated Outsourcing Model (IOM)



Aligned Technology though collaboration, not ownership

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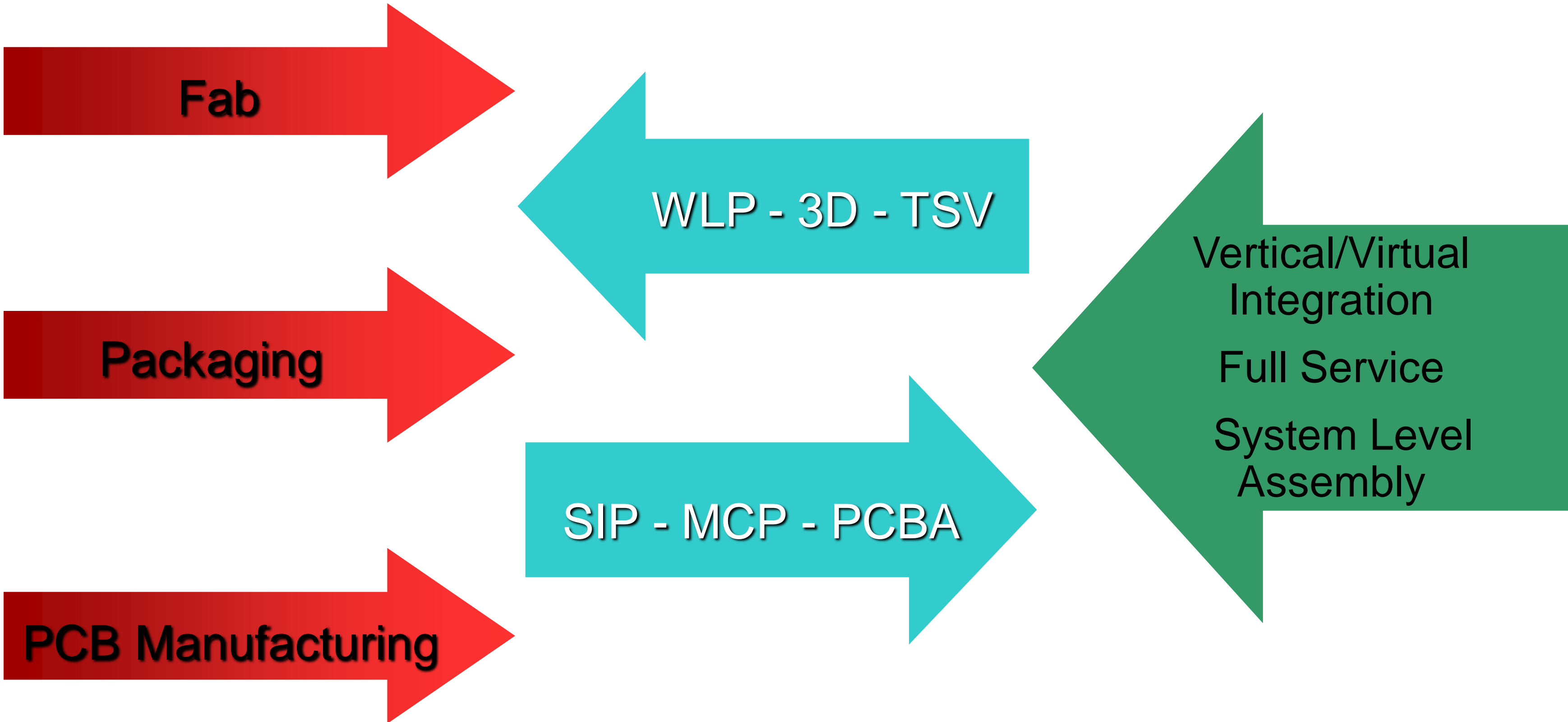
Wafer-Level Packaging: Driving the industry to the Convergence of Outsourcing



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Wafer-Level Packaging: Changing the Manufacturing Environment

- Change in IC design rules
  - True system-level design possible
- Supply chain restructured
  - Equipment and materials suppliers redefined
- Business relationships altered
  - "One-stop shopping"
- Improved logistics
  - Reduced cycle time
- More vertical, continuous process
  - Regional manufacturing

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Supply Chain Restructuring: Equipment Vendor Concerns

- Migration to flip chip, redistribution and WLP reduces need for wire bonders and traditional die-attach machines
- Changes in molding processes: eliminates traditional molds and encapsulation presses
- Absence of lead frame materials eliminates traditional trim, form, and dambar removal equipment
- Absence of traditional plating means no solder plating equipment

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Supply Chain Restructuring: Material Vendor Concerns

- Migration to flip chip eliminates die attach polymers, gold and aluminum wire
- Absence of traditional molding process eliminates epoxy molding compound
- Absence of lead frame substrate reduces usage of copper, AL-42, and solder

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… But New Opportunities for Equipment Growth

- Flip chip bonders (pick-and-place)
- Tape and reel machines
- Wafer thinning/backgrinding/bonding
- Material dispensing (adhesive, glob, underfill, solder jet)
- Wafer handling

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… But New Opportunities for Material Growth

- New solders to replace lead
- Underfills
- Conductive adhesives
- Coatings
- Substrates (PCB, flex, tape)
- Higher-temperature or thermoplastic polymers
- Wafer mask for bumping/coating

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…But Also New Opportunities for Outsourcing Growth

- Device Design with Package Integration
- System-on-Package (SOP)
- Flexible Electronics
- LED Manufacturing
- Solar
- IoT
- Cloud Computing and Storage
- SSD

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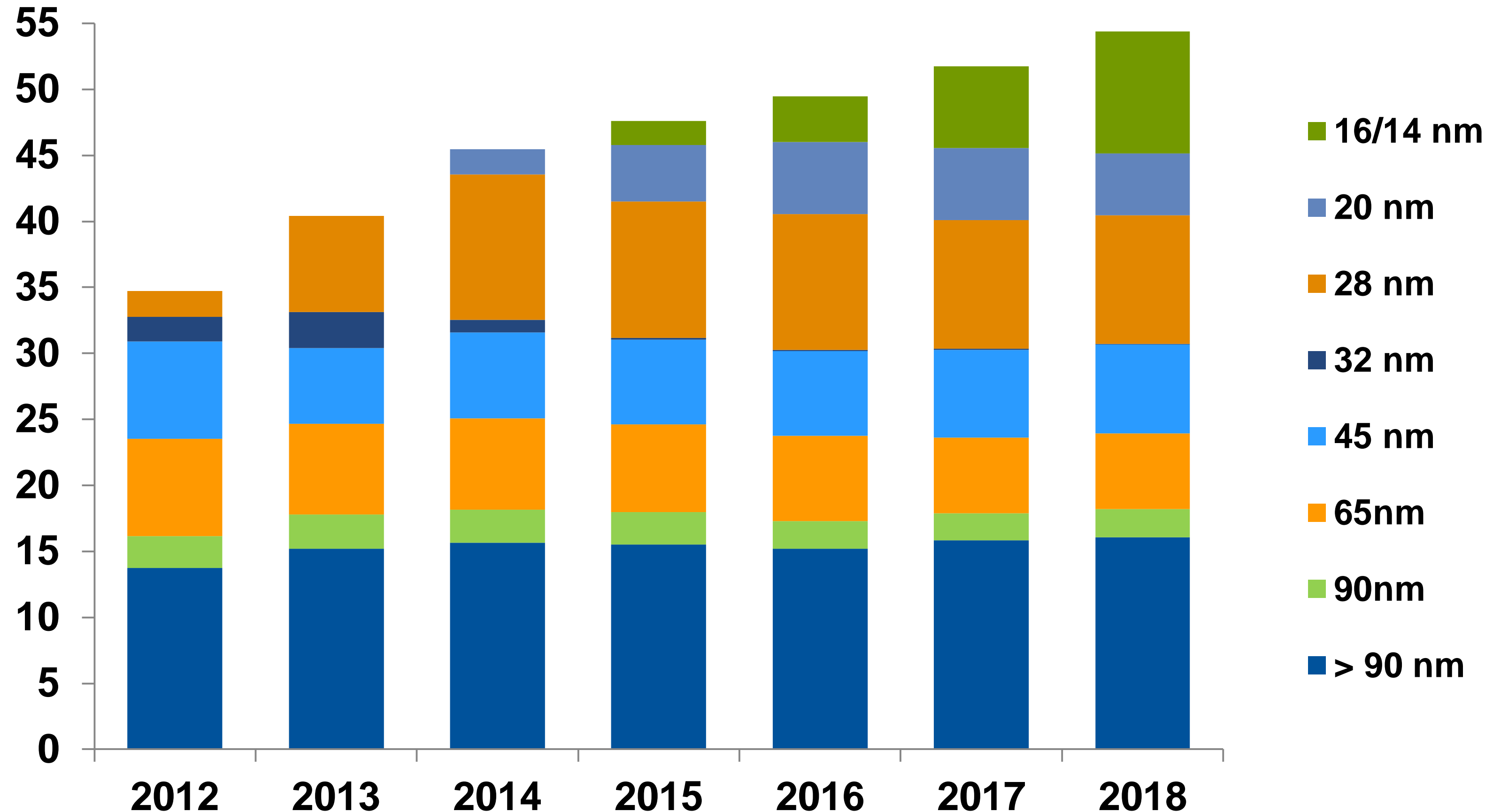
Rapid Migration to Smaller Wafer Nodes Increases Demand for Array Packaging



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WLP Package Forecast: 2013-2018

Wafer-Level Package Forecast, 2013-2018 (Millions of Units)							
Year	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**CAGR 2013-2018**
Units	16,342	19,870	22,675	25,915	31,149	36,400	17.4%
Source: Gartner (July 2014)							

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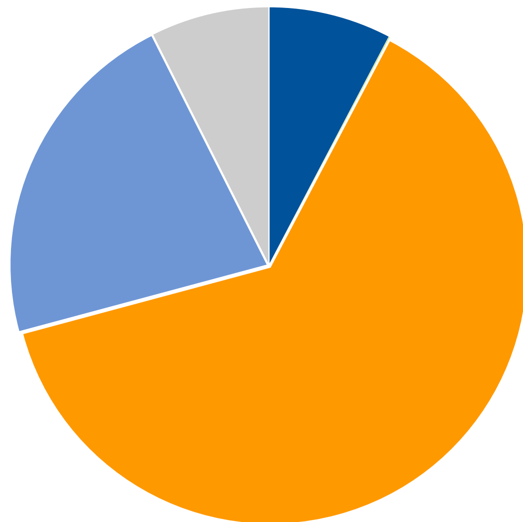
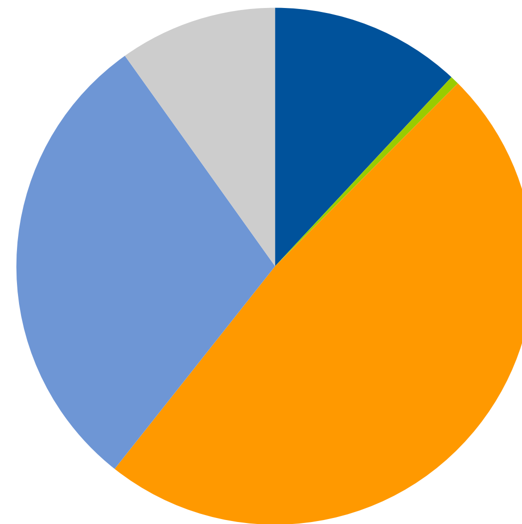
SATS Unit Demand by Package: Advanced Technology Drives Growth

2013



- WLP
- TSV
- Leadframe
- Laminate
- Flip Chip

2018



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The Big Challenge

- Can Foundry do Wafer Level Packaging Processes at 20 - 25% Margin?

or…..

- Will Customers pay the Foundry margin of 45 - 50% when SATS can do it for 20 - 25%?

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The Final Outcome for WLP/3D/TSV

- Optimization of performance, size and cost is system dependent. Maximize manufacturing integration.
- Vertical re-integration, but for Outsourcing Services
  - Solves the margin dilemma
  - Leading edge technologies are implemented
  - Manufacturing assets are maximized
  - Costs lowered

So………

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Summary

- Companies should re-consider the vertical integration model of semiconductor manufacturing to improve performance and reduce costs.
- As SoC manufacturing becomes increasingly difficult and costly, companies should consider packaging options for integration as this enables innovation more rapidly
- However, as mass customization grows, semiconductor companies still need to actively consider all wafer and packaging integration methods to harvest the speed and density benefits that will result.

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