2.5D, Silicon Interposers, Silicon Bridges, Glass Panels, Organic HDI

What is this all about?

By Phil Marcoux

Business Development Consultant

To ALLVIA, Inc.

Sunnyvale, CA

www.allvia.com
About ALLVIA, Inc.

• ALLVIA provides Through Via design and fabrication services.

• Silicon and Glass Interposer are offered..

• The Company was formed in 2004. ALLVIA is the former Tru-Si, Inc. creator of the Atmosphere Plasma Etching System for wafer thinning.

• ALLVIA offers:
  – Prototyping and low volume production in silicon or glass
  – Silicon Interposers with Capacitors
  – Visit www.allvia.com for more information
Acknowledgements

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• Calvin Cheung, ASE
• Javier De La Cruz, eSilicon
• Ed McBain, ALLVIA
Why are we stacking things?
Why are we stacking things?

Increase Density – System in Package, More memory, Size

Higher Performance – More Design Versatility, Thermal

Enhanced Reliability – Reliability Pyramid

Company Advancement - Improved time to Revenue

Lower Cost – Applicable to select applications

To enjoy assembly challenges – What ???
3D Technology Groundswell

Micron announced Hybrid Memory Cube utilizing 3D-IC TSV technology

Samsung released memory standard product using 3D-IC TSV technology

Xilinx presented Xirtex7 device that splits large FPGA into 4 smaller die with an interposer

Source: eSilicon
According to Phil Garrou - “Dr. Ho-Ming Tong, General Manager and CTO for ASE, who some say coined the term "2.5D" for the use of silicon or glass interposers with TSV, indicated that this technology “is ready to move to the next stage”

Tong notes that “2.5D IC should not be regarded as a transitional integration technology.”

According to Tong: “2.5D will enable packaging of chips in the 32-22 nm nodes where the fragile mechanical stability of the low-K dielectrics used in these products will require their bonding to an intermediate silicon interposer before final placement in a standard package”
A Reliability Pyramid - An Interposer Benefit

* Interposer CTE is a function of factors, such as the number and size of the vias.

Source: PPM Associates www.oneppm3D.com

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Today’s Potential Interposer Suppliers
Edited by PPM with JV Approval

- ALLVIA
- ASE
- Dai Nippon Printing (DNP)
- EPWorks
- Ibiden (R&D)
- IBM
- IMT
- IPDiA
- Samsung Electro-Mechanical (R&D)
- Shinko Electric (R&D)
- Silex Microsystems
- SPIF
- STATS ChipPAC
- TSMC
- WLCSP (Planning), China
## Ideal Properties of a Package Material

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Ideal Properties</th>
<th>Materials</th>
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<tbody>
<tr>
<td></td>
<td></td>
<td>Glass</td>
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<td>Silicon</td>
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<td></td>
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<td>Metal</td>
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<tr>
<td>Electrical</td>
<td>• High resistivity</td>
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<td></td>
<td>• Low loss</td>
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<tr>
<td>Physical</td>
<td>• Smooth surface finish</td>
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<tr>
<td></td>
<td>• Large area availability</td>
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<tr>
<td></td>
<td>• Ultra thin</td>
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<tr>
<td>Thermal</td>
<td>• High Conductivity</td>
<td></td>
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<tr>
<td></td>
<td>• CTE matched to Si</td>
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<tr>
<td>Mechanical</td>
<td>• High strength</td>
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<tr>
<td></td>
<td>• High modulus</td>
<td></td>
</tr>
<tr>
<td>Chemical</td>
<td>• Resistance to process chemicals</td>
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<tr>
<td>Processability</td>
<td>• Ease of Via formation and metallization</td>
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<tr>
<td>Cost</td>
<td>• Low cost per I/O at 25um pitch</td>
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Legend:  
- **Good**  
- **Fair**  
- **Poor**
Interposer VIA Types
The Type Affects Assembly.
Redistribution Layers (aka Traces)

Two Types

BEOL Metal – 2 to 3 layers with poly dielectric
FEOL Metal - 4 to 6 layers with CVD dielectric
Multiple Array Interconnect Methods

Flip chip bump pitch of 70 µm

2 Stacks of Up to 4 DRAM Dies

Chip TSV Pitch of 20 µm

Micro Bumps

Interposer

TSVs

Interposer TSV Pitch of 250 µm

Next Generation Complex 3D Package Architecture

BGA Balls

Package

BGA pitch of 0.5 mm

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Multiple Array Interconnect Methods

- Flip chip bump pitch of 70 µm
- Chip TSV Pitch of 20 µm
- Interposer TSV Pitch of 250 µm
- BGA Balls
- Package BGA pitch of 0.5 mm
- IC
- Micro Bumps
- FC Bumps
- BGA Substrate
- Module / Processor PCB

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Copper Pillars Instead of Solder Balls

Copper Pillar Process

1. Chip → Bump → Bonding Pad
2. Flip & Align
3. Dispense Solder Paste
4. Attach Reflow
5. Underfill Dispense & Cure

Radius = 3.5 miles
Flip Chip – Many, Many, Many, Many Options

- Attachment Process
  - Solder
  - TCB or TSB
  - Adhesive
- Die and Substrate pads
  - Metal type: Al, Au, Cu, solder
  - UBM required? For Au and solder yes.
  - Size – Related to bump configuration
- Bump/pillar metal
  - Au (stud or complete bump)
  - Solder
  - Copper
- Wafers or single die
  - Available die
  - ASIC
  - Pillars or bumps or stud bumps
Different Underfills are needed for reliability.

Currently one underfill type is adequate for reliability.
Conclusion

Interposers are becoming an essential element in the quest for stacking more electronics in a smaller area.

The infrastructure is rapidly growing to meet the needs.

Each design presents its own unique set of assembly issues.

The choice of interposer material, underfill composition, via design, and interconnect scheme have large impacts on cost and yields.

Users need to partner with a strong supply chain, especially since the chain is getting longer.