Power Management Using FPGA Architectural Features

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Agenda

• Introduction
  – Impact of Technology Node Adoption
  – Programmability & FPGA Expanding Application Space
  – Review of FPGA Power characteristics

• Areas for power consideration
  – Architecture Features, Silicon design & Fabrication – now and future
  – Power & Package choices
  – Software & Implementation of Features
  – The end-user choices & Enablers
    • Thermal Management – Enabling tools

• Summary
Technology Node Adoption in FPGA

• New Tech. node Adoption & level of integration:
  – Opportunities – at 90nm, 65nm and beyond. FPGAs at leading edge of node adoption.
    • More Programmable logic Arrays
    • Higher clock speeds capability and higher performance
    • Increased adoption of Embedded Blocks: Processors, SERDES, BRAMs, DCM, Xtreme DSP, Ethernet MAC etc
  – Impact – general and may not be unique to FPGA
    • Increased need to manage leakage current and static power
    • Heat flux (watts/cm²) trend is generally up and can be non-uniform.
    • Potentially higher dynamic power as transistor counts soar.

• Power Challenges -- Shared with Industry
  – Reliability limitation & lower operating temperatures
  – Performance & Cost Trade-offs
  – Lower thermal budgets
  – Battery Life expectancy challenges
FPGA-101: FPGA Terms

- **FPGA** – Field Programmable Gate Arrays
- **Configurable Logic Blocks** – used to implement a wide range of arbitrary digital functions.
- Programmable I/O Blocks
- Routing resources
- Switch matrix and interconnects/pass gates
- Configuration -- configuration memory & Configuration states

- Key FPGA attribute – regardless of what heterogeneous functions and elements are incorporated - is the ability to implement arbitrary digital logic circuit.
FPGA Attributes

• The upside – some unique attributes
  – Need more transistors to implement solutions – due to programmability overhead.
  – Die size is relatively large – power density is moderate.
  – More “standby” or “passive” resources – reduced power density
    • Menu of packages offered - with broad heat handling capability,
    • Software & programmability Opportunities to deal with power at the implementation level
  – Flexible and Optional Architectural features

• The challenge to Packaging
  – Flexibility means end-user power needs are largely unknown
  – Tailored thermal solution – no such luck
Market & Their Needs
Where FPGAs are used Today

• Markets:
  – Wired/wireless infrastructure equipment – base stations
  – Modular racks in storage/servers
  – Consumer & Automotive – Telematics & entertainment
  – Industrial & Mil/Aero – battle tanks, planes, radar etc

• Common requirement
  – Bigger, faster, cheaper!
  – Reduce the need for heatsinks or at least the cost of thermal solution
  – Lower power supply overhead & complexity

Revenue by End Market

- Communications: 45%
- Data Processing: 8%
- Consumer & Auto: 15%
- Industrial & Other: 32%
Power Density in Platform FPGA

<table>
<thead>
<tr>
<th>Block Type</th>
<th>Power density (normalized to CLB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DSP</td>
<td>0.78</td>
</tr>
<tr>
<td>CLB</td>
<td>1.00</td>
</tr>
<tr>
<td>PPC</td>
<td>1.32</td>
</tr>
<tr>
<td>IOB</td>
<td>2.33</td>
</tr>
<tr>
<td>BRAM</td>
<td></td>
</tr>
<tr>
<td>Dual Port</td>
<td>3.85</td>
</tr>
<tr>
<td>Single Port</td>
<td>1.93</td>
</tr>
<tr>
<td>MGT</td>
<td></td>
</tr>
<tr>
<td>Transceiver</td>
<td>7.75</td>
</tr>
<tr>
<td>Transmitter</td>
<td>4.22</td>
</tr>
<tr>
<td>Receiver</td>
<td>4.11</td>
</tr>
<tr>
<td>PMCD</td>
<td>11.4</td>
</tr>
<tr>
<td>DCM</td>
<td></td>
</tr>
<tr>
<td>High Freq</td>
<td>11.46</td>
</tr>
<tr>
<td>Low Freq</td>
<td>9.84</td>
</tr>
</tbody>
</table>

Power densities in 4VFX100
(Freq:500MHz)

- Density Uniformity no longer “a given”
- But the magnitude remains manageable – trade up density for efficiency

Source: Xilinx XPE data reported by Priya Sundararajan et al ICCAD ‘06
The Relative Magnitude of FPGA Power

- For high performance Offerings – FPGAs are in the 1 – 10 watts/cm²
- For small devices this is well below 1 watt/cm², and typically less than 0.5.
- Relative to Processors & Graphics Chips, FPGA power density is “lukewarm”, but can surprise some users
- Conventional Pkg Air cooling; Solutions already exist - Rsa
- How can we make this a non-issue?

<table>
<thead>
<tr>
<th>Components</th>
<th>Approx Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>2006/8 High End FPGA</td>
<td>10 – 30 Watts</td>
</tr>
<tr>
<td>INTEL Mobile – eg 2002 P4 or 2004 Pm</td>
<td></td>
</tr>
<tr>
<td>Transmetta 88 series</td>
<td></td>
</tr>
</tbody>
</table>

Today’s FPGA Power relative to early 2000 Mobile Processor Power
The 2 Power Components

1. Static:
   - Power from Transistor leakage or bias Current
   - The larger the device (>> transistors) the higher this component
   - Programmable transistors in FPGAs add to this power
   - It is not activity based, but increases with temperature
   - Gets worse with newer (leaky transistor) technologies.

2. Dynamic:
   - Activity based – similar to other ICs
   - Depends on switching frequency, Capacitance and Voltage levels
   - Improves with newer smaller nodes – for same design
   - Remains relatively flat with temperature
Power Consumption Breakdown

- FPGA Power Consumption is design dependent
- XC3S1000 at 100MHz, with 12.5% toggle rate, typical resource utilization.
- Breakdown shows areas in silicon & implementation that can yield good results
Focus

• Question:
  – How can we leverage the features of the FPGA architecture, the flexibility of FPGA (programmability & placement) to address Power Management challenges?

• Answer:
  – Some of the work and features are discussed - Balance of discussion
  – Focus areas grouped into 4 broad areas encompassing Architecture & Silicon, menu of packages, Design & Implementation software, and thermal management tools and models.
The Focus Areas
(Reduce Generation & Improve Removal)

- Architecture improvements in Silicon - design & fabrication
- The Package menu: FCBGA with consistent TIM for high powered products, down to small form factor (like QFN) for hand-held
- Software implementation of End-user design – Programmability, flexibility & smart design Options – like I/O choices etc
- Enabling the end-user to make their contributions
  - Thermal Management – Enabling tools
  - Thermal Models etc
Considerations - 1

The Silicon: Design & Implementation contribution to Heat generation

- Physical Design (Architecture Features, Circuits & Process)
- Package Choices
- Power Management
- ISE Software
- Power Optimization
- System-Level Design – Choices and Enabling Tools & Models

Addressing Low Power Design
Static Power Increases Dramatically with Temperature

$I_{CCINTQ}$ vs Junction Temperature

Normalized Leakage Current

Junction Temp °C
FPGA Power Components

- XC3S1000
Mixed-Oxide Technology

- Leakage current increases as channel length and gate oxide thickness decrease.
- Same oxide thickness is not needed in all the transistors.
- A low-leakage “Midox” transistor type is used to reduce leakage in configuration memory cells.
- Transistors with longer channel length and higher threshold are used throughout the FPGA to reduce static power.
- Eg. 130nm to 90nm can reduce static power by 50% at 100K gate level.
Dynamic Power Component

- Dynamic Power
  - \[ P = kCV^2f \]
  
  where
  - \( k \) = Nodes switching
  - \( C \) = Capacitance per node
  - \( V \) = Voltage switching
  - \( f \) = switching frequency or toggle rate

- Reduced Core dynamic power
  - Internal operating voltage is the dominant factor (1.5 => 1.2 => 1.0)
  - Secondary scaling by frequency and node capacitance
  - Dynamic power consumption is addressed with low capacitance circuits and custom blocks
  - Each successive node helps to reduce power – same gate count
  - I/O dynamic power – gain limited
  - Similar capacitance, voltage and frequency is required to support industry I/O standards
Hard IPs As Power Saving Feature

• Architecture Features
  – Larger logic blocks; smaller RAMs
  – Embedded hard-blocks give >10X power efficiency over soft-IPs

• Trades moderate power density for overall lower power
Why Hard-IPs help

• Reduced Static Power
  – No extra transistors as in programmable logic
  – No programmable interconnect transistors

• Reduced Dynamic Power
  – Lower switching Transistor count
  – Metal Interconnects vs. Metal and programmable interconnects ➔ low interconnect capacitance
  – Reduced trace lengths
  – No extra node capacitance because of lack of pass transistors
  – Minimized layers of logic
  – Non-optimized Placement issues eliminated

• Examples of Hard IP – see next slide for some IPs
  – 5 – 12x Reduction on power over FPGA fabric and FPGA programmable interconnects
Virtex Series Hard IP Examples

- 500 MHz Logic Array
- 500 MHz Differential Clocking
- 1 Gbps diff I/O with ChipSync™
- 500 MHz BRAM and FIFO
- 500 MHz XtremeDSP Slice
- 450 MHz PowerPC™ with APU
- 10/100/1000 Ethernet MAC
- 500 MHz PowerPC™ with APU
Insights - Low-Power Research

• Focus areas that are receiving attention but may not yet be in commercial implementations
  – Voltage Scaling: - 40 – 70%
    • Trade off performance with low Power for CLBs – Current Power sensitive CLB circuits need to be more robust
  – Fine Grain Power Switching: ~ 30%
    • Block level power switching
    • Controlling leakage in those passive elements that may not be participating in the circuit implementation
  – Deep Sleep Mode - during idle
    • Deep sleep with faster wake-up state than hibernation
    • Dynamically control fine-grain power switches to power down all block and maintain configuration state
  – Heterogeneous Fabric: Banks of fabric with different power rails – an idea.
Package Considerations

The Package implementation

Contribution to Thermal Management

- Physical Design (Architecture Features, Circuits & Process)
- Package Choices
  - Power Management
- ISE Software
  - Power Optimization
- System-Level Design – Choices and Enabling Tools & Models

Addressing Low Power Design
Spectrum of FPGA Packages

- Variety of packages to address Power & Market needs

- PBGAs (1.27 and 1.00 pitch)
  - Mid-Range / Mainstream
  - General Functions
  - Off-the-Shelf
  - User Friendly
  - Cost Effective

- PQFPs
  - PQ208/240 - Spartans
  - Miniaturization, Light Weight
  - Wireless Communication
  - Height Restriction
  - PCMGA, Portables
  - Low Cost and High Volume

- Tape Array CSPs (CP, FT SERIES)
  - High Power / Thermal Dissipation
  - High Performance Interconnect Enabler
  - High Speed Switching Systems
  - Advanced High-End Products

- FCBGA
  - Highest Power / Thermal Dissipation
  - High Density / IOs
  - High Performance / Frequency Design
  - Feature Crammed, High Speed Switching Systems

- Cavity Down BGAs
  - High Power / Thermal Dissipation
  - High Density / IOs
  - High Performance / Frequency Design
  - Feature Crammed, High Speed Switching Systems

- PGAs
  - Special & Market Specific
  - PROM, General Functions
  - High Reliability

- TSOPs

- CLCC

- FCBGA
Attributes - High End Packages

- FPGA’s traditionally have inherent lower Power Density
- Hot Spot has not been the issue; But beginning to change with IP
- Smooth Nickel finished Copper Lid Flipchip BGA are in use for all High power Devices
- The Focus is on TIM-1 interface - spreading heat with.
  - Thinner & Consistent BLT
  - Processing Repeatability
  - Long term stability – no pump out
- Packages that offer Low resistance theta-JC platform for heat sink applications
Improving Package Internal Spreading Capability

- Leveraging on board - In the telecom and Network environment FPGA products are used with over 18 layers of PCB – a source for heat spreading.
- Conscious improvement of heat-spreading through package to board can minimize size of heatsink.
- Up to 20% lower \( \theta_{JB} \) is possible to achieve – through:
  - Making use of over 4000 high density bumps; Improved ‘hot spot’ management
  - Increase vertical thermal conductivity through a denser and distributed via field in substrates
  - Copper density on each layer of substrate > 85%; to enhance internal conductivity
**Software & Implementation Considerations**

**ISE Tool Contribution to Total Thermal management**

**System Architecture Level Controls - Design & Placement Implementation**

- Physical Design (Architecture Features, Circuits & Process)
- Package Choices Power Management
- ISE Software Power Optimization
- System-Level Design – Choices and Enabling Tools & Models

**ISE**
System Architecture Level Controls

• Biggest Optimization “BanG” starts implementation strategy & the software to help manage it.

• This is where choices are made:
  – PlanAhead™ – Floor planning
  – Partitioning & Placement – thermal awareness
  – Possible modes of operation (hibernation etc)
  – Selection of features & IPs, and I/O standards
  – Performance vrs economy

• Lets review a couple of these …
FPGA Power Saving Features

- FPGA Implementation Optimization
  - Power-aware placement and routing:
    - Optimized for performance – time driven
    - Optimized for lower power – power driven
  - Early and detailed power analysis – for feedback to identify key sources of power
    - Xilinx Xpower – block level power estimation

• Your actual mileage will depend on the course you take and your driving habits
Optimizations for Power
Some Design Choices

• Feature selection, including power conservation features, impacts power – Needs to be present on silicon:
  – Suspend mode: Idle with state retention – when inactive
  – Hibernate mode: Idle w/o state retention
  – Back off on peak performance for lower power (voltage scaling)
  – Turn off unused portions (power gating)
• Dynamic Power varies linearly with frequency
  – Implement non-critical functions to run on a low speed clock rather than an arbitrary high speed clock in the design
• I/O standards Selection Options
• Choose Hard-IPs as part of implementation.
Considerations - 4

• Supporting the users in their System level Thermal management
  – On Chip System Monitors
  – Power estimations tools
  – Thermal models

- Physical Design (Architecture Features, Circuits & Process)
- Package Choices Power Management
- ISE Software Power Optimization
- System-Level Design – Choices and Enabling Tools & Models
System Monitor
Available on High Performance FPGAs

• Single-chip solution for monitoring supply voltages and temperature on FPGA
• Easy to use & self-contained for On Chip Temperature & Voltages
• Full access from FPGA fabric or JTAG TAP to System Monitor for handling alarms and feedback
• Fully operational prior to FPGA configuration and during device power down (access via JTAG TAP only)
• Auto chip power down if 125°C is detected on-chip – disabled by default
Pre & Post-Implementation Power Analysis

- XPower™ in ISE® software
  - Integration in Design Flow
  - Considers device data, along with the user's design files
  - Report estimated device power consumption at high level of accuracy customized to specific design
- Enables FPGA designers to perform detailed power analysis
- Tool extracts utilization from ISE and toggle rates from test vectors and simulation
- Output
  - Use the GUI or detailed report to see what is consuming the power
  - FPGA nets can be highlighted in XPower and shown in FPGA Editor
CTM for Thermal Budget Planning

- Accurate temperature prediction of FPGA components at the system level has become critical due to the shrinking thermal budget.
- Xilinx provides Compact Thermal Models (CTMs) for system thermal budget planning:
  - These behavioral models predict package temperature at the selected nodes (e.g., junction, case, and balls) – when integrated with other ICs.
  - CTM libraries are Downloadable from Xilinx.com for usage in conjunction with customers’ thermal simulation tools.
Summary of Key End-user Strategies & Choices

- Package Selection – provides basis for improvement
- Power Estimation & Optimization - Identify the power consuming blocks through look ahead software and optimizing
- Pay attention to Power Supply levels & Operating Temperature itself. The need to keep things “cool” is paramount.
- Implement some form of suspend or Hibernate mode.
- Make use of lower power I/O standards.
- Make use of Embedded blocks to implement design
- Clock generators – smart choices
- Take advantage of thermal management enablers

*Improvements in system and device reliability through significant power reduction techniques and package enhancements are still possible in FPGAs*
Thanks for your attention

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