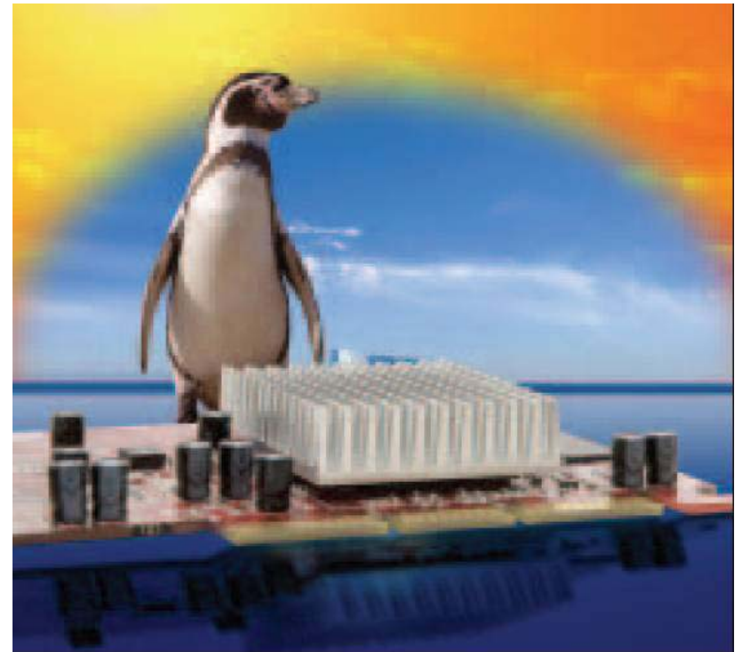
Thermal Interface Materials (TIMs) for IC Cooling



Percy Chinoy

ENGINEERING YOUR SUCCESS.

March 19, 2008

Outline

- Thermal Impedance
- Interfacial Contact Resistance
- Polymer TIM Product Platforms
- TIM Design
- TIM Trends
- Summary

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Thermal Management

- **Heat is a major problem in electronics equipment**
  - Limits performance (e.g. operating speed)
  - Reduces reliability (e.g. product lifetime)
  - Reduces efficiency (e.g. battery life)
  - Adds cost to the product

- **Thermal interface materials (TIMs) enable heat transfer from semiconductor device (die, package) to heat spreader (heat sink / heat pipe / chassis / housing)**
  - Design goal is to minimize thermal impedance and keep the device junction temperature below specified limits (typically 90–100°C)

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Thermal Pathway

Heat Sink

Ta (Ambient Temp ≈ 38–40°C)

TIM2

Integrated Heat Spreader

Tc (Case Temp ≈ 60–70°C)

TIM1

Silicon

Tj (Junction Temp ≈ 90–100°C)

BGA Substrate

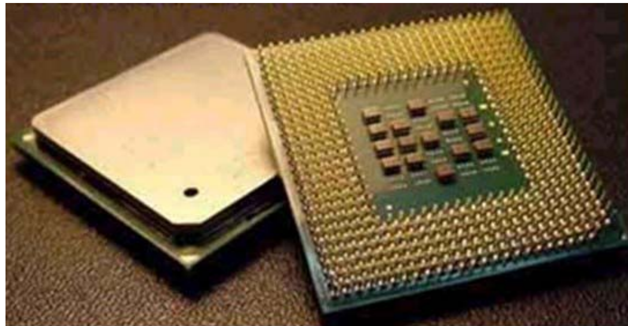
$\theta_{heat\ sink}$

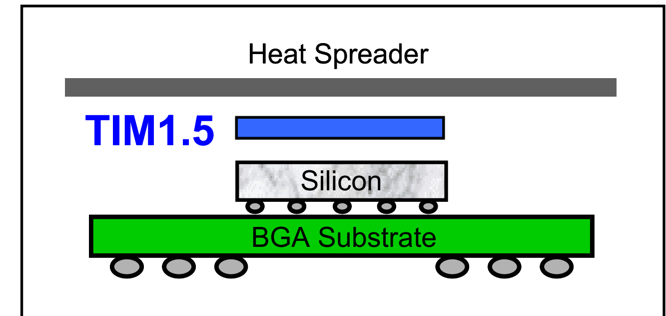
θ_{TIM2}

$\theta_{heat\ spreader}$

θ_{TIM1}

Thermal impedances





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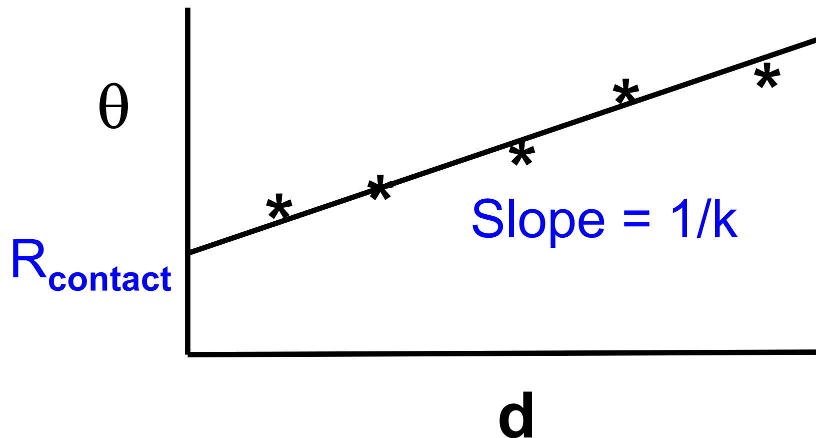
Think beyond thermal conductivity….
Thermal Impedance

$$\theta_{TIM} = R_{contact\ 1} + R_{TIM} + R_{contact\ 2}$$

$$R_{TIM} = d / k$$



d – bondline thickness (mm)

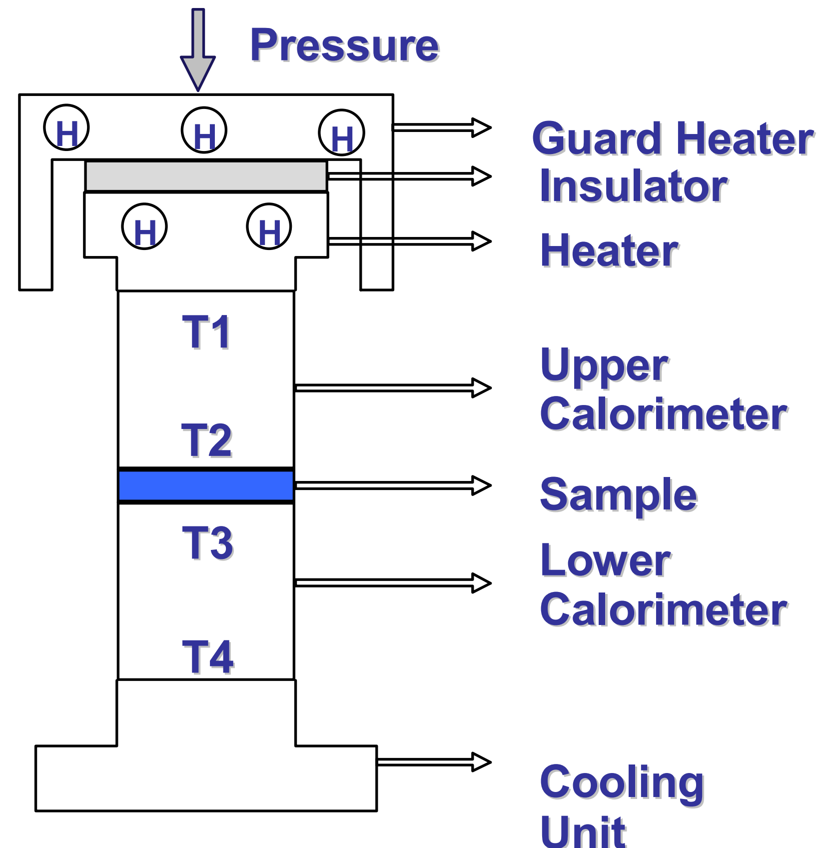
k – thermal conductivity (W/m-K)

θ – thermal impedance (°C-cm^2/W)

R – thermal resistance (°C-cm^2/W)

Measuring Thermal Impedance: ASTM D5470 Test Method

- ASTM D5470 is a convenient, standardized tool to measure and compare performance of TIMs
- Measured thermal impedance at a given pressure is determined by:
  - Bulk thermal conductivity, and
  - Bond line thickness (BLT), and
  - Contact resistance at the interfaces
- Limitations:
  - In-situ reliability measurements
  - Caution when comparing published test results from one tester to another, one lab to another …
  - … particularly for thin bond-line, very low impedance measurements
  - Caution when translating lab test results to real world applications



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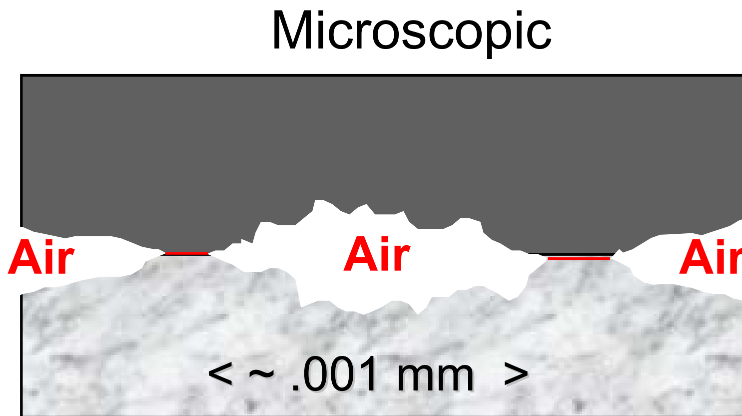
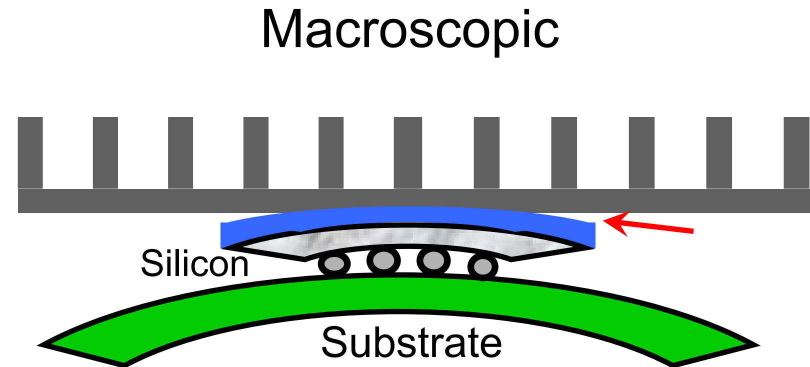
Interfacial Contact Resistance





- Contact resistance is primarily due to surface irregularities on a microscopic scale and out-of-flatness on a macroscopic scale, both of which cause air entrapment
- TIMs essentially replace air with a more thermally conductive material

k_{air}= 0.03 W/m-K **k_{TIM}= 1–5 W/m-K** **k_{Al}= 225 W/m-K**

- Require good surface wetting to aluminum, copper, plastic, silicon, …..

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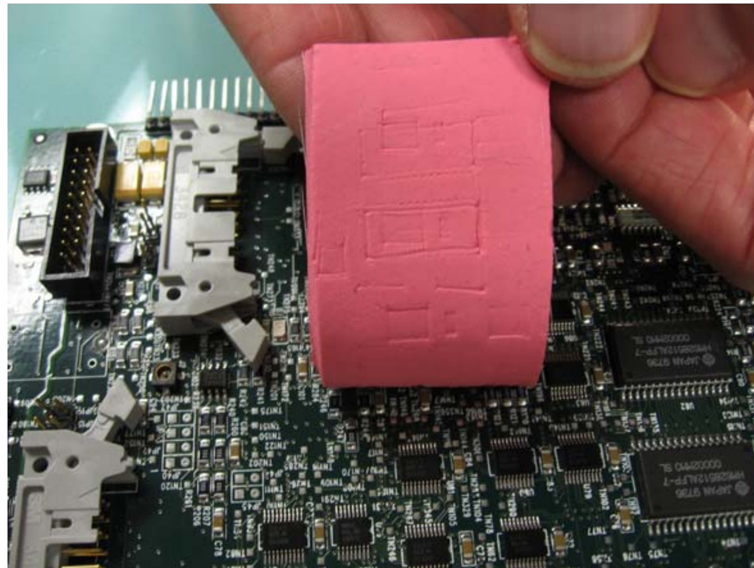
Interfacial Contact Resistance

- Decreasing silicon die thickness gives lower thermal impedance through the silicon but exacerbates die/package warping issues
- Watch out for flatness specs on low-cost heat sinks
- Softer TIMs conform better to surface irregularities and thus reduce $R_{contact}$ (and also reduce stress on the components)
- Higher pressures reduce $R_{contact}$ (and also reduce bond-line thickness)



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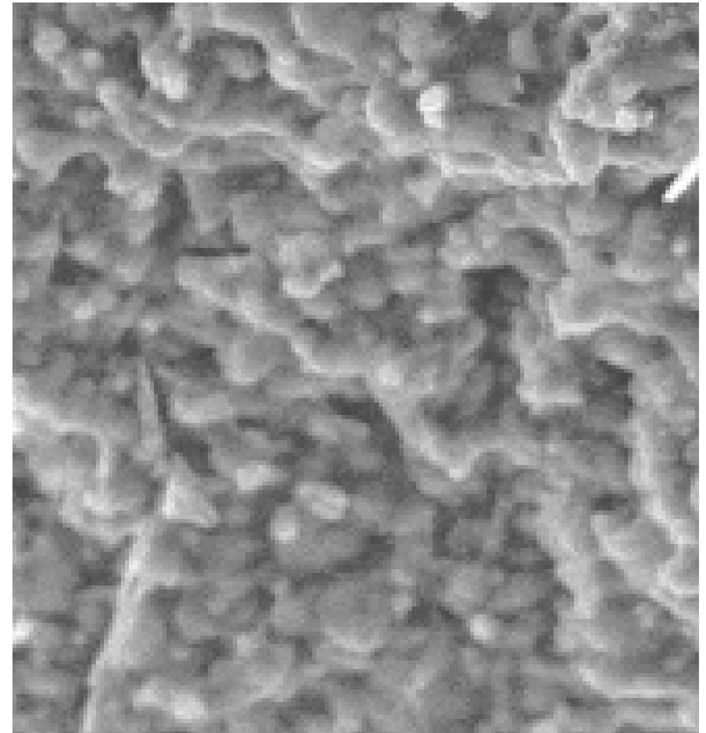
Polymer Thermal Interface Materials

- Thermally conducting fillers dispersed in resin binders

- Formulations optimized for:
  - Thermals, e.g. impedance
  - Bond-line, e.g. thin / thick
  - Mechanicals, e.g. compression
  - Electricals, e.g. isolation
  - Application process, e.g. stencil, pick-and-place
  - Manufacturing process, e.g. mixing, coating, lamination



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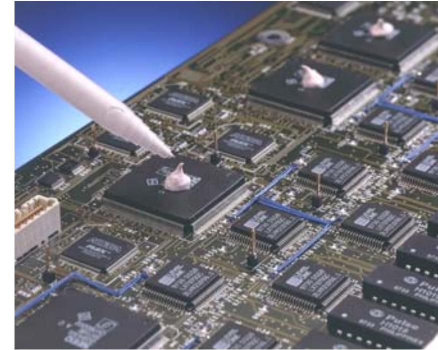
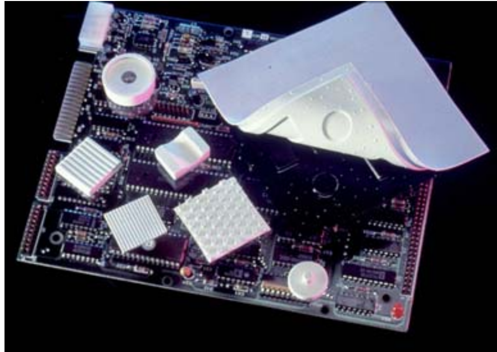
Polymer TIM Product Platforms

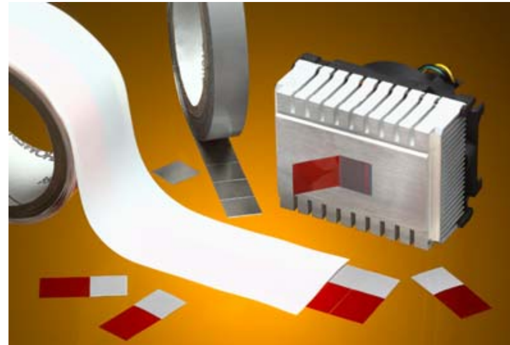
Thermal Grease



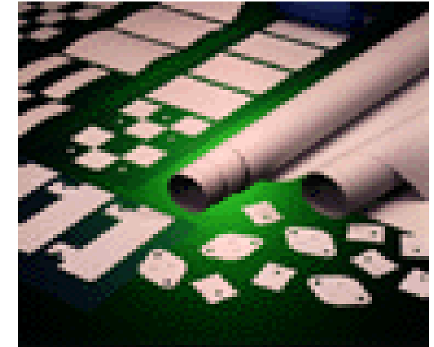
Thermal Gels



Gap Filler Pads



Phase Change



Electrically Insulating Pads

Compounds / Adhesives

Thermal Tapes

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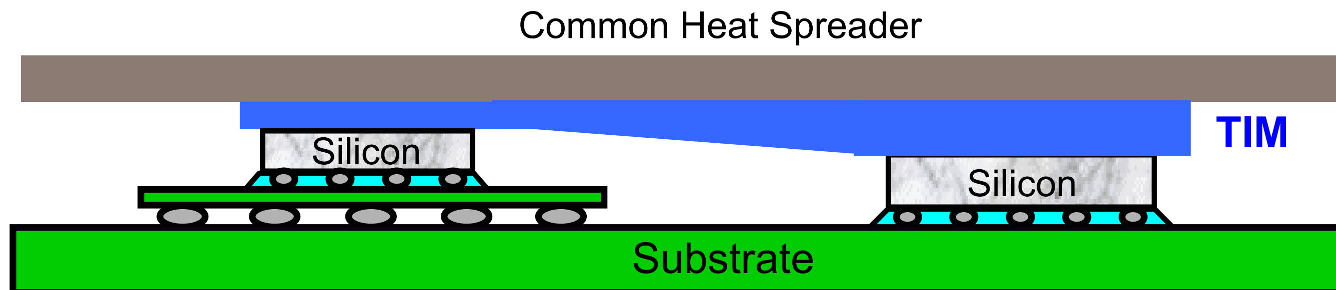
Design Variables for TIMs

Thermal, Physical, Electrical, Mechanical, Regulatory

- Power dissipation – Watts, Watts/cm^2
- Allowable temperatures – $T_{junction}$, T_{case}
- Size of chip, package

} Thermal Impedance specification

- Gap thickness between chip/package and heat spreader
  - Thin bond-line or thick bond-line TIMs
- Flatness tolerances (bow, warp, tilt) and co-planarity of chips/packages and heat spreader



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Design Variables for TIMs

- Contact pressure
  - Impacts bond-line thickness and contact resistance
- Electrical isolation requirement – Volts/mm
- Attachment of heat spreader with mechanical fastener (screw, clip) or TIM – adhesion strength requirements
- Application process
- UL rating
- ROHS compliance
- Out-gassing requirements – TML
- Re-workability
- Storage, shelf-life
- Others ……..

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TIM Applications

Applications / TIMs	Micro Processor 10 - 100+ Watts	Graphics Processor 5 - 100+ Watts	Memory <15 Watts	ASICs <10 Watts (most)	Chipsets 5 - 20 Watts	Power Discretes 10 - 100+ Watts	Power Modules 10 - 100+ Watts
Gap-Fillers	■	■	■	■	■		
Phase-Change	■	■	■		■	■	■
Grease / Gel	■	■	■		■	■	■
Dispensable Compounds			■	■	■	■	■
Tapes			■	■	■		
Insulator Pads						■	■

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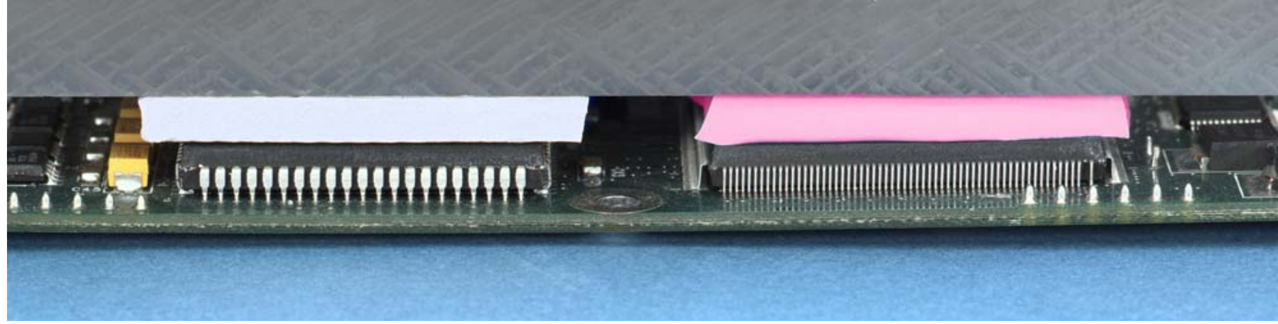
Soft is good



A579 Gap Filler Pad

Deflection vs Load - A579 @ 0.05 in/min

Load (psi)

120
100
80
60
40
20
0

0 5 10 15 20 25 30 35 40 45 50 55 60

Deflection (%)

Actual sample height given in [inches]

Tested 0.5" diameter disc with 1" x 1" probe

Initial [0.290"]
Aged 1000 hrs @ 125C [0.276"]
Aged 1000 hrs @ 200C [0.291"]

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Look beyond time=0 performance

T777 Phase Change Material

Thermal Impedance (°C cm²/W)

0.350
0.300
0.250
0.200
0.150
0.100
0.050
0.000

0
500
1000
1500
2000
2500

Aging Time (Hours)

Grease

T777

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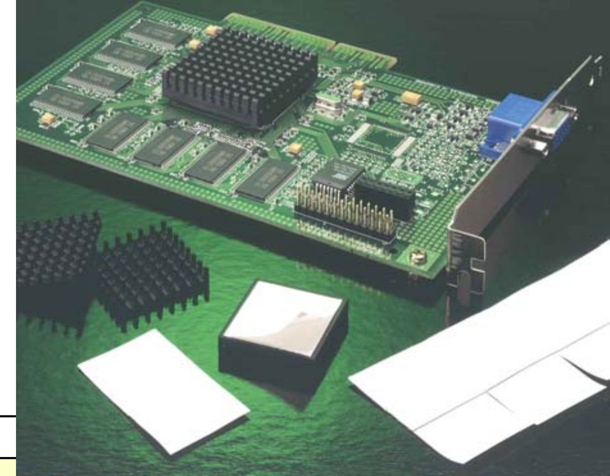
Proven Reliability



T418 Thermal Tape

85°C
100°C
125°C

Lap Shear Strength (psi)

400
350
300
250
200
150
100
50
0

Initial
1 week
6 weeks

Aging Time at Different Temperarures

Microprocessor Power Trends

- Transistor density continues to double every 24 months
  - 65nm in 2005 → 45nm in 2007 → 32nm in 2009
- Clock frequency continues to increase (>3GHz) for high-speed performance, but ….
  - … running into power consumption and heat dissipation limitations
- Thermal challenges dominate microprocessor design and architecture
  - Performance per Watt is key design parameter
- ITRS and iNEMI roadmaps show continuing increase in power for high-end microprocessors
  - >160W for servers/netcom, >100W for desktop, >40W for mobile
- Rapid migration of multi-core processors may slow the trend of increasing *average/max* power, but …
  - *Hot spots* are a growing challenge, power density $\geq$ 200 Watts/cm^2

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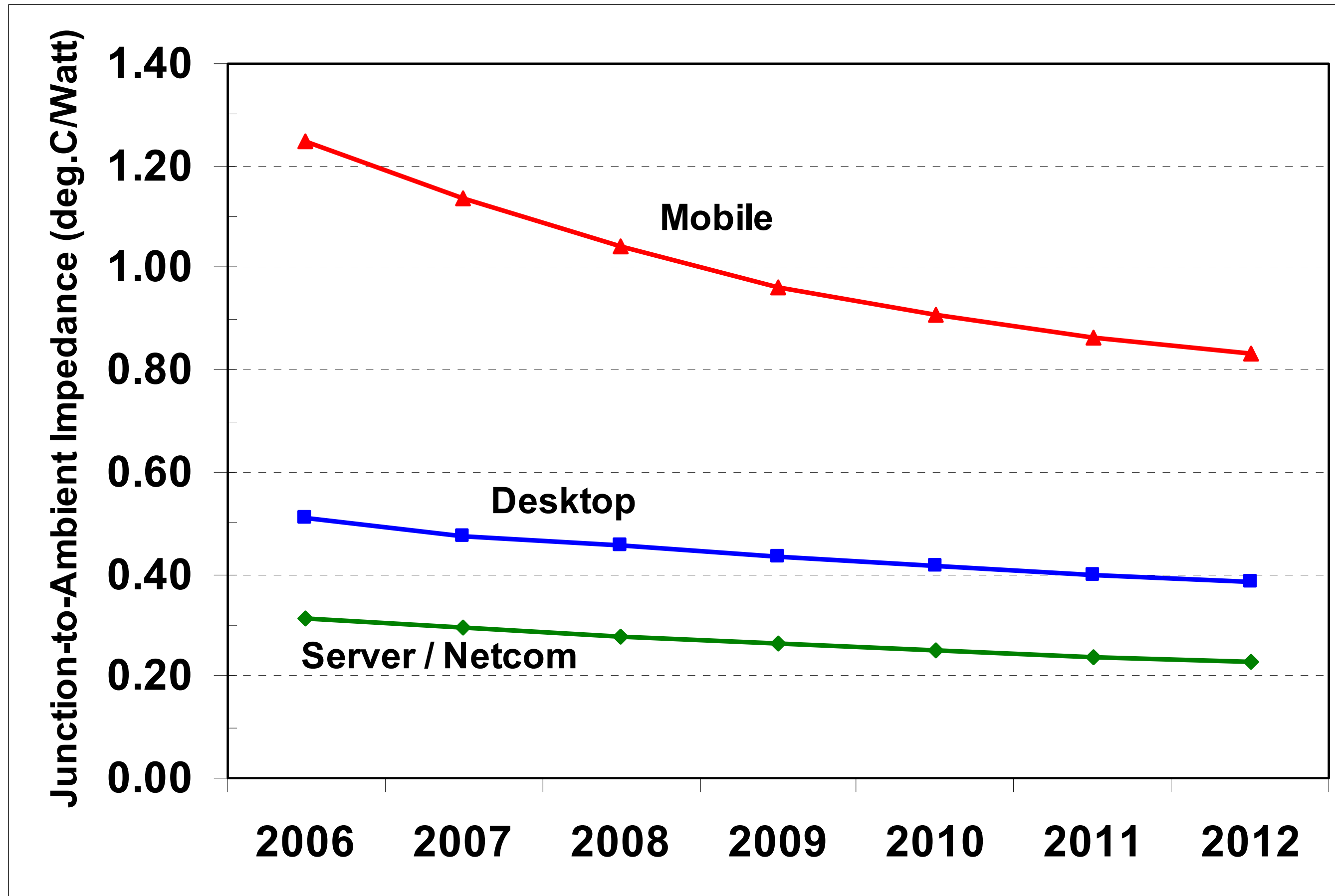
Thermal Impedance Trends
(estimated from ITRS, iNEMI roadmaps)



$$\theta_{TIM} = 0.1 – 0.2\ °C/W$$

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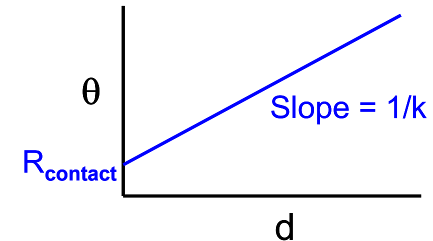
TIM Trends



- Low thermal impedance
  - High thermal conductivity
  - Thin bond line
  - Low contact resistance – softness / compliance, surface wetting
- High reliability
  - End-of-Life performance – TIM degradation over time
  - Cross-link density – Gels
- Low cost
  - Total cost of ownership
- Adhesion strength
  - High adhesion strength for tapes, adhesives
  - Low adhesion strength on some surfaces for ease of rework
- Automated Application Process
  - Dispense, pick-and-place
- Custom Integrated Assemblies
  - Thermal + EMI shielding/RF absorbing solutions

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Summary

- Thermal challenges dominate chip and package design
- Increased power density and reliability are driving innovation in TIMs
- Thermal impedance is the key metric of TIM performance, not just at time=0 but at end-of-life
- Decisions on TIM selection should not be based just on piece-part cost but rather total cost of ownership
- Collaboration of TIM manufacturers with designers at OEMs, ODMs, CEMs is essential to ensure steady stream of new TIMs that meet tomorrow's IC cooling needs

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