Efficient Thermal Management Using Advanced Semiconductor Packaging Techniques

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Thermal Management Issues in Semiconductor Packaging

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Overview

• Synopsis of issues facing power delivery systems
  – Focus is primarily on CPU power delivery (VRM’s)
  – How do we dissipate more power?

• Advanced Semiconductor Packaging
  – Discrete Solutions
  – Integrated Solutions

• Die on Leadframe Technology

• Conclusions
Background

- Processors have been consistently tracking and possibly outpacing Moore’s law
- As a result, CPU power consumption has been increasing at an alarming rate

Powering Moore’s Law

- To meet these demands the CPU roadmap requires the VRM to supply
  - Increasing current
  - Decreasing voltage
- Helps the CPU manage power dissipation, however places significant demands on power supply
Effects on the VRM

- As the Output Current Increases → Efficiency Decreases → Increased Ploss
- Helps the CPU, however places significant demands on power supply.
  - In effect it, moves the problem
- “How do we dissipate more power?”
1U VRM

- Standard power delivery form factor for CPU applications
- As CPU power demands increase, higher power VRM’s can be “Plugged in”
1U Dissipation Trending

- Power dissipation increases by > 2X
- Form factor remains constant
- How do we dissipate 2X power in the same form factor?
Traditional Solutions for VRM Applications

- Single path through PCB
Thermal Resistance Analysis

- Traditional (single path) SO-8 solution
- Overall thermal resistance $\theta_{j-A} \sim 28 \, ^\circ\text{C/W}$
- Predominate thermal resistance (71%) is $\theta_{j-\text{PCB}}$
  - Due to SO-8
Thermal Resistance Analysis

- New QFN solution
- Overall thermal resistance is 14 °C/W, down from 28 °C/W
- Now only 7% is $\theta_{j-PCB}$, down from 71%
- Limiting factor is now $\theta_{PCB-A}$
How To Dissipate More Power?

- Two options
  - Heatsink the PCB
  - Heatsink the case (Top Side) of the device
- Similar costs, but which is more effective?
- With QFN, the best option may be to heatsink the PCB due to high $\theta_{j-c}$
- Is there another option?

![QFN Top vs PCB Cooling Comparison](chart.png)
The Optimum Solution

- Maintain the low $\theta_{j-\text{PCB-A}}$ path
- Add a new, parallel path through the top with similar efficiency
  - in effect reducing $\theta_{j-A}$ by 50%
- Requires package with $\theta_{j-\text{case}} \sim 2 \, ^\circ\text{C/W}$
- Maintain package $\theta_{j-\text{PCB}} \sim 2 \, ^\circ\text{C/W}$
Two Efficient Heat Transfer Paths

Sink

TIM

Advanced Package

Power Input

PCB

TIM

Case

Junction

R_{sink-Ambient}=X \text{ C/W}

R_{Case-Sink}=X \text{ C/W}

R_{j-CASE}=X \text{ C/W}

R_{j-PCB}=X \text{ C/W}

R_{PCB-Ambient}=X \text{ C/W}

T_{Ambient}

T_{Ambient}
Advanced Semiconductor Packaging Techniques

• How to dissipate more power with
  – Discrete Solutions
  – Integrated Solutions
Discrete Packaging

- First order cooling limitations are based on the FET package and associated thermal resistances
- Power densities and delta T’s are high - this is the first place to solve thermal issues!
- Starting with a more efficient package in the beginning can alleviate many issues in the back end of the design

QFN

- \( R_{th(j-c)}: 14^\circ C/W \)
- \( R_{th(j-b)}: 1^\circ C/W \)

DirectFET™

- \( R_{th(j-c)}: 2^\circ C/W \)
- \( R_{th(j-b)}: 1^\circ C/W \)
Advanced Discrete Package
Package Comparison

- Comparison of package $\theta_{j-c}$
- Significant differences $\rightarrow$ significant effects
Effect on VRM

If DirectFET is used compared to QFN, 40% more power can be dissipated - or the same power can be dissipated with a smaller fan (400→200 LFM)

If DirectFET is used compared to SO-8, 2X the power can be dissipated! - or the same power can be dissipated and the fan can be eliminated! (600→0 LFM)
Integrated Solutions
Integrated Solutions
(Synchronous Buck Converter)

Features

- 4 Layer BT Substrate
- Si FET’s
- Si ASIC Driver
- Passives
- Au Wire Bonding
- Eutectic Pb/Sn Solder Ball-Grid Array
- Plastic Mold-Cap (PBGA)
T-PAC Concept
Land-FET
(DirectFET w/ no can)

T-PAC Concept
T-PAC Photos

Top View

Profile View
Architecture Comparison

Traditional Architecture

- Primary thermal paths are Vin & Vout under Q2 (SwNode)

(T-PAC) Architecture

+ Heat is distributed over large area of substrate (lower thermal resistance to motherboard)
+ Significantly improved heat transfer through case (lower thermal resistance to heatsink)
More than 87 % reduction in $R\theta_{j-c}$!
T-PAC Testing

4-phase Board without Fin

4-phase Board with Fin

Both Boards Tested in Wind Tunnel @ 400 LFM and 45 C
T-PAC Impact

400 LFM, Ta=45°C, 1 MHz

T-PAC Enabled
+22 A/Phase
+9 W Pd
Die On Leadframe
**Technology Comparison**

**Direct Bonded Copper Substrate**

Identical power module designed with DBC Substrate

**Die on Leadframe**

**ELECTRICAL**

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<th>mOHMs (avg)</th>
<th>Loop Resist</th>
<th>mOHM (avg)</th>
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<td>B+ to GND</td>
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**THERMAL**

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- Applications include motor drives, converters, etc
- Lower cost with improved electrical & thermal performance
- IR patented process

Rth_{MAX} = 1.15 C°/W

Rth_{MAX} = 0.95 C°/W
DOL Power Module Example

- FULL THREE PHASE INVERTER
- + TEMPERATURE SENSE
- + CURRENT SENSE (no wirebonds)
- + HIGH FREQUENCY EMI CAPACITOR
Die On Leadframe Benefits

• Fewer Manufacturing Process Steps than DBC
  – Lower Cost

• Low Inductance and Electrical Resistance:
  – Better motor performance and behavior
  – Lower junction temperature, or allows smaller die size

• Low Thermal Resistance:
  – Lower junction temperature, or allows smaller die size
  – Improved Reliability

• High Current Handling Capabilities
Conclusions

- Advanced semiconductor packaging techniques are required to increase power dissipation capabilities of VRM’s
- Efficient dual path cooling is required
- An effective discrete packaging solution has been developed
  - Enables 40% more dissipation compared to QFN
  - Enables 2X more dissipation than SO-8
- An effective integrated packaging solution has been developed
  - Enables nearly 3X more power dissipation than traditional PBGA’s
- A novel “Die on Leadframe” concept has been developed
  - Enables improved thermal & electrical resistance with lower costs
Questions?