New Techniques for Chip and Package Thermal Modeling
Agenda

• Industry Trends
• Package Thermal Modeling Standards
  – JEDEC Roadmap
  – Compact Thermal Models
    – 2-Resistor
    – DELPHI
• Chip Thermal Modeling Tools and Techniques
• Summary, Questions and Answers
Industry Drivers

- **Moore’s Law**
  
  - In 1965, Gordon Moore observed an exponential growth in the number of transistors per integrated circuit and predicted that this trend would continue.
Industry Drivers

• Combined effect is an increase in (max) chip power…
Trends in Thermal Design

Thermal solution innovation is moving downscale

- Thermal design moves downscale as chip power increases
- Co-design between levels and design data exchange are critical
- New standards and tools are needed to improve co-design, data exchange and detailed chip-package thermal analysis
Co-Design and Data Exchange Standards

- FLOHERTHERM
- Icepak
- Coolit

- FLO/PCB
- Iceboard
- TASPCB
- BetaSoft

- Flopack
- Icechip
- PTD

CTM standards for in-application junction temperature prediction
Progression of Compact Thermal Modeling (CTM) Standards

Theta j-a
Package to package comparison

2 resistor
Coarse junction temperature prediction

DELPHI
“Accurate” junction temperature prediction

Case Study: 25 W PCI board

• Charter
  – To generate thermal measurement and modeling standards for microelectronic packaging
  – These standards shall be meaningful, consistent, and shall be proven to be scientifically sound
  – The standards will provide a common means of comparison of thermal phenomena for users of microelectronic packaging
All standards are available for downloading free of charge from www.jedec.org
Thermal Modeling Standards and Guidelines

Overview

General
- Terms and Definitions
- File Interchange Format

Modeling Process
- Detailed Model
- Compact Model Overview
  - 2R CTM
  - DELPHI CTM
  - FUTURE METHODS
  - BCI & BCA Index Generation
  - BCI & BCA Index Application Guide

Validation Process and Reporting
- Validation Process
  - Detailed Model
  - Compact Model
- Validation Report
- Model Error Analysis

Experimental Validation Method
- Double Cold Plate
- JEDEC Metrics
- Modified Ring Cold Plate

Goals for Thermal Modeling Standardization

- Generate standards governing thermal model generation, documentation, data exchange, and validation
- Promote more efficient division of labor between component suppliers and system integrators
- Complement test-based standards
- Multi-parameter
- Boundary condition independence (i.e. satisfy appropriate level of Boundary Condition Independence or BCI) with numerically efficient predictive capabilities
- Capable of insertion into standard computational codes for system-level analysis
- Fully documented and non-proprietary
CTM Summary

- Chip level thermal design margins shrink with miniaturization and increasing performance
- New package modeling standards are needed
  - To bridge the gap between semiconductor and systems manufacturers and minimize the cost of data exchange
  - For reliable, accurate, in-application junction temperature prediction
  - To control proprietary information
- But what about the chip…?
New Techniques for Chip and Package Thermal Modeling

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MEPTEC, 3rd Annual “The Heat is On”, February 2007
Thermal Management in Microelectronics: Challenges and Innovations
Die-level thermal modeling

Geometry associated power map

Area averaged power map

Uniform power map

IF Subsystem
BPF
PLL/VCO
Control Logic
TX Subsystem and PA
Front End
Power Sources
Fine-grain IC temperature simulation

Coarse-grain

Fine-grain
Die-level thermal modeling

- Power modeling
- Design layout
- Package modeling
- Thermal techfile
- Thermal modeling
- Functionality modeling
- Timing modeling
- Reliability modeling

Die stack-up
Data needed to run FireBolt

- Chip layout is used to model the heat transport within the chip
  - e.g. LEF/DEF (or GDS2 if needed)
- Average power per circuit element from power analysis tools
  - e.g. Cadence Encounter Platform; Synopsys PrimeTime-PX
- Package $\Theta_{JA}$ (for each surface, or lumped)
- Thermal techfile – layer thicknesses (die stack-up) and material properties

De facto standard
EDA tool specific
JEDEC standard
Gradient specific
Average powers per circuit element

- Determine instance powers via SoC power analysis or transistor simulation
  - Average power for all cell/block instances
  - Alternatively: transistor-level power can come from FastSPICE

- Simulate representative activity levels using appropriate stimuli
  - e.g., for each mode of chip operation
Outputs from FireBolt

- Steady-state 3-D temperature on the die
  - Metal wire temperatures are important
  - Low-K dielectrics: bad thermal conductors
- Backannotates instance temperatures (per circuit element) to static TA and power analysis
  - Show the thermal impact on delay times, leakage currents
  - e.g. Cadence Encounter Platform; Synopsys PrimeTime(-PX)
The temperature data can be used to:

- Identify thermal hotspots, and verify that you are meeting the $T_{J\text{-MAX}}$ spec
- Verify that thermal gradients are harmless
- Help with thermal sensor placement
- More accurately determine the thermal effects on critical aspects of the IC designs, such as leakage power, voltage drop and timing, signal crosstalk and timing, and electro-migration
Google Map for chip temperature?
Do you see where is the thermal problem?
As usual, the devil is in the details

$\Delta T \approx 8^\circ C$
Package and IC co-simulation

Package model at horizontal face of die

Package-level temperature

Die-level temperature

Thermal profile at horizontal face of die
Summary

• Miniaturization, performance and functionality trends are decreasing thermal design margins at the package the chip levels

• Modeling methodologies and standards must increase in sophistication to meet current and future chip and package design challenges. This is being realized by:
  – JEDEC CTM standards for packages
  – Emergence of fine-grain thermal analysis for semiconductor chips
  – Emergence of multi-scale, chip-package-environment analysis methodologies