Thermal Management of Mobile Electronics: A Case Study in Densification

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Tessera

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Outline

- Trends in mobile system thermal management
- Case Study: A miniaturized computing node, components and design considerations
- Thermal analysis of package and the system
- Design optimization
- Summary
Increasing function integrations

- Increasing demand for miniaturization
- Increasing functionality and diversification
- Increasing clock speed
Increasing power dissipation

Total Chip Dynamic and Static Power Dissipation Trends
Background

- Increasing demand for miniaturization
- Increasing functionality in mobile systems
- Increasing clock speed
  ⇒ An integrated approach to design

- Traditional packaging and thermal solutions need to be revisited for optimizing system price/performance/volume
  ⇒ Integrated design from chip to system
  ⇒ Thermal management an integral part of the whole design process

- System drivers
  - Cost: newer manufacturing techniques for integrated designs
  - Materials: Multi-functional (thermal, electrical and mechanical) due to close proximities
  - Test: Built-in test methodologies for higher yields
Many functional devices
- Digital: processors, memory
- RF & analog: transceivers, audio
- Optical: imagers, lens

Thermal components
- heat spreaders
- heat pipes
- TIM
- fan

Optimized design needs to combine the heat dissipating devices with the thermal management components to meet the specifications

In this study, a highly functional module is designed for high performance.

A systematic thermal analysis of the above module is presented
A Miniaturized High Performance Computing Node
Specifications

- Develop miniaturized digital signal processing (DSP) system
  
  AC power source
  
  - Programmable for different applications

<table>
<thead>
<tr>
<th>Specification</th>
<th>Actual</th>
</tr>
</thead>
<tbody>
<tr>
<td>Size (mm)</td>
<td>38 x 48 x 4.7</td>
</tr>
<tr>
<td>Processor Architecture</td>
<td>32 bit</td>
</tr>
<tr>
<td>Processor MIPS</td>
<td>600</td>
</tr>
<tr>
<td>Processor MFlops</td>
<td>300</td>
</tr>
<tr>
<td>FPGA CoProcessor Performance (MFlops)</td>
<td>1800</td>
</tr>
<tr>
<td>DRAM</td>
<td>256 MB</td>
</tr>
<tr>
<td>Power</td>
<td>Up to 6 Watts</td>
</tr>
<tr>
<td>I/O Pitch</td>
<td>1000 µm, 400 µm</td>
</tr>
</tbody>
</table>

- Numerous Potential Applications:
  
  - Image processing
Applications of Imaging Systems

- Homeland Security and DoD Surveillance Needs in Inconspicuous Locations
- Facial recognition
- On vehicle collision avoidance system
- Obstacle detection and avoidance in UAV
- Machine Vision for Robotic Search Vehicles
System block diagram

Operation Model

sensing node → Computing / control node → Transmitter actuator

Computing Node

Boot Flash → Xilinx FPGA → Flash → DRAM

FPGA: XC2VP40 Virtex2 Pro
DDR2: 2 Gb
Flash: 4 Gb
Boot flash: Mb

- carry out computationally intensive tasks (image processing for facial recognition, etc.)
Miniaturization Goal

~6.5” x 3”

~2” x 1.5”
μZ Ball Stack 3D Package for Memory

- Ideal for high density memory applications,
- Individual package test & burn-in leads to higher yields
- CSP design - small size, low profile

Size: 1.5 x 2.0 x 0.5 inch Advanced packaging

- Xilinx FPGA
- DRAM + Flash
Thermal Analysis
Power generators:

<table>
<thead>
<tr>
<th>Device</th>
<th>Power Watt(s)</th>
<th>Qty</th>
<th>Total Typical-Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPGA</td>
<td>3 - 6</td>
<td>1</td>
<td>3 - 6</td>
</tr>
<tr>
<td>Memory</td>
<td>0.25 – 0.5</td>
<td>4</td>
<td>1 - 2</td>
</tr>
<tr>
<td>FLASH</td>
<td>μW</td>
<td>2</td>
<td>-</td>
</tr>
<tr>
<td>PSU</td>
<td>80 -90% eff</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Other</td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>

TOTAL SYSTEM POWER | 6 -10 Watts

Heat flux of FPGA: 2.1 W/cm², package average: 0.8 W/cm²

For particular imaging applications, the case temperature needs to be below 50 °C, which is less than 25 °C over ambient.

Optimized thermal management design is required
First step: establishing boundaries on system power and volume for conduction-based cooling requirements in mobile electronics.

Assume: heat dissipation uniformly distributed within the whole volume of PCB
PCB in perfect thermal contact with upper and lower surface
1.5 x 1.5 x 0.5 inch : \( \Delta T = 185 \, ^\circ C \) under natural convection

Even with perfect conduction, natural convection is not sufficient for the power density and available surface area
The upper boundary for the power density is below 1.5W at given footprint

Simulation conducted with Flotherm v6.1 \( \text{T}_{\text{amb}} = 20 \, ^\circ C \)
Flash – DRAM stack

Flex: 17 x 13 x 0.025mm
die: 16 x 9.3 x 0.15mm

Flash – DRAM stack

Flex: 17 x 13 x 0.025mm
die: 11.3 x 10 x 0.15mm
Ball: 0.35mm, 0.8mm pitch

<table>
<thead>
<tr>
<th></th>
<th>Power (W)</th>
<th>ΔTj (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCB</td>
<td></td>
<td>52</td>
</tr>
<tr>
<td>DRAM1</td>
<td>0.5</td>
<td>63.2</td>
</tr>
<tr>
<td>DRAM 2</td>
<td>0.5</td>
<td>63.5</td>
</tr>
<tr>
<td>Flash</td>
<td>0.1</td>
<td>57</td>
</tr>
</tbody>
</table>

θjb = 10°C/W;

Build model to quantify components’ temperature dependence on power
BT substrate: 31 x 30 x 0.5mm (4 lyr)
FPGA: 17.2 x 16.8 x 0.15mm
Ball: 0.6mm, 1.0 mm pitch
Epoxy molding: 23 x 22 x 0.45 mm

- Ambient = 20 °C, Power = 4W
- $\theta_{jb} = 0.8$ °C/W; $\theta_{ja} = 25$ °C/W
- Natural convection
A Preliminary System Model

<table>
<thead>
<tr>
<th>component</th>
<th>FPGA</th>
<th>DRAM 1</th>
<th>DRAM 2</th>
<th>FLASH</th>
<th>PCB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power (W)</td>
<td>4</td>
<td>0.25*</td>
<td>0.25*</td>
<td>0.1</td>
<td>5.2</td>
</tr>
<tr>
<td>Temp (°C)</td>
<td>160.5</td>
<td>159</td>
<td>158</td>
<td>150.5</td>
<td>158</td>
</tr>
</tbody>
</table>

20 °C ambient * 50% duty cycle

This helps to determine the components’ temperature dependence on the system power level.
DRAM-Flash Side Temperature

Flash surface Temp
Flash works like a heat sink

DRAM 2 surface (Flash removed)
Heated by the PCB temp

PCB is heated by the FPGA, and therefore increase the temperature of the memory chips
## Variation of Die Power and Temperature

<table>
<thead>
<tr>
<th></th>
<th>FPGA</th>
<th>DRAM 1</th>
<th>DRAM 2</th>
<th>FLASH</th>
<th>PCB</th>
<th>ΔT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power (W)</td>
<td>4</td>
<td>0.25*</td>
<td>0.25*</td>
<td>0.1</td>
<td></td>
<td>5.2</td>
</tr>
<tr>
<td>Temp (°C)</td>
<td>160.5</td>
<td>159</td>
<td>158</td>
<td>150.5</td>
<td>158</td>
<td>10</td>
</tr>
<tr>
<td>Power (W)</td>
<td>4</td>
<td>0.5</td>
<td>0.5</td>
<td>0.1</td>
<td></td>
<td>6.2</td>
</tr>
<tr>
<td>Temp (°C)</td>
<td>182.5</td>
<td>186</td>
<td>185</td>
<td>173.5</td>
<td>180</td>
<td>9</td>
</tr>
<tr>
<td>Power (W)</td>
<td>6</td>
<td>0.25*</td>
<td>0.25*</td>
<td>0.1</td>
<td></td>
<td>7.2</td>
</tr>
<tr>
<td>Temp (°C)</td>
<td>207.5</td>
<td>202.3</td>
<td>200.5</td>
<td>191</td>
<td>203.5</td>
<td>16</td>
</tr>
</tbody>
</table>

Temperature of all components increase linearly with FPGA power

Temperature gradient within package less than 16 °C

Need to cool the FPGA effectively
Thermal Resistance and Temperature Calculation

A simplified formula to calculate multiple chip temperatures

\[
R_{\text{th (pcb-a)}} = 25 \, ^\circ\text{C/W}
\]

\[
R_{\text{th (FPGA- pcb)}} = 0.65 \, ^\circ\text{C/W}
\]

\[
R_{\text{th (DRAM- pcb)}} = 3 \, ^\circ\text{C/W}
\]

To estimate junction temperature

\[
T_{\text{pcb}} = T_{\text{amb}} + R_{\text{th(pcb-a)}} \times P_{\text{total}}
\]

\[
T_{\text{FPGA}} = T_{\text{pcb}} + R_{\text{th(FPGA - pcb)}} \times P_{\text{FPGA}}
\]

\[
T_{\text{DRAM}} = T_{\text{pcb}} + R_{\text{th(DRAM - pcb)}} \times P_{\text{DRAM}}
\]

This preliminary analysis provides valuable insights for system thermal design

We need to reduce \( R_{\text{th (pcb - a)}} \) from 25 \(^\circ\text{C/W}\) to below 3 \(^\circ\text{C/W}\), which includes thermal resistance of TIM, heatsink, and spreading resistance

Active cooling is required
Optimized Design
FPGA is directly bonded to Cu plate with thermally conductive adhesive

Wire bonded to cavity substrate

The Cu plate can be directly cooled from the bottom

The memory stack and other temperature sensitive devices are placed on an interposer, therefore are separated from the FPGA by a short distance
System Model

Memory module

FPGA module

whole system

interposer

TSC: temperature sensitive chip
To calculate $\theta_{jb}$ of the FPGA, attach an infinite heat sink with constant temperature of 30 °C to the Cu plate

$$\theta_{jb} = 0.33 \degree C/W$$

*regular FPGA packages > 10 °C/W*

Almost all heat from FPGA is removed from the bottom, and the memory interposer is not affected by FPGA.

The cavity substrate has large thermal mass to reduce FPGA temperature variation.
Assume the module is attached to a heat spreader with temperature maintained at 30 °C.

The maximum temperature is at the DRAM, and the TSC is below 44 °C.

External cooling system: to keep the base of the module below 36 °C.
External Thermal Solutions

- Challenges:
  - temp sensitive component $\leq 50^\circ\text{C}$
  - $\Delta T = 50^\circ\text{C} - T_{\text{ambient}}$

Need to keep heat spreader temperature below 35 $^\circ\text{C}$, while dissipating 6W.
=> less than 2 $^\circ\text{C}/\text{W}$ thermal resistance

- One solution:
  - heat pipe
  Remove heat generated by the FPGA directly from the package case
  Low thermal resistance due to phase change heat transfer
  Design flexibility
  High reliability
Summary

- Thermal management is a critical design consideration due to function integration and miniaturization within mobile systems.

- A high density computing module using Tessera’s 3D packaging technology was used as a case study.

- The limit of conduction cooling with given volume is estimated.

- Extensive computational analysis using CFD software showed the influence of system level parameters: on power levels, choice of thermal components, external environment and system size.

- **Integrated design analysis is instrumental in optimizing thermal performance and miniaturization.**
Tessera Engineers:
Celia Morales, Jinsu Kwon and Sean Moran

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Thank You!