Advanced Thermal Management Technologies for Electronic Systems

Ken Goodson
Goodson@Stanford.Edu
Mechanical Engineering
Stanford University

MEPTEC 2005
ITRS View of Thermal Management Challenge

- **Power Q (W)**
  - **0**
  - **50**
  - **100**
  - **150**
  - **200**
  - **250**

- **ITRS Year:**
  - 1999
  - 2001
  - 2003
  - 2005
  - 2007

- **Graph:**
  - **fin-arrays, heat pipes**
  - **excessive volume**
  - **no known solution**

- **Lines:**
  - **High-Performance**
  - **Cost-Performance (including laptops)**

- **Question Marks:**
  - ?
  - ?

- **Legend:**
  - **ITRS**
Thermal Resistance Hierarchy

- $C_{\text{interconnect}}$ and $T_{\text{interconnect}}$
- $C_{\text{transistor}}$ and $T_{\text{transistors}}$
- $C_{\text{chip}}$ and $T_{\text{chip}}$
- $C_{\text{heat sink}}$ and $T_{\text{spread}}$

- $R_{\text{interconnect}}$ and $q_{\text{interconnects}}$
- $R_{\text{transistor}}$ and $q_{\text{transistors}}$
- $R_{\text{chip + TIM}}$
- $R_{\text{heat sink}}$

- $T_{\text{ambient}}$

Device-Level SEM

- Chip carrier
- Si chip
- Heat spreader
- Heat sink
Lots of Thermal Activity

New technologies appearing in a conservative discipline: Pumped liquid cooling in laptops (e.g., Hitachi, Toshiba) and desktops (Apple).

Chip makers are studying liquid cooling in detail, while scaling back power density projections.

Unprecedented startup climate for thermal technologies, in areas ranging from microfluidics and thermoelectrics to interfaces (over $60 million in venture capital in 2004, more likely in 2005).
Outline

• On chip challenges & solutions
• Thermal interface materials
• Advanced heat sinks
On-Chip Thermal Challenges

\[ \text{Peak } \Delta T \sim \frac{j^2}{d_m \rho_m} \frac{d_d}{k_d} N^2 \]

\(~ 30^\circ \text{C at 70 nm node} ~
\(~ 80^\circ \text{C at 50 nm node} ~\)

Interconnect Self Heating

\[ R_{\text{interconnect}} \]

Student: Sungjun Im, Proc. IEDM 2000
Interconnect Self Heating

Student: Sungjun Im. Sponsor – MARCO IFC

Compounding ITRS trends lead to accelerating peak temperature:
- low-k dielectric materials with poor thermal conductivities
- increasing current densities and aspect ratios
- increasing number of interconnect layers

\[
\text{Peak } \Delta T \sim j^2 d_{\text{MET}} \rho_{\text{MET}} \frac{d_{\text{ILD}}}{k_{\text{ILD}}} \eta \ N^{1.7}
\]

![Temperature Contour Plot](image)
On-Chip Thermal Challenges

- Microprocessor hotspots (mm scale)
- Interconnect
- Self heating

$R_{\text{chip} + \text{TIM}}$

$R_{\text{interconnect}}$

$R_{\text{heat sink}}$

$R_{\text{total}}$ (ITRS 2003)


$0.3 \, \text{°C/W}$

100 W

50 W
**Hotspot Cooling by Microchannels**

Jae-Mo Koo, Sungjun Im (Stanford) with Ravi Prasher (Intel)

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**Power Map (200W)**

- **Conventional Heat Sink, Cu Spreader**
  - $\Delta T_{\text{max}} = 21.4 \, ^\circ C$
  - $\theta_{j-TIM} = 0.11 \, \text{K/W}$

- **Microchannel Heat Sink**
  - $\Delta T_{\text{max}} = 13.2 \, ^\circ C$
  - $\theta_{j-TIM} = 0.066 \, \text{K/W}$

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Liquid Water flow

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Hotspot Cooling by Microchannels
Hotspot Cooling by Chip-integrated Thermoelectrics


Die Thickness=50um; $q_{fb} = 680$W/cm²; $q_{avg} = 70$W/cm²
Fireball = 70um; MicroCooler = 70um; Doping=$1\times10^{19}$cm⁻³
On-Chip Thermal Challenges

- Transistor hotspots (nm scale) $R_{\text{transistor}}$
- Microprocessor hotspots (mm scale) $R_{\text{chip + TIM}}$
- Interconnect self heating $R_{\text{interconnect}}$

ITRS transistor in 2010


18 nm
Transistor Timeline

Bulk FET

Silicon substrate

Buried oxide

SOI/SiGe

Strained Si, Ge, SiGe

Silicide

FinFET

UC Berkeley/AMD

Gate

Source

Drain

HfO₂

top gate (Al)

CNT

Carbon nanotube transistor

Stanford

back gate
(p++ Si)

IBM

1995

2000

2005

2010

2015
Transistor Thermal Processes

Students: Eric Pop, Sanjiv Sinha, Jeremy Rowlette
Sponsors: SRC 1043, IBM, Intel

High Electric Field

Hot Electrons (Energy E)

E > 50 meV
τ ~ 0.1 ps

E < 50 meV
τ ~ 0.1 ps

Optical Phonons

τ ~ 10 ps
(v_{op} ~ 1000 m/s)

Acoustic Phonons

τ ~ 1 ms – 1 s
(v_{ac} ~ 9000 m/s)

Heat Conduction to Package

IBM

Source
Gate
Drain

IBM

Heat Conduction to Package

Optical Phonons

Acoustic Phonons

Energy (meV)

Freq (Hz)

Phonon Wavevector qa/2π

Students: Eric Pop, Sanjiv Sinha, Jeremy Rowlette
Sponsors: SRC 1043, IBM, Intel

Optical

Acoustic

\( E > 50 \text{ meV} \)

\( E < 50 \text{ meV} \)

\( \tau \sim 0.1 \text{ ps} \)

\( \tau \sim 10 \text{ ps} \)

\( \tau \sim 1 \text{ ms} – 1 \text{ s} \)

(\( v_{op} \sim 1000 \text{ m/s} \))

(\( v_{ac} \sim 9000 \text{ m/s} \))
2D Monte Carlo of 18 nm Thin-Body SOI Transistor


**ITRS Specs:**
- $L_G=18$ nm, $t_{Si}=4.5$ nm, $t_{OX}=1$ nm
- $N_{SD}=1e20$ cm$^{-3}$, $N_{CH}=1e15$ cm$^{-3}$
- $I_{ON}=1000$ $\mu$A/$\mu$m, $I_{OFF}=1$ $\mu$A/$\mu$m
- $\Phi_{GATE}=4.53$ eV (Mo), $V_{DD}=0.8$ V

*if W/L = 4 then $N_{elec} \sim 2500$ total!*
Phonon Hotspot Temperature

Based on ITRS 2003

Targeted Junction Temperature

Actual Junction Temperature

Hotspot Effect

ULTRA-THINBODY

Year\(^1\)

\(^1\) Based on ITRS 2003
Outline

• On chip challenges & solutions
• Thermal interface materials
• Advanced heat sinks
Carbon Nanotubes in Thermal Interface Materials

Students: Xuejiao Hu, Angela McConnell, Antonio Padilla, Senthil Govindasamy
Sponsors: SRC 1064, NSF NIRT, IBM, Raytheon, Molecular Nanosystems

• Homogeneous mixture with particles
  Hu, Jiang, and Goodson, Itherm 2004, SRC patent pending

• Aligned growth (one side)
  Hu, Padilla, Xu, Fisher and Goodson
  Submitted to Semitherm 2005

• Aligned growth (two sides, “thermal nano velcro”)
  Work in progress! In collaboration with Dai’s group, Stanford
Aligned CNTs on Silicon

Hu, Padilla, Xu, Fisher, Goodson, submitted to SEMI - THERM 2005
Stand-alone Single-walled CNT

McConnell, Jiang, and Goodson, NSF Design, Service & Manufacturing Grantees and Research Conference, 2004

AC heating current

measure $T_{\text{cold}}$

measure $T_{\text{hot}}$

cold side

hot side

$1 \, \mu m$

polysilicon

cold side

hot side

polysilicon

Si substrate

nanotube
Thermal Conductances of Carbon Nanotubes

Student: Angie McConnell. Sponsor: NSF

![Graph showing thermal conductance vs temperature for different types of carbon nanotubes. The graph includes data points for 14 nm MWNT (Kim 2001), 148 nm SWNT bundle (Shi 2003), 10 nm SWNT bundle (Shi 2003), and individual SWNT from the current study.](image-url)
Outline

- On chip challenges & solutions
- Thermal interface materials
- Advanced heat sinks
Space Wars

Heat Sinks are 3000x bigger than chip

They crowd away more important functional components

ASICS
$\sim 1 \text{ cm}^3$

Power Delivery
$\sim 1 \text{ cm}^3$

Heat Sinks, Heat Pipes, Vapor Chambers
$\sim 10^2 \text{ cm}^3$

RAM
$\sim 10^{-1} \text{ cm}^3$

Video
$10^{-1} \text{ cm}^3$
“Dream Heat Sink” (1998 Brainstorm)

- no larger or heavier than microprocessor chip
- targeted cooling at hotspots
- fully-integrated, silent, reliable pump
- temperature sensors control pump flowrate
Microfluidic Cooling: Government Seed

Microchannel Modules

2D
- Channels In silicon
- Thermal attach
- Si chip
- Pyrex seal

3D
- Fluid inlet
- Outlet
- Si chip
- Thermal attach

ElectroOsmotic Pump

Research Background

DARPA Heretic
Intel
AMD
Apple

1999 2000 2001 2002 2003 2004 2005
Microfluidic Cooling: Venture Growth

Research Background
- DARPA Heretic
- Intel
- AMD
- Apple

MicroCoolers for Computers
- Cooligy Startup (VC funding)
- Product Shipment

Timeline:
- 1999
- 2000
- 2001
- 2002
- 2003
- 2004
- 2005

ElectroOsmotic Pumps

Groups of Santiago, Goodson, Kenny, Stanford Mechanical Engineering
Sponsor: MARCO IFC, DARPA, Intel

Idealized pore channel:
Glass or fused-silica capillary wall

Charge double-layer
Deprotonated silanol groups

EOF

\[ u(r) = \frac{\varepsilon \zeta E}{\mu} - \frac{dp}{dx} \left( \frac{a^2 - r^2}{\mu} \right) \]

\[ Q_{\text{max}} = \frac{\varepsilon \zeta}{\mu} \frac{VA}{l} \quad \Delta p_{\text{max}} = \frac{32 \varepsilon \zeta}{d^2} V \]

• Very high volume to flowrate ratio
• Stanford pump performance (Feb 2003):
  \( P_{\text{max}} \sim 2 \text{ atm}, Q_{\text{max}} \sim 40 \text{ ml/min}, \text{Vol.} \sim 2 \text{ cm}^3 \)

Free-standing pump
Silicon micromachined pump
Microfluidic Cooling: Mixed-Signal

Mixed signal I/O module releases chip backside for RF, Photonic, MEMS I/O using integrated electrical/fluidic interconnects.
Microfluidic Cooling: 3D ICs

Vertical Fluidic Microchannels at Chip Corners

Interconnect Layers

Device Layers

Fluidic Microchannel Cooling Layers

Vertical Metallic Via

Lateral Metallic Heat Spreading Structure

Fluidic Microchannel

1999 2000 2001 2002 2003 2004 2005
Briefly: Refrigeration Techniques

1. Vapor-Compression

- Cold Heat Exchanger: Input from Chip
- Compressor
- Valve (Spray or Jet)
- Hot Heat Exchanger: Heat Rejection

2. Solid State

- Cold Side: Input from Chip
- Hot Side: Heat Rejection
- p n p n p n
- Current

3. Acoustic

- Piezoelectric Actuator, ~3 kHz
- Resonator
- Heat Exchangers
Routes to Higher Performance


Low-dimensional solids with reduced phonon conductivity

M. Dresselhaus, Proc. EPRI Workshop, 2004

Point Contacts
(Gmelin et al., MPI; Ghoshal et al., IBM)

Electron Tunneling
(Kenny Group, Stanford; CoolChips)

Thermionic Transport
(Bowers, UCSB; Shakouri, UCSC)
Concluding Remarks

• Power density (W/cm$^2$) is the critical metric for the difficulty of a cooling problem, and is as relevant for individual transistors as it is for hotspots on the microprocessor and air cooling of heat sinks and the computer case.

• Pumped liquid cooling has arrived, and will buy the industry a few more years of power density scaling, specifically to the limits of case-level heat rejection.

• Frontier research opportunities (microfluidics and microthermoelectrics) can extend power density scaling (even to 3D circuits), although they pose major challenges in chip-integration and cost.
# Micro Heat Transfer Lab

Ken Goodson, Stanford Mechanical Engineering

## Current Group

<table>
<thead>
<tr>
<th>Name</th>
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<tbody>
<tr>
<td>Sanjiv Sinha</td>
<td>Roger Flynn</td>
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<tr>
<td>Xuejiao Hu</td>
<td>Julie Steinbrenner</td>
</tr>
<tr>
<td>Sungjun Im (Materials Science)</td>
<td>Evelyn Wang</td>
</tr>
<tr>
<td>Kevin Ness</td>
<td>Ankur Jain</td>
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<tr>
<td>Jae-Mo Koo</td>
<td>Fu-Min Wang</td>
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<tr>
<td>Yue Liang</td>
<td>Eon Soo Lee</td>
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<tr>
<td>Angela McConnell</td>
<td>Dr. Carlos Hidrovo</td>
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<tr>
<td>Jeremy Rowlette</td>
<td>Dr. Eric Pop</td>
</tr>
<tr>
<td>(Electrical Engineering)</td>
<td>Dr. Ching-Hsiang Cheng</td>
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<tr>
<td>David Fogg</td>
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## Recent Alumni

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<tr>
<th>Name</th>
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<tr>
<td>Prof. Mehdi Asheghi</td>
<td>Carnegie Mellon University (ME)</td>
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<tr>
<td>Prof. Dan Fletcher</td>
<td>UC Berkeley (Bioengineering)</td>
</tr>
<tr>
<td>Prof. Bill King</td>
<td>Georgia Tech (ME)</td>
</tr>
<tr>
<td>Prof. Katsuo Kurabayashi</td>
<td>University of Michigan (ME)</td>
</tr>
<tr>
<td>Prof. Sungtaek Ju</td>
<td>UCLA (ME)</td>
</tr>
<tr>
<td>Prof. Kaustav Banerjee</td>
<td>UC Santa Barbara (EE)</td>
</tr>
<tr>
<td>Dr. Uma Srinivasan</td>
<td>Xerox</td>
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<tr>
<td>Dr. Per Sverdrup</td>
<td>Intel</td>
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<tr>
<td>Dr. Peng Zhou</td>
<td>Cooligy</td>
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<tr>
<td>Dr. Maxat Touzelbaev</td>
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