MEPTEC Report

SUMMER 2019

A Quarterly Publication of The Microelectronics Packaging & Test Engineering Council

Volume 23, Number 2

Advanced Materials Challenge Failure Analysis

page 16

Destructive Wire Bond Shear Testing

page 26

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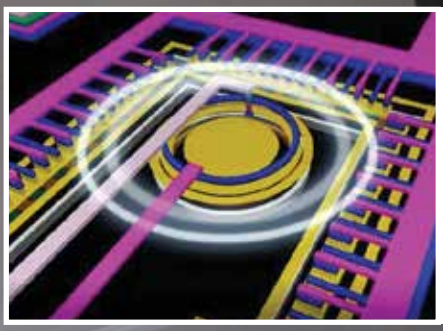
Packaging & Assembly for High-Temperature Electronics

Part III – Materials Behavior – Electrical

page 20



University of Twente researchers have succeeded in connecting two parts of an electronic chip using an on-chip optical link. Using CMOS technology, the intrachip connection via light is instantaneous and provides electrical isolation. This approach can be a safe way of connecting high-power electronics and digital control circuitry on a single chip without a direct electrical link.

page 23

INSIDE THIS ISSUE

Amkor Technology®

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As the original pioneers of the OSAT industry, Amkor has helped define and advance the technology, manufacturing and test landscape.

We deliver innovative packaging solutions with the service and capacity global customers rely on.

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Welcome and Hello!

Ira Feldman
Executive Director, MEPTEC

WELCOME! FROM LONG TIME MEPTEC members to recent subscribers to casual visitors, we are glad you are here.

It is a great pleasure to introduce myself as the new Executive Director of MEPTEC. I'm very excited to join Bette and the team to focus on the event side of MEPTEC.

Since its founding in 1978, MEPTEC has a very rich history of serving the microelectronics packaging and testing industry. This is primarily through exceptional technical and networking events along with the publication of the MEPTEC Report. Our goal has never been on being the biggest or loudest, just to provide the highest quality technical content with the right focus to help our members be they engineers, managers, or executives.

My initial focus will be on the ***Semiconductor Speaker Series Luncheons*** and the 'reboot' of the ***Known Good Die (KGD) Workshop*** on Thursday December 12, 2019 in Silicon Valley. Please save the date as we prepare to celebrate KGD's 20th year!

Some of you may know me from MEPTEC and other related industry events. Others of you may know me from my *Coupling & Crosstalk* column here in the Report. Readers of my column certainly know that I have strong opinions especially on how to improve things and to do things right. However, I value your opinion and welcome all feedback and suggestions. And don't worry, as an engineer I know that negative feedback can be more useful than positive. It's more important that I hear from you on how to improve MEPTEC and to ensure that it serves your needs and those of the industry.

Now that I've introduced myself, please return the favor and let me know how we may help you!

Kind regards,

Ira Feldman
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The MEPTEC Report is a Publication of the Microelectronics Packaging & Test Engineering Council

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Publisher MEPCOM LLC
Editor Bette Cooper
Art Director/Designer Gary Brown
Sales Manager Gina Edwards

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ON THE COVER

Failure Analysis, Shear Testing, and Materials Behavior – three topics discussed in this issue. *Advanced Materials Challenge Failure Analysis* is presented by Ron Leckie from Infrastructure Advisors on page 16; industry veteran and R&D Consultant for Electronics Technology, Dr. Randall K. Kirschman, delivers *Packaging & Assembly for High-Temperature Electronics, Part III – Materials Behavior – Electrical* on page 20; and William Boyce from SMART Microsystems discusses *Destructive Wire Bond Shear Testing* on page 26.

12 FOLLOW UP – The Microelectronics Packaging & Test Engineering Council (MEPTEC) held its monthly meeting at SEMI in Milpitas on April 10. Two speakers outlined their companies' capabilities and demonstrated their own expertise in solving specific industry challenges – Tom Gregorich from Zeiss and Sitaram Arkalgud from Xperi.

HERB REITER
EDA 2 ASIC

16 MATERIALS – Semiconductor packaging technology is advancing faster than ever before. New package technologies are enabling increased circuit density, higher power and higher voltage in today's semiconductor devices. As a result, new materials and assembly technologies are being deployed and, of course, these add complexity to the integrated circuit build process.

RON LECKIE
INFRASTRUCTURE ADVISORS

20 PACKAGING – In Part II of this series thermomechanical and thermal properties were explored. Parts III and IV will focus on basic behavior of assembly and packaging materials at high temperatures. Part III, in this issue, explores basic electrical properties, and Part IV, in the next issue, will explore basic mechanical properties.

DR. RANDALL K. KIRSCHMAN
R&D CONSULTANT FOR ELECTRONICS TECHNOLOGY

23 TECH BRIEFS – The State-of-the-Art Technology Briefs contains articles from the Binghamton University S3IP "Flashes." Binghamton University currently has research thrusts in healthcare/medical electronics; 2.5D/3D packaging; power electronics; cybersecure hw/sw systems; photonics; MEMS; and next generation networks, computers and communications.

DR. GAMAL RAFAI-AHMED
XILINX

DEPARTMENTS

AMKOR NAMES DANIEL LIAO AND GIL TILY TO BOARD OF DIRECTORS

Amkor Technology, Inc. has announced that Daniel Liao and Gil Tily have been appointed as new members of the Company's Board of Directors. With these appointments, Amkor's Board has been expanded to twelve members.

Mr. Liao has been a senior executive at Lam Research since 1993 and currently serves as Chairman of Lam Asia Pacific Operations (Taiwan, China and Southeast Asia regions).

Mr. Tily's appointment follows his notice to Amkor of his retirement as Executive Vice President, Chief Administrative Officer, General Counsel and Corporate Secretary, effective in June 2019.

www.amkor.com

DELPHON APPOINTS STEVEN CHAN AS CORPORATE CHIEF FINANCIAL OFFICER

Delphon has appointed Steven Chan as Chief Financial Officer. Mr. Chan is a seasoned executive with extensive experience in leading high-growth organizations in the life sciences and technology industries.

Mr. Chan brings with him over 25 years of broad financial expertise and proven leadership in positioning companies for profitable and sustainable growth.

Prior to joining Delphon, Mr. Chan was Vice President of Finance and Corporate Controller for Arcus Biosciences, Inc., where he helped lead the company to a $125M IPO in 2018 and was responsible for all finance and accounting operations.

www.delphon.com

New Sub-Micron Bonder FINEPLACER® lambda 2 to Make European Debut

AT LASER WORLD OF Photonics in Munich, Finetech will present the successor of its acclaimed sub-micron bonder for research and development. Technological innovations make the high-precision placement and assembly system the ideal starting point for cost-efficient and fast development of opto-electronic products.

As a manufacturer of micro assembly equipment and process technology, Finetech has been supporting start-ups as well as global technology leaders in the development of innovative semiconductor products for more than two decades. The FINEPLACER® lambda - the worldwide epitome of a versatile, high-precision and compact R&D die bonding system with an unrivaled price/performance ratio - is a cornerstone in Finetech's product line-up.

At Laser World of Photonics, the Berlin-based company presents the successor of this successful model. The FINEPLACER® lambda 2 continues the virtues of its predecessor and sets new benchmarks in optoelectronics assembly.

With the FINEPLACER® lambda 2, components can be placed and bonded with an accuracy of better than 1 micrometer - ideal for the high requirements, e.g. in the development of opto-electronic products such as transceivers (TOSA/ROSA) or laser diode modules.

With sub-micron accuracy from development to series production. The FINEPLACER® lambda 2 is the ideal starting point for successful product development in opto-electronics.

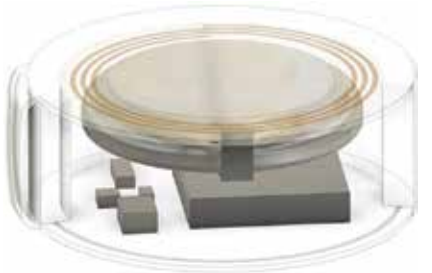
The European premiere of the new FINEPLACER® lambda 2 will take place from 24 to 27 June 2019 at the Laser World of Photonics in Munich, hall B2, booth 212. ◆

World's Smallest Active NFC Sensor Module

DYCONEX HAS DEVELOPED A NOVEL approach to miniaturized, hermetic and highly reliable smart sensor modules with diameters down to 6 millimeters. The modules are ideal for use in medical, food processing, pharmaceutical, chemical or industrial applications.

The tiny modules are based on Liquid Crystal Polymer (LCP), a thermoplastic dielectric material with very low water absorption (< 0.04%), high chemical stability and low thermal expansion. LCP is best suited both as a substrate material and as an encapsulate. LCP's permeability for water and gases is the lowest among all polymeric materials. Phosphate buffered saline and sulfuric acid soak tests with an embedded, moisture sensitive test chip have demonstrated long term stability (> 14 months) and sufficient hermeticity for exposures in harsh environments.

Processing techniques for LCP substrates are the same as for other substrate materials. Resolution of lines, spaces and vias are comparable, multilayer structures can be built up and part of the metal layers can be used to



form a coil for NFC (Near Field Communication). The substrates can be assembled with standard SMT processes as well as connected and sealed without the need for any adhesives by benefiting from its thermoplastic properties. LCP is a homogenous material and can be easily machined with UV lasers with a precision down to the micrometer scale, for example to integrate cavities and openings for recessed components.

For further information on the sensor modules please contact Dr. Eckardt Bihler, Business Development & Program Manager at DYCONEX. ◆

DISCO to Construct New Building at Nagano Works Chino Plant

DISCO CORPORATION has decided to invest approx. JPY 17.5 billion to construct a new seismically isolated building at Nagano Works Chino Plant (Chino City, Nagano).

With the introduction of fifth generation (5G) communication systems accelerating, the semiconductor and electrical components markets, including the development of IoT, self driving systems, and remote medical technology, are expected to expand. The demand for DISCO's precision processing equipment and tools is also expected to increase accordingly. In response to the expected growth of these markets, DISCO is expanding Kuwabata Plant (Kure City, Hiroshima). However, it was determined that further enhancement of the production system will be required.

In addition, most of the precision processing equipment and tools are currently produced in Kure and Kuwabata Plants, which are located in Hiroshima. Seismically isolated structures have been adopted in the buildings at both plants, and construction to ensure an independent water source has been conducted to protect against future water outages. However, the distance between the two plants is only about 10 km. Therefore, in order to prevent a situation where both plants cannot function should a disaster affect the entire area, resources must be divided further. In consideration of these factors, DISCO has decided to begin construction of a new building at Nagano Works Chino Plant.

Construction of the building is scheduled to begin in July 2019 with an estimated completion date of December 2020. ◆

KYOCERA and Vicor to Collaborate on Advanced Power-on-Package Solutions

KYOCERA AND VICOR Corporation will collaborate on next-generation Power-on-Package solutions to maximize performance and minimize time-to-market for emerging processor technologies,. As a part of the collaboration between the two technology leaders, Kyocera will provide the integration of power and data delivery to the processor with organic packages, module substrates and motherboard designs. Vicor will provide Power-on-Package current multipliers enabling high density, high current delivery to processors. This collaboration will address the rapid growth of higher performing processors, which has created proportionate growth and complexity in high-speed I/Os and high current consumption demands. ◆

ON SEMI RANKS 485 ON FORTUNE 500

ON Semiconductor Corp. announced that it has been named to the Fortune 500 list of America's largest companies by revenue for the second year in a row; moving up seven positions from last year. In addition to this accomplishment, ON Semiconductor was recognized in 2018 as one of Fortune's 100 Fastest Growing Companies, one of Wall Street Journal's Management Top 250, was listed on the Dow Jones Sustainability Index and was recently recognized by Ethisphere as one of the World's Most Ethical Companies for the fourth year in a row.

www.onsemi.com

XPERI AND LG ANNOUNCE LAUNCH DATE FOR DTS CONNECTED RADIO PLATFORM

Xperi Corporation and **LG Electronics** have announced the development and integration of DTS® Connected Radio™ technology into automobiles sold around the world. The first implementation will arrive at dealerships in 2020. Xperi will deliver to LG the DTS Connected Radioplatform, which enables an engaging incar radio experience, combining over-the-air radio with IP delivered content. Utilizing an IP connection installed in a vehicle, DTS Connected Radio delivers an innovative analog and digital FM experience. DTS Connected Radio aggregates metadata, such as artist and song information, station contact information and more, directly from broadcasters around the world to deliver an enhanced in-vehicle radio experience.

www.LG.com
www.xperi.com ◆

Integra Technologies Announces New Headquarters

INTEGRA TECHNOLOGIES has announced that it has moved it's corporate offices into a new facility in Wichita, Kansas to accommodate rapid company growth. Expanding by 14,000 sq feet, the new location will house the company's administrative, sales, and support staff, making Integra's total footprint approximately 115,000 sq.ft.

The expansion is due to the increase in business the Qualification, Design Verification and Reliability Testing Services division has encountered over the last year. In 2018, Integra Wichita completed over 600 complex military and aerospace part qualifications, having processing times of 12 – 26 weeks each.

Integra's Wichita factory is on pace to perform over 700 complex military and aerospace part qualifications

in 2019. With the increased demand, Integra made the decision to move the corporate staff out of the Wichita factory to allow for further expansion of production capabilities. Integra plans to further increase the production space in 2019 adding new equipment and engineering staff.

"The move will allow us to better serve our entire customer base of semiconductor manufacturers, military/space/aerospace, automotive OEMs, and medical device customers by increasing our capacity and reducing lead times," said Brett Robinson Integra's President & CEO. "Integra is currently seeing rapid increase in production at all three factory locations. We are looking forward to continued growth throughout the rest of 2019 and beyond."

The corporate office remit to address remains the same, 3450 N. Rock Rd., Bldg #100, Wichita, KS 67226. For more information contact Integra Technologies, sales_inquiry@integra-tech.com ◆

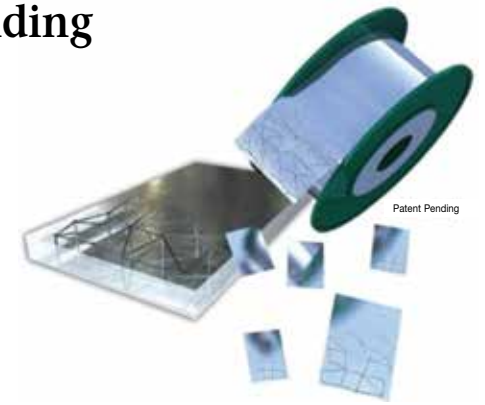
Indium Corporation Launches InFORMS® ESM02 for Die-Level Bonding

INDIUM CORPORATION HAS LAUNCHED InFORMS® ESM02, a reinforced matrixed solder composite specifically designed to produce consistent bondline thickness for die-level attach applications.

Indium Corporation's InFORMS® ESM02 is a reinforced solder fabrication that produces a high-reliability solder joint with increased thermal and mechanical performance.

Until recently, InFORMS® technology was only applied at the baseplate level. New production capabilities have expanded its use to the die-level with a bondline of 50µm. Other benefits of InFORMS® include:

- Drop-in replacement for other bondline control methods
- Increased lateral strength
- Bondline co-planarity
- Improved thermal cycling reliability
- Available in ribbon and preforms



Indium Corporation is a premier materials manufacturer and supplier to the global electronics, semiconductor, thin-film, and thermal management markets. Products include solders and fluxes; brazes; thermal interface materials; sputtering targets; indium, gallium, germanium, and tin metals and inorganic compounds; and NanoFoil®. Founded in 1934, the company has global technical support and factories located in China, Malaysia, Singapore, South Korea, the United Kingdom, and the USA.

For more information about Indium Corporation visit www.indium.com. ◆

COUPLING & CROSSTALK

By Ira Feldman

Electronic coupling is the transfer of energy from one circuit or medium to another. Sometimes it is intentional and sometimes not (crosstalk). I hope that this column, by mixing technology and general observations, is thought-provoking and "couples" with your thinking. Most of the time I will stick to technology but occasional crosstalk diversions may deliver a message closer to home.

5 Thoughts About 5G

1 – Just in time. The cell phone has become a commodity that has saturated a finite market. Everyone has one and the sales pitches are becoming more like the automotive industry trying to convince you to trade up to a new model with almost the same functionality. 5G is the marketer's dream — Premium Performance! — for handset companies and network carriers. Just because the new car can do 250 miles per hour, will you ever drive it that fast? Especially when the availability of the required "premium fuel" (network) is unknown?

2 - It's here! It's here! Well, sort of… 5G phones are shipping today from Samsung and a 5G 'add-on' module is available from Motorola. Others plan to bring new phones to the market 'shortly'. In a few test areas in the US you can see how much faster 5G really is (about 10x the data speed of the current 4G wireless network). And 'select customers' can access 5G networks in Korea and Japan. Handset companies are marketing the heck out of 5G in hopes of spurring sales and motivating wireless carriers to roll out infrastructure faster. So is this the classic "build it and they will come" or closest to "sell it so they will build it"?

3 - Waves of Disruptive Innovation. Remember how the BlackBerry was 'the phone' when everyone wanted to do more than talk? The first wave of disruption was the BlackBerry serving up your emails on your phone. (Remember the Pavlovian response people had to the 'ding' announcing a new email?) Then a following wave delivered this really cool looking and very expensive phone that no one seriously thought would amount to much. Well, Apple basically cornered the market with the iPhone and its concept of an "Application Store". Today Apple and Samsung, both late entrants, dominate the market.

Just like waves that travel in "groups", 5G will be another group of disruptive waves. Two waves forming on the horizon are the rise of new handset manufacturers, including Google and Chinese brands, and the promised applications enabled by 5G. As part of the race to see where 5G networks are built out first, there may be some disruption in the network equipment side. Huawei is looking to give Nokia and Ericsson a run for their money especially as China may out pace both North America and Europe in terms of network deployment.

4- It's not just phones. Businesses need to prepare for the disruptive technology that is 5G. And this isn't just about beefing up your network to accommodate your customers' and employees' equipment under a bring-you-own-device (BYOD) plan. Yes, as users get hooked on lightning speed and low latency on the carriers' networks, they will expect even higher performance of your in-house network. Don't worry, your network will not be fast enough to keep some of them from complaining. Ask any hotel manager about the never-ending demand for more bandwidth or the inevitable bad Trip Advisor reviews over the speed of the hotel WiFi network.

5- It's more than hype. 5G is not a simple incremental performance update from today's 3G and 4G networks. The order of magnitude speed increase combined with extremely low latency enabling entirely new usage models is what makes 5G disruptive. Think autonomous vehicles, remote surgery robots, truly immersive real time video, and more. **As such, every business – regardless of size or industry – needs to treat this as a disruptive technology not an incremental upgrade.** Being conservative and 'hanging back' to let others lead is a poor strategy since your company will be left in the dust. Even 'Fast Followers' will not reap the rewards of those who embrace the unknown early. The best way to think of the disruption is that of a land grab or a gold rush. Existing markets and relationships will be upended. And just like the California Gold Rush of the 1850's, those who really made the money were not the miners and prospectors but those who sold the essential supplies like shovels, food, and clothing. Remember Levi Strauss? You may be wearing a modern-day version of the miner jeans that made their family fortune.

Okay, you got the message that 5G is disruptive but let's take a lesson from another messenger. Remember Paul Revere? He rode from Boston to Lexington screaming the "British are coming!" Everyone along the route knew they were coming soon. His ride just told them when and which route. The revolutionists' success depended on their preparation and strategy! Okay now, 5G is coming tomorrow morning: what is your strategy to win?

Every company needs to have a strategy in place today for 5G! So not only does 5G need to be a part of your yearly strategic planning process, the tactical implementation needs to be a part of your quarterly business reviews (QBRs) now. (Don't have an effective strategic planning process or QBRs? That should be corrected immediately and we're happy to help.)

In the case of major disruptions like 5G there are many uncertainties especially unknown-unknowns. And I'm certainly not a fan of just jumping in the pool in hopes of being able to learn to swim. Therefore, having a strategy that is continually tested and adjusted is essential. **First make sure you have the stamina to swim (assets to compete). Then jump in the pool with a destination in mind. Lastly, have the proper processes and support in place to adjust as your organization progresses up the learning curve.** With a race to scale (i.e. a land grab) it is essential to learn quickly to remain in the race. Those who wait to enter the race may have to wait until the next disruption – if they are still in the business. Use a stage gate process similar to a Product Lifecycle to deploy resources efficiently and to balance the risk with potential return.

Pin this to your wall:
These questions need to be answered in a company's 5G strategy or any strategy where disruptive technology includes the potential to impact products (includ-

ing services), customers, operations, and markets. For example:

- What can the technology enable or improve in your own or your competitor's **products**?
- What new **products** are now possible?
- How will **customer** expectations change based upon this technology?
- What features or products will **customers** demand and value?
- How can this new technology make your **operations** more efficient?
- What new procedures / processes are needed to deploy and **operate** this technology?
- How will the technology disrupt the existing **market** or create new **markets**?
- What **market** should you be in? Selling products based upon the technology or enabling the technology?

Our business plan in regards to 5G? Helping our clients build the right strategy to grow their businesses as result of 5G innovation. We are prepared to be much more than a messenger of change since everyone knows 5G, like the British, is coming. Our goal is to help successfully guide your company through disruptive changes in technology, markets, and manufacturing concepts.

For more of my thoughts, please see my blog http://hightechbizdev.com.

As always, I look forward to hearing your comments directly. Please contact me to discuss your thoughts or if I can be of any assistance. ◆

IRA FELDMAN is the Principal Consultant of Feldman Engineering Corp. which guides high technology products and services from concept to high volume manufacturing. He engages on a wide range of projects including technical marketing, product-generation processes, supply-chain management, and business development.
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INDUSTRY INSIGHTS

By Ron Jones

The OSAT Landscape

I'VE BEEN IN THE SEMICONDUCTOR industry for a very long time with much of it close to the assembly and test segment. For the past two or three decades, there have typically been around 150 OSAT (Outsourced Semiconductor Assembly Test) providers. These are usually broken into 3 groups with no firm dividing lines among them:

- Tier 1 players are a few companies with billion dollar annual revenues, multiple factories in various Asian countries and sufficient profit to support the development of advanced packages and technologies such as 2.5/3D and wafer level interconnect.
- Tier 2 players that have 100+ million dollar annual revenues, one or two factories and profits that typically limit them to spending CapEx on process upgrades like conversion from Au to Cu wire bonding or capacity expansion.
- Tier 3 typically have a single factory located in a low labor cost region. They often focus on a limited number of high volume, very cost sensitive packages.

Each year, some OSATs disappear, usually due to acquisition or going out of business, and new ones come on the scene.

For the past several years, there has been a high level of M&A activity in the semiconductor industry, averaging 100 + billion in annual acquisitions, most involving IDM and fabless semiconductor device companies. Though in the minority, some acquisition has taken place in the OSAT space, examples include:

- JCET's (Jiangsu Changjiang Electronics Technology) acquisition of STATS ChipPAC.
- ASE's (Advanced Semiconductor Engineering) acquisition of SPIL (Siliconware Precision)
- Amkor's increased ownership in J-Devices to 100%.

There has typically been a division in outsourced semiconductor manufacturing between foundry (front of line) and OSAT (end-of-line) processes with little overlap in capabilities. Foundries manufactured the wafers and OSATs assembled the chips into completed IC's. There were operations like wafer thinning and bumping that fall in the middle and might go to one or the other. With complex packages that involve a number of steps that don't clearly fall into fab or assembly, a new middle-of-line category has emerged and is growing quickly. There is competition between foundry and OSAT to capture this extra source of revenue and lock in customers.

An obvious question is why foundries or OSATs don't offer the full range of fab, probe, assembly and test processing. For many years, attempts have been made and all have failed. The underlying reason is that a key success factor in outsourced manufacturing is utilization of capital intensive resources.

- Wafer fab capacity utilization revolves around nodes, poly/metal layers, etc.
- Probe capacity utilization revolves around device technology: digital, analog, mixed signal, RF
- Assembly capacity utilization revolves around package types and pin count
- Test capacity utilization revolves around device technology and test handler configuration.

It is virtually impossible to co-optimize utilization of these assets within an outsourced manufacturing company unless you have a very simple and controlled product mix, e.g. DRAMs. This is not the environment of outsourced manufacturing. One way to achieve turnkey process support is through partnerships between foundries and OSAT's.

There is a lot of talk about TSMC and Samsung, the largest foundries, offering services that were typically supplied by OSATs. One should note that instances of this are few and far between and usually involve a mega customer like Apple and not the average IDM or fabless company. The reasons for limited penetration are enumerated in the capacity utilization above.

The influence of China in the OSAT space will continue to grow. Historically, China's support for assembly/test has been on lower lead count, lower technology packages serving local market applications. The Chinese government has earmarked funds to grow the impact in the world semiconductor arena, but it is unclear how much will go towards advancing assembly/test versus wafer fab and semiconductor device design. Note the Chinese government did assist JCET in the acquisition of STATS ChipPAC, the fourth largest OSAT.

I think we will continue to see a large number of OSATs, split among the 3 Tiers, driven by the IDM and fabless companies that provide the world with $450+ billion in semiconductor devices:

- Advanced packages and technology requirements will continue to support the growth of Tier 1 and some Tier 2 suppliers
- The need for continuing cost reduction will drive support of many of the Tier 3 players in lower cost countries on highly cost sensitive packages.
- The lack of a significant number of broad product range suppliers that can support all of a customer's package requirements
- The need for IDM and fabless companies to have second sources to avoid risk and support customer driven satisfaction. ◆

Update on 3D X-ray and DBI Technology for Advanced and 3D Packaging

Herb Reiter, President
eda 2 asic

Editor's Note: This article first appeared in 3D InCites, and is printed here by permission.

The Microelectronics Packaging & Test Engineering Council (MEPTEC) held its monthly meeting at SEMI in Milpitas on April 10. Two speakers outlined their companies' capabilities and demonstrated their own expertise in solving specific industry challenges.

Tom Gregorich presented why and how Zeiss supports IC package inspection with 3D X-ray machines, then Sitaram Arkalgud conveyed the benefits of Xperi's direct bond interconnect (DBI™) technology for interposer (2.5D) designs and vertical die stacking (3D).

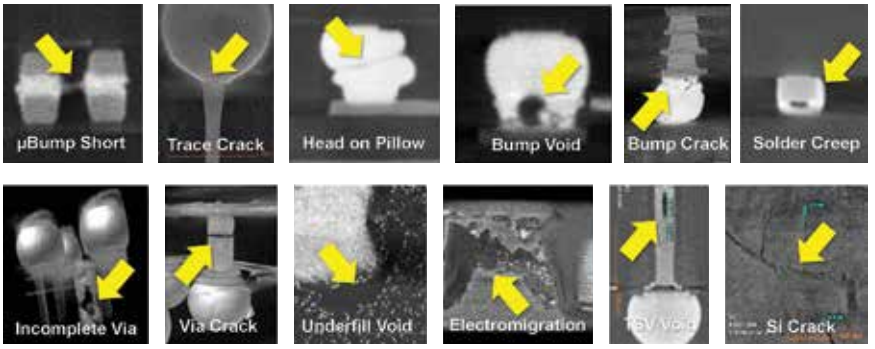

Figure 1. Demonstrating the versatility of Zeiss' Versa 3D Xray Systems.
(Courtesy Tom Gregorich, Director of Business Development Advanced Packaging, PCS Business Unit, Carl Zeiss Inc.)

Figure 2. Versa XRM measurement workflow.
(Courtesy Tom Gregorich, Director of Business Development Advanced Packaging, PCS Business Unit, Carl Zeiss Inc.)

The Magic of 3D Xray

Zeiss, headquartered in Germany, is well known as a supplier of microscopes, camera lenses, and binoculars. They can do more. Gregorich titled his message "Measurement of Buried Features in Packages Using 3D X-ray". He started with a brief look back in time and explained that inspection of package defects traditionally relied on the sharp eyes and skills of human operators, only supported by magnifying lenses. In recent years increasing pin-count, multi-die assemblies, higher signaling speeds, higher power, and other parameters have made IC packaging much more complex and shifted a significant part of ICs' value creation from the die to the package.

Avoiding hidden cost in the package assembly process — e.g. caused by poor yields and quality problems or missed market windows and lost opportunities — is becoming more important. More thorough and more sophisticated inspection procedures are now clearly needed and economically justifiable.

Because IC final tests only check for electrical performance to be within specific margins, they rarely detect marginal mechanical dimensions inside a package that may lead to reliability problems. This can result in expensive field failures and makes the benefits of 3D X-ray package inspection much more compelling. Gregorich showed how Zeiss applies its metrology expertise to the growing number of IC package inspection challenges. Figure 1 shows a number of defects their Versa 3D X-ray system can detect and visualize.

Figure 2 shows how these 3D X-ray systems accomplish the tasks of capturing, tracking, computing and clearly visualizing defects on prototypes during manufacturing flow development and/or failure analysis. Likewise, in-line inspections allow QA experts to monitor manufacturing margins on samples and,

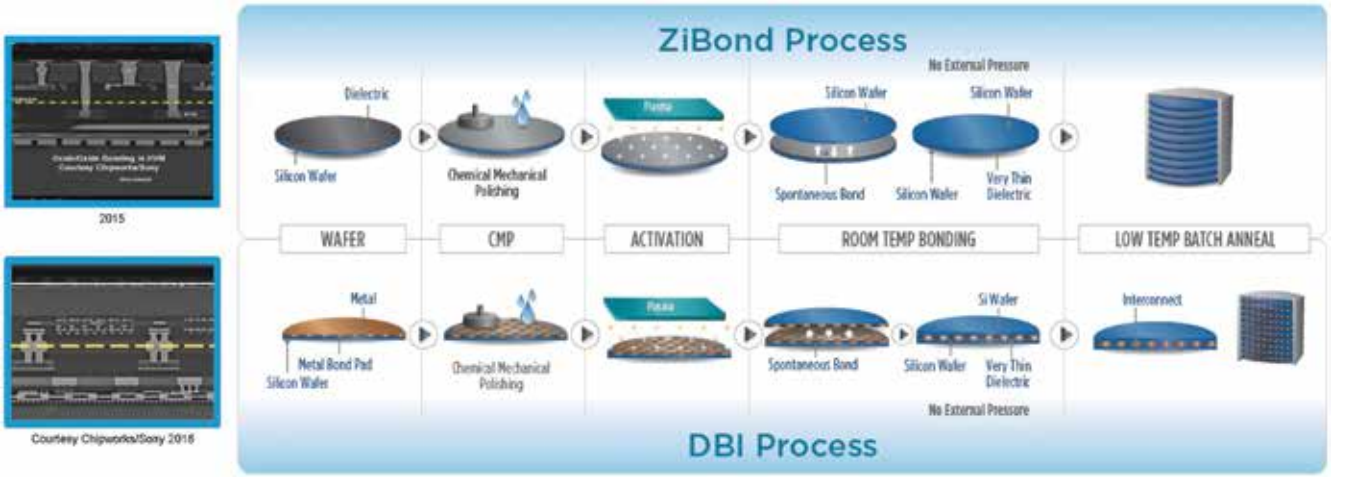

Figure 3. Zibond and DBI™ process flows. *(Courtesy Sitaram Arkalgud, Vice President 3D Applications, Xperi Corporation)*

if necessary, fine-tune the manufacturing flow to assure highest yields and best quality products.

The four quadrants in figure 2 show:

- How parts are loaded onto rotating carriers to offer the X-ray beam a 3D perspective,
- How the inspection station reconstructs the acquired 3D data and passes it on to
- The manufacturer's host computer for data storage and analysis.
- Indicates that Zeiss equipment, in addition to visualizing defects and manufacturing margins, uses 3rd party software to analyze repetitive measurements and generate production reports.

In response to a question from the audience, Gregorich explained that Zeiss' business model is to focus on supplying the equipment for 3D X-ray inspections. If customers are interested in 3D X-ray inspection services, Zeiss refers them to 3rd parties.

Die-to-Wafer Hybrid Bonding is Here

In the second half of this luncheon, Xperi's Sitaram Arkalgud briefly explained the ZiBond process – Oxide to Oxide bonding – then the DBI process and its applications for wafer-to-wafer (W2W) stacking, as shown in Figure 3. He emphasized that Xperi has also developed a die-to-wafer (D2W) process flow to enable the bonding of different size dice.

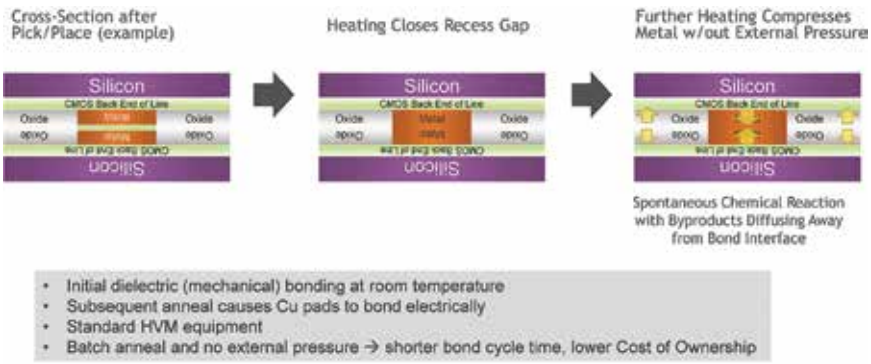

Figure 4. A closer look at the interconnect formation.
(Courtesy Sitaram Arkalgud, Vice President 3D Applications, Xperi Corporation)

Using a face-to-face example, Figure 4 shows how the mechanically strong and low resistance connections are accomplished. Key point: Copper (Cu) expands significantly more per °C than oxide, and creates a mechanically strong bond and a very good electrical contact without external pressure at relatively low temperatures. Arkalgud emphasized that these process steps need to be performed in a cleaner environment than typically used for package assembly. Having said this, he stated that Xperi achieves yields in the high 90s in their Class 1000 cleanroom.

Compared to the complex chemistry in today's microbumps, DBI connections simplify the manufacturing process flow, eliminate the need for underfilling, reduce Z-height, as well as significantly enhance thermal connectivity and vertical heat-flow. In addition, the much smaller DBI contacts, versus microbumps or Cu studs, reduce interconnect capacitance (C) and path inductance (L). Last but not least, the direct Cu-Cu connections offer much less resistance (R) than above-mentioned methods and, with all these RLC advantages, increase circuit performance while reducing heat generation at these vertical interconnects. Figure 5 compares cross sections of both interconnect technologies.

Just in case all these benefits were not convincing enough, Arkalgud added that the DBI density of 100k to 1 million connections per square mm, exceeds micro

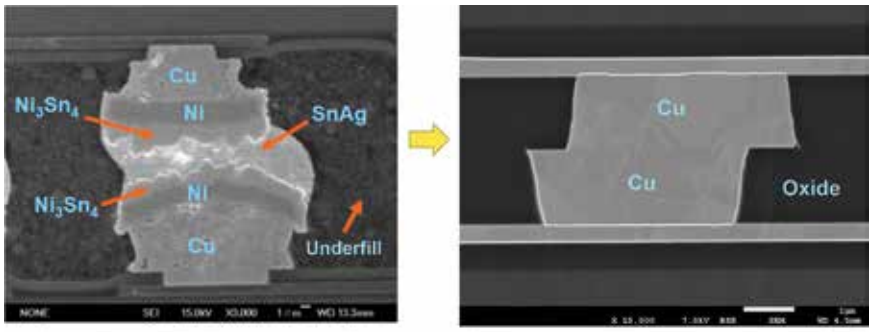

Figure 5. Simplifying interconnects: from microbumps to DBI™.
(Courtesy Sitaram Arkalgud, Vice President 3D Applications, Xperi Corporation)

Test	Standard	Test Condition	Part type (31k chain)	Sample Size	Status of Test Cycle / hrs	Result
Temperature Cycling[1]	JESD22-A104D Condition M	-40°C to 150°C, 1000 cycle	5um pad DBI	45	2000 cycles	100% pass
High Temperature Storage[2]	JESD22-103D	225°C and 275°C 1000 hours	5um and 10um pad DBI	22	2000 hours	100% pass

- Reliability criterion: < 10% change in resistance
  - Resistance of DBI daisy chains typically reduces as the parts are thermal cycled

Figure 6. DBI exceeds automotive reliability tests.
(Courtesy Sitaram Arkalgud, Vice President 3D Applications, Xperi Corporation)

balls' interconnect density by several orders of magnitude.

Considering the rapidly growing and very demanding opportunities for semiconductors in an automotive application, Arkalgud also showed DBI qualification test results that exceed requirements (Figure 6).

Arkalgud reported that DBI for W2W stacking has been in high volume production for years in CMOS image sensors, used in RF applications, and is gaining ground for stacking memories.

As D2W placement equipment now offers high throughput at < 1-micron placement accuracy, the DBI benefits can also be utilized economically for D2W manufacturing.

In response to a question from the audience about the testability of vertically stacked dice, Arkalgud showed an Xperi test vehicle, where the top die was smaller so that the test pads on the periphery of the bottom gave access to the entire circuit. People can also use thinned top dice and open probe pads that connect to the top or bottom die – it depends.

In response to my question, Arkalgud confirmed that DBI and the die placement accuracy available now, also lend themselves perfectly for placing chiplets onto interposers. This will make 2.5D designs and the use of chiplets even more attractive.

DBI Q&A

During the Q&A several more topics were raised and answered by Arkalgud:

Q: Is DBI limited to face-to-face stacking?

A: No, TSVs enable DBI for face-to-back or back-to-back stacking.

Q: What about stacking more than two dice?

A: TSVs also enable multiple dice to be stacked, as Arkalgud showed a slide with 20 dice, each 50μm thick, stacked – at a total height of only 1 mm.

Q: How can a user avoid large TSVs, that would counter DBIs tight interconnect density?

A: Stacking additional wafers on the (thicker) bottom wafer allows thinning of the upper wafers, down to 10 microns, and enables TSVs down to 1μm diameter.

I'm looking forward to meeting you at future MEPTEC luncheons. For schedules and agendas, please check the MEPTEC website at www.meptec.org.

Thanks for reading these two presentation summaries ... Herb. ◆

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Advanced Materials Challenge Failure Analysis

Ron Leckie
Infrastructure Advisors

SEMICONDUCTOR PACKAGING technology is advancing faster than ever before. New package technologies are enabling increased circuit density, higher power and higher voltage in today's semiconductor devices. As a result, new materials and assembly technologies are being deployed and, of course, these add complexity to the integrated circuit build process.

Consider the fact that while the manufacturing technology increases in complexity, so does the challenge facing the failure and yield analysis professionals who have to reverse the process to gain access to the encased silicon to diagnose any failures. Naturally, this only occurs to a very select few of the many tens of millions of chips shipped daily around the world – only on those packaged devices that exhibit performance issues or failure during final test or, even worse, failure in the field. When it gets to the point that a failing device must be decapsulated and analyzed, there is usually significant pressure on the engineer acting as "Sherlock Holmes" to determine the root cause of the problem and generate corrective action. Often, there are few – maybe even just one – example(s) to work with, so the decapsulation process must be effective and not degrade or destroy the product being examined. Otherwise the failure analysis may be stalled or the results could be tainted.

Package decapsulation methods have been around for many decades and generally involve using heated wet etch (acids) to dissolve and remove the molded encapsulant material selectively around the die, leaving the silicon chip and its connecting wires intact and accessible for failure analysis.

Historically, gold bond wires were used and the molding epoxy-based compound could be wet-etched using chemicals such as fuming nitric acid. This author remembers performing this rather hazardous step back in the 1970's with little more than a hot plate, eyedropper for the acid and protective clothing. Since that time, automated decapsulation equipment was developed and sold by companies such as long time market leader, Nisene Technology Group, that made the wet-etch decap process safer, more effective and more repeatable.

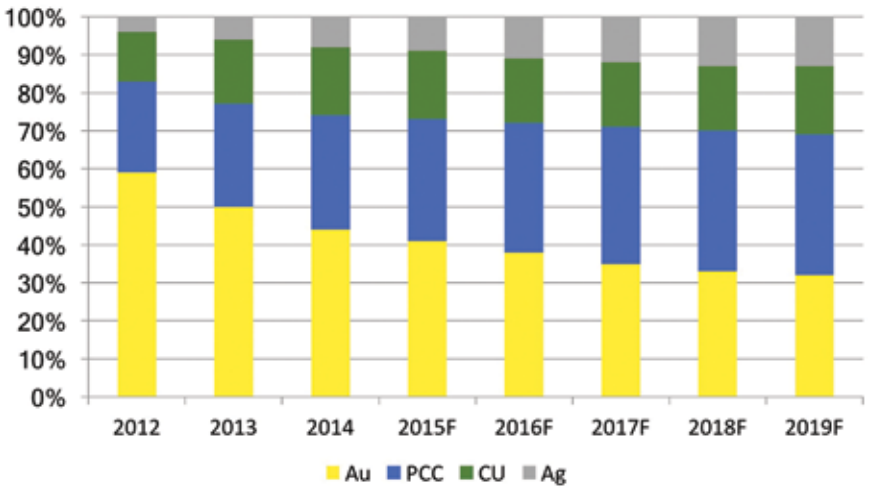

Figure 1. Wire Shipment Share by Material Type. *(Source: SEMI, TechSearch International)*

For both economic and technical reasons, the market for bond wire materials has been evolving over the last decade, showing less gold (Au), more copper (Cu) and palladium coated copper (PCC), while silver (Ag) wire is increasingly being used in more selective applications (see Figure 1). Conventional gold bond wires withstood the aggressive wet-etch and remained intact through the decap process. However as copper and copper alloy wires were introduced, the traditional wet etch process had to be further refined to prevent it from attacking these new bond wire materials. Nisene evolved its wet-etch process in a system called CuProtect, which employs its patented bias voltage application process combined with sub-ambient cooling of the etch acid to protect copper wire materials during decap. The more recent plasma etch technologies do not themselves pose any real threat to bond wires.

There is talk in the industry of an SAE task force that has been working on new requirements for wire pull tests of copper wire and the testing methods for maintaining copper wire integrity. Challenges in the market have shown limited processes are available for wet-chemical and dry etching methods that can fully remove mold compound out to the stitch/second bond while maintaining limited pitting/corrosion to the copper wire (see Figure 2). Further complicating the processes is the requirement of not using any ultrasonic in the decap process or post decap cleaning.

More recently, silver wires have been introduced to give higher density, fine-pitch interconnections at a more affordable cost structure than gold and less fragile than copper. The new silver and silver-alloy materials have challenged traditional wet-etch decapsulation techniques due to silver's extreme sensitivity to corrosion during decap. In fact, wet-etching of silver wire products generally ends up totally removing the wires, rendering failure analysis impossible. Plasma-based decap solutions leaves the silver wires totally untouched.

As a result, failure analysis labs are moving to the new plasma-based decapsulation equipment and processes, which can remove the molded encapsulant without damaging any of the gold, aluminum, copper or silver interconnect materials. Plasma-based tools have been used in wafer fabs for many years to etch the silicon and metal layers of the chip as well as to clean/remove inorganic materials such as photoresist. The chemistry is well known, but only relatively recently has it been applied to package decapsulation by failure analysis tool-makers. The emerging process of choice for multiple reasons is MIP (Microwave Induced Plasma) in which a microwave source ignites or induces plasma in a carrier gas (see Figure 3).

There are different gasses used for the plasma in the various tools. Some use pure oxygen (O_2) gas while others may incorporate carbon tetra-fluoride (CF_4) gas. The reason for this is that mold compounds are generally a combination of epoxy and silica materials. Pure O_2 plasma will remove only the epoxy component, while the addition of CF_4 gas with O_2 will remove both the silica and the epoxy in a faster process. However, if it is given access to the chip surface, CF_4 will attack the silicon and silicon dioxide of the chip, so care must be taken to avoid exposure of CF_4 to the chip surface. Using pure O_2 plasma removes the epoxy but leaves the silica elements, which must then be removed, usually with some ultrasonic cleaning steps. Care must be taken with ultrasonic cleaning since there is the possibility that it can also induce damage to the die surface. The optimum approach would appear to be a combination of the two plasma gasses in a controlled manner.

Figure 2. Copper bond wires after MIP decap (left) and traditional acid-etch (right).
Source: Jiaco Instruments

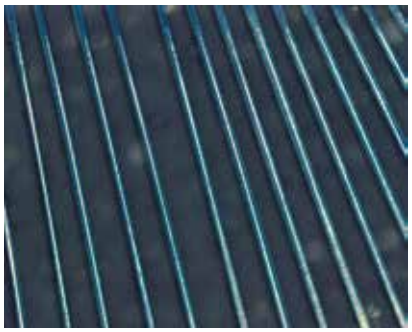

Figure 3. Silver wires exposed and intact after MIP decapsulation.
(Source: Nisene Technology Group)

The main suppliers who have introduced advanced dry-etch decap tools are US-based Nisene Technology Group; the relatively new European company, Jiaco Instruments; and US-based BSET EQ.

Nisene's PlasmaEtch™ is a MIP-based technology system that uses a microwave-induced, downstream-focused plasma etch technology using controlled gases within a vacuum to etch and remove the encapsulant within a two-stage process. In the first stage, their patent-pending process involves the use of CF_4 gas (in combination with O_2) to accelerate the mold compound removal rate until it drops down close to the chip surface. Before any of the chip surface is exposed, the CF_4 is shut off and the process switches over to an oxygen-only (O_2) plasma with the argon carrier gas to effectively perform the final exposure of a clean die surface without introducing any damage. Thus, the first stage of the process is accelerated, reducing the overall process time. Full control over the mix and timing of gas flow enables fine-tuning of this process to optimize for different mold materials and fastest throughput. No ultrasonic cleaning is required. Based in California, for over 40 years, Nisene has specialized in wet-etch and MIP-based plasma decap systems.

Jiaco's MIP-based decapsulation system uses a pure oxygen plasma system at ambient pressure to remove the epoxy within the mold compound. This, however, leaves the silica particles, which must be removed by ultrasonic cleaning. Care must be taken with such mechanical cleaning steps not to induce damage to the chip or wire bonds. With a fixed single gas delivery system for the plasma, the Jiaco's pure oxygen MIP will likely have a longer processing time than more versatile CF_4-based MIP systems that can quickly etch the bulk epoxy and silica filler in the molding compound prior to approaching the die surface. Jiaco was founded in 2014 as a start-up out of the Delft University of Technology, The Netherlands, to focus on commercializing its O_2-only MIP decap system.

The BSET EQ Plaser™ system uses an RF plasma with a combination of oxygen, CF_4 and nitrogen gases used in the recipes. The mixture is reduced in stages from predominantly CF_4 to predominantly oxygen. The RF power source is likely slower than the competitive MIP-based systems. Every 5-10 minutes, the part is subjected to their Fillerblast® cleaning process to remove excess mold compound fillers using CO_2 which forms dry ice for the abrasive removal of the fillers. Apparently, the aggressiveness of this can be reduced to minimize damage to wire bonds. In order to compensate for their slower plasma decap rates, laser ablation is generally also required to remove as much as possible of the excess package molding material ahead of the plasma etch process. The company bundles an OEM laser system incorporated within its Plaser™ system, which likely raises the cost of the tool. BSET is a 20 year old California-based company

that markets its own decap equipment and represents other equipment companies with an array of other equipment for laser and thermal applications.

Regardless of which technology or system is used for package decap, the first step is often a mechanical or laser ablation to pre-cavitate the molding compound down to the tops of the bond wires. From that point onwards, either wet-etch or plasma etch technologies take on the job as outlined above to clear access to the interconnect and silicon system below for failure analysis.

While plasma decapsulation systems primarily address the need to remove encapsulants from around more advanced materials without causing damage, there are additional benefits in terms of increased safety and environmental friendliness. Traditional wet-etch methods use hazardous chemicals that must be safely handled, stored and disposed of in accordance with local environmental regulations. Other big advantages of MIP tools are that the facility requirements are considerably less and the maintenance for the tool is minimal. It is understandable that heated wet-chemicals just naturally can cause more wear and tear on the equipment.

It should be kept in mind that although plasma-based processes have made significant progress in reducing processing times, wet-chemical techniques continue to provide higher throughput and are still a better solution for conventional packaging materials. The MIP-based technologies are clearly superior for tackling advanced materials and we will continue to see both wet- and dry-etch technologies in use in failure analysis labs. It would appear, however, that the use of aggressive ultrasonic cleaning should be minimized or avoided to protect the integrity of copper wire bonds.

As with all tasks, it goes without saying that one should always use the correct tool for the job!

About the Author

Ron Leckie has almost 50 years of experience in the semiconductor and related industries. His background includes 14 years of engineering and manufacturing within the semiconductor industry and 11 years in the capital equipment industry, where he led both the development and marketing of state-of-the-art semiconductor test systems. Since 1995, he has been an independent analyst and consultant to the chip manufacturing industry, bridging "Technology to Business".

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Packaging & Assembly for High-Temperature Electronics

Part III – Materials Behavior – Electrical

Dr. Randall K. Kirschman
R&D Consultant for Electronics Technology

PART I OF THIS SERIES INTRODUCED semiconductor devices and their general high-temperature capabilities that must be accommodated by assembly and packaging, followed by a glimpse of assembly and packaging materials and technology in regard to high-temperature operation.

Parts II, III and IV focus on basic behavior of assembly and packaging materials at high temperatures, to 500–600°C, considering the parameters illustrated in Figure 1. **Part II**, in the previous issue, explored *thermomechanical and thermal* properties, **Part III**, in this issue, explores basic *electrical* properties, and **Part IV**, in the next issue, will explore basic *mechanical* properties.

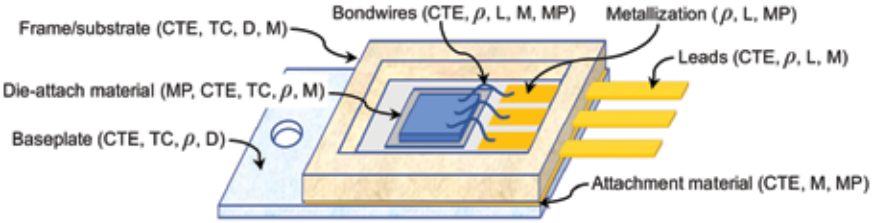
Electrical Properties

Basic electrical properties are

- For ***conductors*** (attachments and interconnections/wiring): electrical resistivity (including size and frequency effects) and inductance;
- For ***dielectrics/insulators*** (substrates, packages): resistivity, dielectric constant and loss (both of which depend strongly on frequency), and breakdown.

Conductors

Metallic conductors used in electronic packaging—e.g. Al, Ag, Au, Cu—all increase their resistivity substantially with increasing temperature. Their resistivity is approximately proportional to absolute temperature, and resistivity at 600°C can be 3-4 times that at room temperature (RT) (Figure 2 *left*)[1][2]. *Temperature coefficients of resistivity* (TCR) may seem small: e.g. Cu is ≈ 0.39%/°C at room temperature, but over the range from room temperature to 600°C—and because TCR increases slightly with temperature—the resistivity of Cu increases nearly 4x.



(CTE = coefficient of thermal expansion, TC = thermal conductivity, ρ = resistivity, L = inductance, D = dielectric constant and loss, M = mechanical, MP = melting point)

Figure 1. A generalized package and basic materials parameters relevant for high temperature operation. *(Repeated from Part II.)*

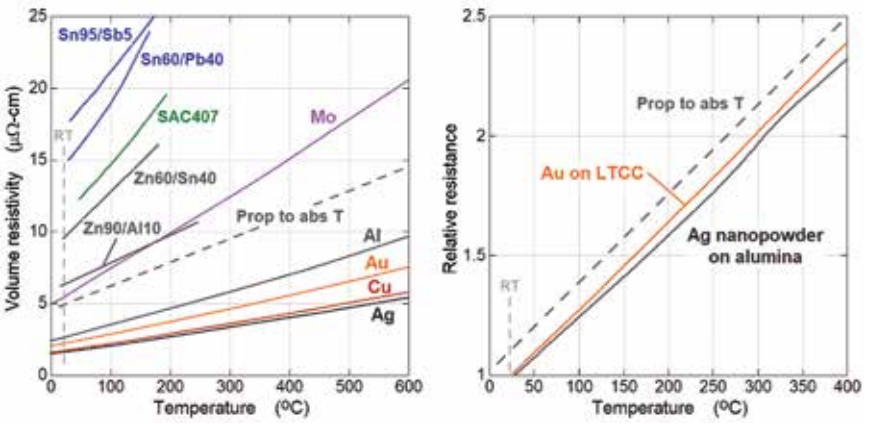


Figure 2. Electrical behavior of conductors, showing strong temperature dependence: pure metals and solders *(left)*[1][2]; thick-film conductors on ceramics *(right)*[3][4].†

Other conductors—alloys, solders and thick films—typically have much higher resistivities than pure metals, but likewise their resistivities increase greatly with temperature. In Figure 2 *right* are examples for two different thick-film conductors[3][4]. Their relative R-versus-T is very similar, essentially proportional to absolute temperature. The materials in Figure 2 exhibit regular behavior, but others may not.

In this temperature range, thermal effects are normally dominant over materials conditions. Serious deviation from the proportionality to absolute temperature would require an extremely disordered material. Normally, deviation occurs only at very low temperatures ≈ –200°C and lower, where thermal effects recede and materials conditions take over.

Generally, in the RT–600°C range, the higher the temperature, the higher the parasitic resistive loss. This may be compounded if a designer chooses wiring materials that have higher resistivity, trading off for durability at high temperature.

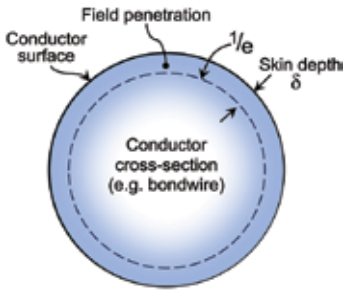


Figure 3. Illustration of AC field penetration and skin depth, δ, contributing to conductor AC resistance; current (blue) is perpendicular to page.

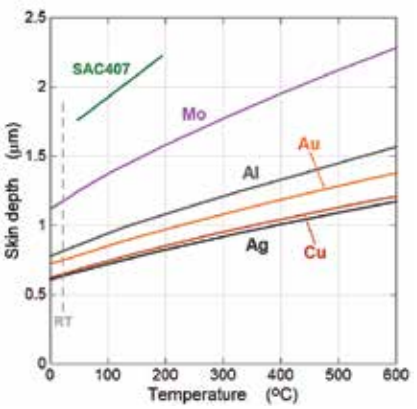


Figure 4. Skin depth, δ, illustrating its temperature dependence; this plot is for 10 GHz, for other frequencies δ varies as 1/√frequency.

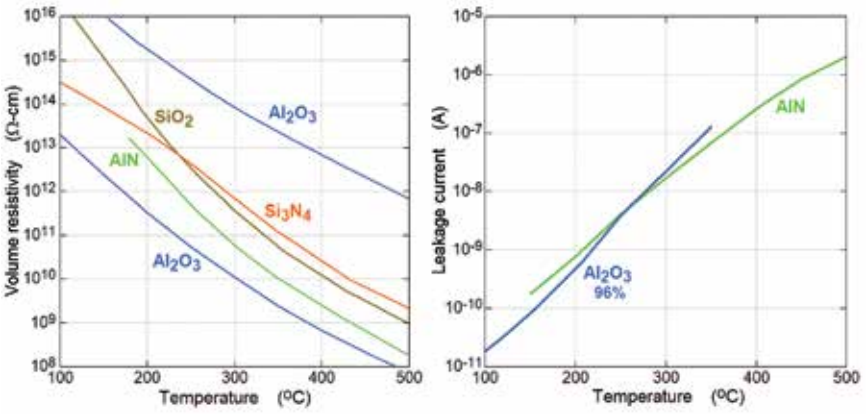


Figure 5. Electrical conduction of ceramics versus temperature: volume resistivity, showing orders of magnitude decrease *(left)*[7][Manufacturers' data]; surface leakage, showing orders of magnitude increase *(right)*[10][11].

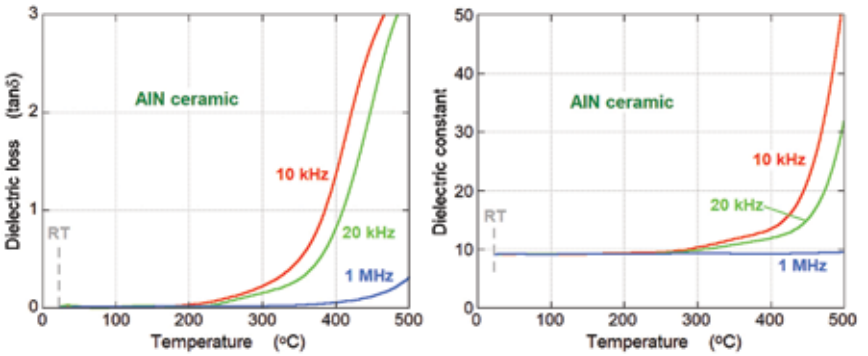


Figure 6. Example of ceramic dielectric properties showing increases in both dielectric constant *(left)* and loss *(right)* with increasing temperature[14].

Electrical conduction is subject to *size effects* and *skin effects*, which modify the effective resistance of conductors; both effects are somewhat temperature dependent.

Size effects arise when the mean distance between conduction-electron collisions (*mean free path, mfp*) becomes as large as the cross-section dimensions of a conductor, such that surface scattering contributes to resistance. At room temperature the mfps for Al, Ag, Au, Cu and Mo are ≈ 10-50 nm, much less than the typical dimensions of a thin-film or thick-film conductor, and as temperature increases, the mfp decreases, reducing any size effects[5]. Thus, for packaging wiring at high temperatures, size effects should usually be minimal.

Skin effects come into play for AC when the skin depth, δ, becomes smaller than the cross-section dimensions, restricting current to a surface layer (Figure 3). For example, at room temperature and 10 GHz, δ ≈ 0.5-1 μm for Al, Ag, Au, Cu and Mo; for solders, brazes and other alloys δ will be larger. Because δ is proportional to the square-root of resistivity, it increases as temperature increases. However, from room temperature to 600°C the increase in δ is not great: a factor of ≈ 2 (Figure 4). For microwave signals, sharp pulses, and thick conductors (e.g. bondwires) skin effects could contribute to a temperature dependence of parasitics. As frequency decreases, skin effects diminish since δ varies as frequency$^{-1/2}$.

Wiring also has *inductance*, which can affect operating frequency and switching, but inductance has negligible temperature dependence[6].

Dielectrics/Insulators

Dielectrics/insulators lose insulating ability as temperature increases: volume resistivity, both DC and AC, drops by orders of magnitude with increasing temperature (Figure 5 *left*)[7][8][9]. But in practical terms—even at 500°C—the corresponding leakage current should be less than a μA for a typical conductor. In practice, however, surface effects may dominate, and surface resistivity also drops orders of magnitude (Figure 5 *right*)[10][11].

Breakdown voltage, applicable to packaging of high-power or high-voltage devices, or for very small dimensions, may decrease, but can depend greatly on the particular material[12]. Again, surface effects—as well as the atmosphere, any overcoat or encapsulant, plus contaminants—are likely more relevant than bulk properties.

For many dielectric materials, including ceramics, cofired ceramics and thick-film, both dielectric constant and loss increase as temperature increases (Figure 6). At low frequencies the increase can be dramatic[8][9][13][14][15]. These increases with increased temperature result from

additional dielectric mechanisms being enabled by greater thermal energy. The increases are smaller as frequency increases because fewer mechanisms can keep pace. Thus, temperature and frequency have opposing effects on AC dielectric behavior.

The *optical properties* of a material are an additional concern if these affect device performance (e.g. optical, infrared, and microwave transducers). The refractive index (the square root of dielectric constant) of most materials is a strong function of temperature. Also, polymers will likely change color permanently at high temperature and render an optical "window" opaque.

The data in Figures 5 and 6 are for *polycrystalline ceramics* used for substrates and packages. These materials may also be used in *single-crystal* form in electronic packaging (e.g. Al_2O_3, *sapphire*), or in semiconductor devices (e.g. SiC), and will exhibit widely different electrical properties.

Upshot

Overall, as temperature increases, conductors become more resistive and insulators become more conductive and lossy—parasitic losses are mounting from both directions. These changes in electrical properties and the associated increase in parasitics will present new challenges. Thus, circuit designers as well as package designers must take these into account and adjust signal levels, operating frequencies, and other circuit parameters accordingly.

Caution

Like thermal conductivity, electrical properties are sensitive to materials conditions. The data in the Figures in this article are derived from particular materials specimens and are not universally applicable: much depends on materials conditions, fabrication and processing details, test parameters, aging, and history. E.g. the two lines for *alumina* (polycrystalline Al_2O_3) in Figure 5 *left* differ by four orders of magnitude in resistivity. Likewise, the data for other materials and situations may differ considerably from those shown. The purpose of the Figures is to indicate typical trends with temperature rather than provide general numerical values. ◆

Read Part IV of *Packaging & Assembly for High-Temperature Electronics* in the Fall 2019 MEPTEC Report.

Acknowledgements

I am indebted to Rich Grzybowski (MACOM), Harold Snyder (Physical Solutions Group), and Jeff Watson (Analog Devices, Inc.) for reviewing this article and for valuable suggestions.

Notes

†SAC407 = Sn95.3/Ag4.0/Cu0.7 Pb-free solder. The Zn alloys in Figure 2 *left* are not eutectic compositions that would be used in practice, but are close compositions for which resistivity data was found.

Room temperature (RT) is taken to be +22°C.

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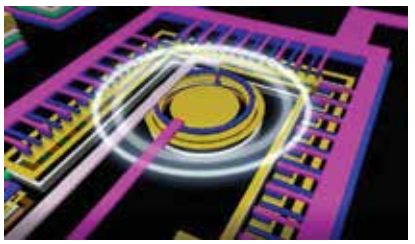
State-of-the-Art Technology Briefs

A special feature courtesy of Binghamton University

We are pleased to continue this feature in the MEPTEC Report, brought to us by new Advisory Board member Dr. Gamal Rafai-Ahmed from Xilinx. The State-of-the-Art Technology Briefs contains articles from the Binghamton University S3IP "Flashes." Full text is available upon request through the IEEC Site at: http://www.binghamton.edu/s3ip/index.html.

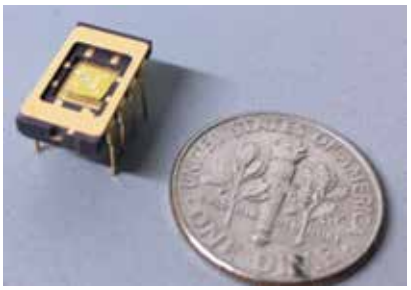
Virginia Tech researchers have new technique to control the magnetism of developed a process to 3D print Kapton (polyimide). Kapton has exceptional thermal and electrical properties with a degradation temperature around 550˚C, doesn't dissolve in solvents, acts as an electrical insulator, and is resistant to ultraviolet irradiation. Kapton is also very stable and can withstand harsh environmental such as radiation, high temperature, chemical reagents. Kapton was previously available only in thin 2D sheets. *(IEEC file #10946, Printed Electronics World, 11/30/18)*



University of Twente researchers have succeeded in connecting two parts of an electronic chip using an on-chip optical link. Using CMOS technology, the intrachip connection via light is instantaneous and provides electrical isolation. This approach can be a safe way of connecting high-power electronics and digital control circuitry on a single chip without a direct electrical link. The researchers created a very small optocoupler circuit that delivers a data rate of megabits per second in an energy-efficient way. The 1 Mbit/s data rate of the optocoupler is acceptable for many applications; Researchers expect this rate can be increased at least tenfold. *(IEEC file #11048, Lase Focus World, 2/6/19)*

University of Tokyo researchers have performed logic operations with a chemical device using electric fields and ultraviolet light. The device and the pioneering methods used, open up research possibilities including low-power, high-performance computer chips. From smartwatches to data centers, all computers feature similar kinds of components, including processors and memory. Conventional computers use electric charge to represent binary digits (1s and 0s), but the new device uses electric fields and UV light. This allows for lower power operation and creates less heat than logic based on electric charge. The device is also vastly different from current semiconductor chips as it is chemical in nature, and it's this property that gives rise to its potential usefulness in the future of computation. The device features disk and rod-shaped molecules that self-assemble into spiral staircase-like shapes called columnar liquid crystals. *(CLC) in the right conditions. (IEEC file #11010, R&D, 1/17/19)*

University of California researchers have developed a new photonic switch that can control the direction of light passing through optical fibers faster and more efficiently than ever. This optical "traffic cop" could revolutionize how information travels through data centers and high-performance supercomputers that are used for artificial intelligence and other data-intensive applications. The photonic switch is built with 50,000 microscopic "light switches," each of which directs one of 240 tiny beams of light. The switch uses multiple integrated silicon structures that can switch on and off in less than a microsecond, approaching the speed necessary for use in high-speed data networks. *(IEEC file #11134, Science Daily, 4/12/19)*



Caltech scientists have developed microscopic components that could usher in the next generation of sensors, mobile phones and quantum computing. These are new versions of phononic devices that make up mobile devices, which have the ability to vibrate extremely fast, moving back and forth up to tens of millions of times per second. To develop the improved devices the researchers created 90 nanometer thick silicon nitride drums that are arranged into grids with different grid patterns containing different properties. The arrangement of the arrays of these drums acts as a tunable filter for signals of different frequencies. *(IEEC file #10991, R&D, 1/4/19)*

MIT researchers have invented a way to fabricate nanoscale 3-D objects of nearly any shape. They can also pattern the objects with a variety of useful materials, including metals, quantum dots, and DNA. It's a way of putting nearly any kind of material into a 3-D pattern with nanoscale precision. Using the new technique, the researchers can create any shape and structure they want by patterning a polymer scaffold with a laser. After attaching other useful materials to the scaffold, they shrink it, generating structures one thousandth the volume of the original. These tiny structures could have applications in many fields, from optics to medicine to robotics. *(IEEC file #10954, Solid State Technology, 12/14/18)*

Researchers from Caltech, et al, have developed a method to make fluoride batteries work using liquid components. This is in early stages of development, but it is the first rechargeable fluoride battery that works at room temperature. Fluoride batteries can have a higher energy density and can last up to eight times longer than batteries in use today. To make the new batteries work in a liquid state, the researchers used an electrolyte liquid called bis(2,2,2-trifluoroethyl)ether (BTFE), which helps keep the fluoride ion stable so that it can shuttle electrons back and forth in the battery. *(IEEC file #10952, R&D, 12/11/18)*

University of Illinois researchers have discovered that tiny, disordered particles of magnesium chromium oxide may hold the key to new magnesium battery energy storage technology, which could possess increased capacity compared to conventional lithium-ion batteries. Lithium-ion technology is reaching the boundary of its capability, so it's important to look for other chemistries that will allow us to build batteries with a bigger storage capacity and a slimmer design. The study reports a new, scalable method for making a material that can reversibly store magnesium ions at high-voltage, the defining feature of a cathode. This is a significant development in moving towards magnesium-based batteries. *(IEEC file #10971, ECN, 12/19/18)*

MARKET TRENDS

China Jiliang University researchers have created a graphene-based sensor based on graphene sheets that can simultaneously detect multiple substances like bacteria and other pathogens in food before it ever hits the supermarket shelves. The sensor is not only highly sensitive but can also be easily adjusted to detect different substances. The researchers used calculations and simulations to design an array of nanoscale graphene disks that each contain an off-center hole. The sensor also includes ion-gel and silicon layers that can be used to apply a voltage to tune the graphene's properties for detection of various substances. *(IEEC file #10956, R&D, 12/4/18)*

The global optical fiber market was $3.4 billion in 2017 and is expected to reach $8.1 billion by 2025, registering a CAGR of 11.6% from 2018 to 2025. Widespread adoption of 5G, rise in implementation of fiber-to-the-home (FTTH) connectivity, and advent of internet of things (IoT) drive the growth of the industry. However, high cost of installation and widespread presence of wireless communication systems would restrain the market growth. On the other hand, increase in investments in optical fiber cable (OFC) network infrastructure would create new pathways in the industry. *(IEEC file #10979, Sensors, 12/18/18)*

University of Tokyo researchers have developed a new system to charge electronic devices such as smartphones and smartwatches wirelessly. The method involves a cuttable, flexible power transfer sheet which charges devices wirelessly and can be molded or even cut with scissors to fit different-shaped surfaces and objects. The sheet is thin and flexible so it can mold it around curved surfaces such as bags and clothes. The system uses conductive coils in the charger to induce a current in corresponding coils in the device. Currently a 400-millimeter square sheet provides about 2 to 5 watts of power, enough for a smartphone. *(IEEC file #11003, Printed Electronics World, 1/7/19)*

Intel has perfected a manufacturing technology called Foveros to stack different chip elements directly on top of each other, a move that should dramatically increase performance and the range of chips Intel can profitably sell. The first Foveros chips will arrive in 2019. If 3D stacking delivers the benefits Intel promises, the performance boost and power savings could once again give you a good reason to invest in a new personal computer. One of the big benefits of 3D chip stacking is that it can dramatically speed up connections between processing logic circuitry and the high-speed memory. *(IEEC file #10958, CNET, 12/12/18)*

The emerging role of 5G wireless networking is being studied for future mobile military communications. The global rollout of 5G will cost service providers the enormous sum of $325 billion by 2025. Millions of dollars have already been spent to tout the benefits 5G will deliver to individual and commercial users, but little attention is paid to the role of 5G in the future world of defense and national security. 5G data moves at 10 gigabytes per second, and latency is less than a millisecond, a hundred times faster than 4G. These attributes will connect sensors and enable unmanned air, sea, subsurface, and ground vehicles to become autonomous. *(IEEC file #11140, Military & Aerospace Electronics, 3/26/19)*

Carnegie Mellon University researchers have found ways to track body movements and detect shape changes using arrays of RFID tags. RFID-embedded clothing thus could be used to control avatars in video games. The researchers call this embedded clothing RF-Wear and it could be an alternative to systems such as Kinect, which use a camera to track body movements. What is unique is the method for tracking the tags, and thus monitoring movements and shapes. RFID tags reflect certain radio frequencies. By attaching these paper-like RFID tags to clothing, they were able to demonstrate millimeter accuracy in skeletal tracking. *(IEEC file #10982, Product Design & Dev., 12/20/18)*

University of Manchester researchers have found a low-cost method for producing graphene printed electronics, which significantly speeds up and reduces the cost of conductive graphene inks. Printed electronics offer a breakthrough in the penetration of information technology into everyday life. The possibility of printing electronic circuits will further promote the spread of Internet of Things (IoT) applications. The development of printed conductive inks for electronic applications has grown rapidly, widening applications in transistors, sensors, antennas RFID tags and wearable electronics. *(IEEC file #10997, Printed Electronics World, 12/26/18)*

The Fan-Out packaging market will grow at 19.4% and a CAGR 2019-24 to reach a projected $3.8 billion in 2024. In 2015, the Fan-Out market was small and

consisted mostly of standard devices like BB, RF, and PMU. But after TSMC's 2016 game-changer with info for Apple's iPhone APE, market value increased 3.5x by 2017. So was the HD Fan-Out market segment created, reducing the market-share ratio of OSATs. Fan-Out platforms are increasingly viewed as one of the top options amongst leading package technologies. *(IEEC file #11056, Electronics Weekly, 2/1/19)*

RECENT PATENTS

Chip package structure with conductive pillar (Assignee: Powertech Technology Inc.)- *Patent No.- 10,157,828-* A chip package structure includes a semiconductor component, a plurality of conductive pillars, an encapsulant and a redistribution layer. The semiconductor component includes a plurality of pads. The conductive pillars are disposed on the pads, wherein each of the conductive pillars is a solid cylinder including a top surface and a bottom surface, and a diameter of the top surface is substantially the same as a diameter of the bottom surface. The encapsulant encapsulates the semiconductor component and the pillars, wherein the encapsulant exposes the top surface of each of the pillars. The redistribution layer is disposed on the encapsulant and electrically connected to the conductive pillars.

Process of fine pitch traces for a solid-state diffusion bond on flip chip interconnect (Assignee: Compass Tech.) *Patent No.- 16/110055-* A method to produce a semiconductor package or system-on-flex package comprising bonding structures for connecting IC/chips to fine pitch circuitry using a solid-state diffusion bonding is disclosed. A plurality of traces is formed on a substrate, each respective trace comprising five different conductive materials having different melting points and plastic deformation properties, which are optimized for both diffusion bonding of chips and soldering of passives.

Landless via concept. (Assignee: Flex Ltd.) *Patent No.- 10,182,494-* A heat sink is mounted to a PCB for thermal heat removal. The PCB is configured with plated through hole vias within a footprint of the heat sink. The plated through hole vias can include thermal via types and signal carrying via types. The signal carrying via types are landless vias on the PCB back side configured to eliminate physical and electrical contact between the plated through hole via and the heat sink. The landless via is configured by removing a conductive annular ring on the back side of the PCB, and then covering this area with an insulating material such as solder mask. The insulating material forms an insulation cap between the via side wall plating and the attached heat sink.

Semiconductor packages with embedded bridge interconnects (Assignee: Intel Corp.)- *Patent No.- 10,157,847-* Semiconductor packages with embedded bridge interconnects, and related assemblies and methods, are disclosed herein. In some embodiments, a semiconductor package may have a first side and a second side, and may include a bridge interconnect, embedded in a build-up material, having a first side with a plurality of conductive pads. The semiconductor package may also include a via having a first end that is narrower than a second end. The bridge interconnect and via may be arranged so that the first side of the semiconductor package is closer to the first side of the bridge interconnect than to the second side of the bridge interconnect.

Device including quantum dots (Assignee: Samsung Research America.) *Patent No.- 10,164,205* - A device including an emissive material comprising quantum dots is disclosed. In one embodiment, the device includes a first electrode and a second electrode, a layer comprising quantum dots disposed between the first electrode and the second electrodes, and a first interfacial layer disposed at the interface between a surface of the layer comprising quantum dots and a first layer in the device. In certain embodiments, a second interfacial layer is optionally further disposed on the surface of the layer comprising quantum dots opposite to the first interfacial layer.

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BINGHAMTON UNIVERSITY *currently has research thrusts in healthcare / medical electronics; 2.5D/3D packaging; power electronics; cybersecure hw/sw systems; photonics; MEMS; and next generation networks, computers and communications. The S3IP Center of Excellence is an umbrella organization comprising five constituent research centers. More information is available at* ***www.binghamton.edu/s3ip***

Integrated Electronics Engineering Center (IEEC) - The IEEC is a New York Center of Advanced Technology (CAT) responsible for the advancement of electronics packaging. Its mission is to provide research into electronics packaging to enhance our partner's products, improve reliability and understand why parts fail. More information is available at ***www.binghamton.edu/ieec***

Center for Autonomous Solar Power (CASP) - The CASP center focusses on thin film solar cells and supercapacitors. The CASP team has been invited to take part in the Cohort 5 NEXUS-NY program to explore market opportunity of a dielectric capacitor technology (patent currently drafted) that recently came out of CASP center. More information is available at ***www.binghamton.edu/casp.***

NorthEast Center for Chemical Energy Storage (NECCES) - NECCES has been extended by DOE until 2020. One of our major goals for 2018 is to build the capability to make prototype lithium-ion cells that are more realistic than the coin cells that are now being used. An industry grade dry-room has been installed, and a pouch cell prototype manufacturing line is now being installed. We expect this to be operational before year-end 2018. More information is available at ***www.binghamton.edu/necces.***

Analytical and Diagnostic Laboratory (ADL) - The ADL provides an array of analytical and diagnostic tools located in a single facility to address the needs of faculty and industry in understanding materials, structures and failures that are found in electronics packaging. The ADL supports the 5 research centers previously mentioned. The facilities of the ADL are available to our industry partners. More information is available at ***www.binghamton.edu/adl*** ◆

Destructive Wire Bond Shear Testing and its Purpose

William Boyce
SMART Microsystems Ltd.

IN OUR LAST ARTICLE "DESTRUCTIVE Wire Bond Testing for Development and Production" was discussed. In this piece we will discuss the use and purpose of one element of the destructive wire bond testing, and that is, specifically the wire bond shear test. In the next article, the wire bond pull test will be discussed in greater depth. The reason that the shear test is being discussed first is that it is our view that it is the first step in a thoughtful wire bond process development plan. The process of wire bonding a wire to a substrate is simply the joining of two metals through force and vibration. The best way to determine the strength and integrity of that weld, is by shearing the weld with a blade to evaluate not only the force required to shear the joint (shear strength), but also to determine the total amount of the intended weld area that is actually welded (nugget size) as a percent of the intended weld area. The wire bond shear test is not a replacement or substitute for the pull testing, but rather a completely different test, with a different purpose and intent, typically used to develop the wire bond process. Shear testing is the often the forgotten or unknown method of testing wire bonds. Perhaps because it has been conspicuously missing from mil STD883 it has gone largely unknown as a testing tool in the new product development process design cycle.

In the product development cycle, the development of the process used to manufacture or produce the new product is an iterative and hopefully a collaborative approach in the new product design phase. In the case of the wire bond process development, once the metal systems and the geometry have been determined, the work of developing a robust repeatable wire bond process must be completed. We always begin the wire bond development cycle with the shear testing. Whether it is a gold, aluminum, copper, wedge, or ball bond, the foundation of any good wire bonded interconnect is the weld between the wire bond foot and the substrate to which it is bonded. In fact the fundamental characteristic of any welded joint is that the weld should always be stronger than the materials being joined by that weld. This is the reason that a wire bond lift during destructive pull testing is considered a rejectable condition in all cases at SMART.

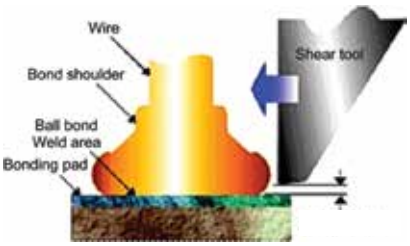
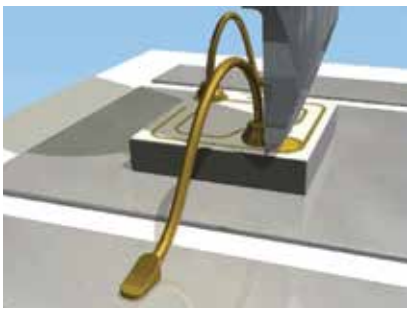


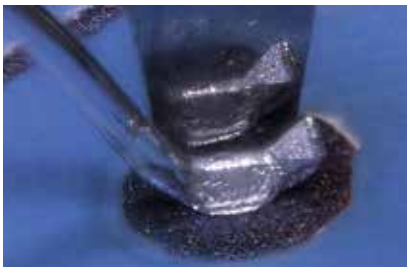
Figure 1.

SHEAR NUGGET	
	Nugget Size
Rank	% of total
1	0 - 25
2	25 - 50
3	50 - 75
4	75 - 100

Figure 2.



Ball Bond Shear



Aluminum Wedge Bond Shear

The destructive wire bond shear test is the tool used to quantitatively and qualitatively measure the integrity of the welded joint of the wire bond. A sharp flat blade is placed parallel to bond foot on the bond pad and raised to a height above the pad approximately equal to 10% of the wire diameter (see figure 1). The force required to shear completely through the welded joint of the bond foot is recorded. The remnant of the welded joint remaining on the bond pad can also be quantified as a percentage of the weld area. We simply rank them on a scale of one through four (see figure 2). All bond wire should be supplied with a certification that includes the tensile strength of the wire. The wire tensile strength along with the shear area can be used to calculate the theoretical shear strength of the joint to insure that the measured values are within reason. Through the application of tools like a thoughtful, well designed DOE, the bond parameters can be optimized to produce welded joints that consistently have high shear values and seventy-five to one hundred percent weld nuggets.

The wire bond shear test is one of many tools that we use to develop, measure, qualify, and maintain the integrity of the welded joint in the wire bonded interconnect system. During the process development phase it is used extensively to develop the wire bond process for long term sustainable manufacturability of a bonded assembly.

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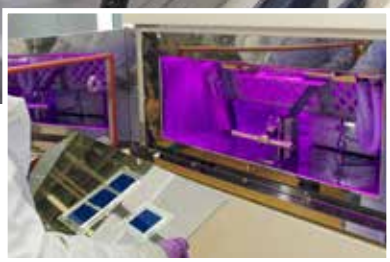

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After release into production it is also good practice to periodically use the shear test as a tool in the overall SPC plan to insure the process has not drifted out of control and the incoming material is still stable (see figure 3). It is also one of the many tools we use in the diagnostic journey of failure analysis. There are many high quality multifunction bond testers on the market today. The bond tester that we employ at SMART is the Nordson DAGE 4000Plus multifunction shear and pull tester.

MIL-STD-883 is a collection of test methods, the "go-to standard" for many companies and industries. So it is interesting that the test method for destructive wire bond shear testing is absent from this widely used standard. That is likely the reason that it often gets overlooked in the wire bond process development cycle. Recently at the iMAPS New England 46th Symposium & Expo, Thomas Green delivered a paper on wire bond inspection criteria in which he discussed the efforts currently underway to update the standard. Hopefully it will one day include a section on shear testing. But for now, if one is involved in the design and development of a microelectronics assembly interconnects that includes wire bonding, then shear testing should not be overlooked, in fact it should be considered the foundation of the process design.

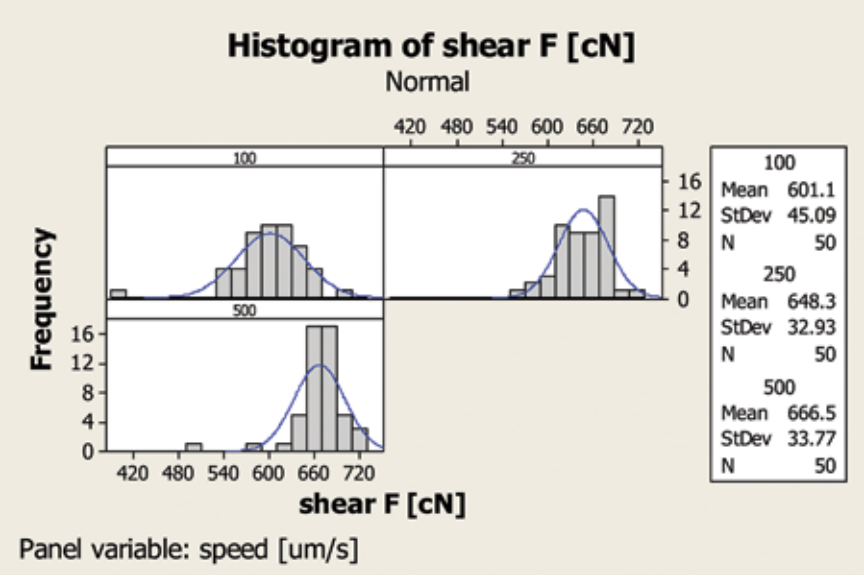

Figure 3.

For more information visit our website at www.smartmicrosystems.com. ◆

William Boyce is the Engineering Manager at SMART Microsystems. Mr. Boyce earned a Bachelor of Science in Engineering degree from the University of Rhode Island and has served in the field for over 20 years as a mechanical design engineer, process engineer, team leader, engineering Manager, and Global Engineering Director. In addition to his current role at SMART, he has held positions at General Dynamics, Texas Instruments, Sensata Technologies and TT Electronics. Mr. Boyce has also been a member of the IMAPS New England Chapter for over 10 years as a session chair. He is EIT certified, a Six Sigma Green Belt, and an industry recognized expert in Al wire bonding.

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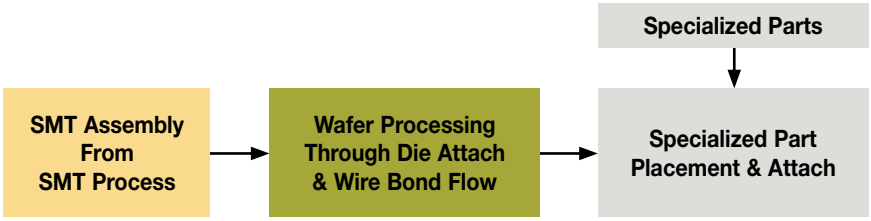

Figure 1: Overall Heterogeneous Assembly Process.

quality requirements. Compatible second source components sources are fleeting.

Developing and managing the supply chain should begin with design and proceed in parallel. Good design is of no value if the parts, materials and equipment required are not available in a timely manner with acceptable cost and quality.

4. Cost. One of the most popular trends – the requirement to reduce the size of heterogeneous devices to make them more convenient to use, often minimizes power consumption and costs by utilizing a small amount of material. However, cost is raised by the increased number of parts, the complexity of the supply chain, the number of assembly processes and the increased precision required by the small size.

Despite the design challenges, many applications are enabled with heterogeneous integration. Table 1 provides examples of those applications and the adoption status in today's market.

Heterogeneous Assembly Can Require 50+ Manufacturing Process Steps

A very simplified assembly flow of the most common heterogeneous assembly process often starts with SMT, as shown in Figure 1.

Some of the common packaging methods that can be utilized for heterogeneous devices include:

- Die stacking with and without spacers
- Flip chip
- 2.5 D integration utilizing Silicon interposer
- 3.0 D integration using through-silicon vias
- System in Package (SIP) utilizing multiple interconnected die and parts
- Chemistries deposited in arrays
- Sealing of liquid channels
- Optical chains; LED, lens, filter, photodetector, etc.

Increased Demand for Heterogenous Assembly

The trend in many new electronic products is to combine the data gathering, analysis, storage and communication capability of classic electronics with additional components that interact with the user and environment to gather the primary information. Prime examples are medical devices and smart home electronics.

However, there are limited numbers of compatible design software and capable manufacturing resources. At previous inflexion points in our industry, such as SMT, industry groups gathered to help facilitate the growth of resources *(Ref. 1 The SMT Council)*. Efforts have been initiated in the past to facilitate Heterogenous acceptance *(Ref 2. The 3D Business Council)* but were too early to gain traction.

If the number of recent seminars that have focused on Heterogenous Integration is any indication of interest, then the time is ripe for the industry to agree on common infrastructure. ◆

References

Ref 1. SMT Council. https://www.ipc.org/4.0_Knowledge/4.1_Standards/smcstatus.pdf

Ref 2. The 3D Business Council. Initiated by Phil Marcoux in 2012 as an initial effort to facilitate orderly standards and acceptance in the industry. The initial meeting, with over 35 attendees spawned follow-on efforts by SEMI, IPC, IEEE, and others.

ABOUT THE AUTHORS

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Promex
Industries, Inc.

Dick has more than 50 years of technical and executive electronics manufacturing experience. Named CEO of Promex Industries Inc. in 1995, he provides the vision and leadership that result in unique engineering solutions for which Promex is well known. Dick's business acumen, as demonstrated by the acquisition of Quik-Pak in 2014, has ensured Promex continues its history of profitability and steady growth. In addition to being a member of IEEE, IMAPS and OSA, Dick is involved in numerous industry roadmap activities with iNEMI, the IRDS Outside System Connectivity Subcommittee, the MIT Microphotonics Center Communications Technology Roadmap and the AIM Integrated Photonic Systems Roadmap (IPSR) where he chairs the Assembly Technical Working Group. Previously, he was general manager of Kaptron, president of Advanced Packaging Systems, and held executive and engineering positions at Raychem. Dick earned his MBA at Harvard University and BSEE and MSEE degrees from MIT. ◆

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Managing
Director,
PPM Associates

Phil was past CEO and co-founder of one of the first SMT facilities in the US and was named "Father of SMT" by the IPC in 2007. He is the past CEO and co-founder of Chipscale, Inc. one of the first wafer level packaging development companies. He is a member of the MEPTEC Advisory Board, a Member of the Board of Directors for Hopes-Corner, and a past member of the University of Florida College of Engineering Advisory Board. Phil earned an MSEM from Santa Clara University and a BSEE form University of Florida. ◆

Can I Have a Plain Vanilla SIP, Please!

Richard Otte , CEO, Promex Industries
Phil Marcoux, Managing Director, PPM Associates

HETEROGENOUS ELECTRONICS! Much has been written, promoted, and hyped over the past decade about the extension of electronic assembly to what is now called Heterogenous Assembly. This is a very positive and promising enhancement as it allows designers and their end products to benefit from greater functional density and design freedom.

Heterogenous is the latest branding effort to promote the assembly of dissimilar components. Past brands include SIP (System in Package), 3D/2.5D, and MCM (Multichip Modules). What's is new about heterogeneous integration and assembly is the inclusion of non-electronic parts such as lenses, mirrors, fluid channels, chemistry, acoustic devices, etc., that extend device functionality.

As with any new set of capabilities it's necessary for the users, especially the designers, to know what they can and can't use easily, economically, or reliably. It's equally important for anyone wanting a heterogenous assembly to understand what tools and materials are available from the limited base of capable assemblers.

Application	Benefit	Status
Diagnostic medical devices	Enables small devices with many broad capabilities for use locally to speed diagnosis.	Many emerging
Implanted medical devices	Enables pain relief, brain function improvement, repair of lost capability such as hearing and sight, etc.	Many in use, more emerging
Biotech devices	Enables analysis of DNA, proteins, toxins, bacteria, viruses, etc.	Many emerging
Wearables	Enables measuring many phenomena and communicating the data to the individual, to their doctor or to a data base for further analysis.	Many in use, more emerging
Smart mobile devices	The functions of a modern cell phone are enabled. These include RF communication methods, motion and location tracking, cameras, microphones, speakers, vibration and audible alerts, high resolution graphics and images, finger print reader, touch control, etc.	Widely used and a key driver of technology developments
Internet of Things (IoT)	Enables gathering of information and data, analyzing and compressing key the data, communicating between devices and individuals over the Internet.	Emerging, many new applications limited only by imagination

Table 1: Applications Benefitting from Heterogeneous Integration.

Heterogenous Integration Requires Complex Design

As with most products, good performance and low cost starts with and is dominated by good design. Heterogeneous integration makes the design function much more complex than is typical for electronic products because many parameters can impact performance. Additional design issues include:

1. Design software. Especially functional simulation as is done for electronics utilizing SPICE models. Models of that level of sophistication do not exist for most heterogeneous integrated products. Thermal and RF analysis is still being enhanced. Designing heterogeneous devices often requires the use of SolidWorks, 3D design and simulation software, as well as classic electronic design software, and usually some specialized custom software.

2. The lack of good data on materials and their properties. Considering, as an example, that an implantable medical device must cause no harm when it encounters human tissue, it's obvious why having good data on materials used in the device is essential. Fluids or tissue may become contaminated by materials in the implantable device or may cause the device to deteriorate in some manner. Designing around the relevant detrimental phenomena is difficult even when material properties are well known. Optical devices also require extreme mechanical stability to avoid unwanted effects over the life of a product. Optical attenuation results especially from thermal and stress induced motion, but also from yellowing, crazing, etc. The RF properties of many materials (the dielectric constant and loss tangent) vary with frequency, water content, etc., in ways that are poorly documented.

3. The availability of components and materials. Sourcing heterogeneous components is complex due to the wide variety of parts that must be sourced. A wider variety increases the number of vendors needed, the length of the resulting supply chain, the cost resulting from margin stack from multiple vendors, and the need for some level of part traceability and compliance with the variety of

continued on page 29

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Grip Ring Magazines


Grip Ring Shippers


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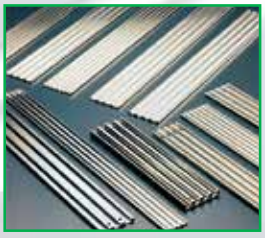
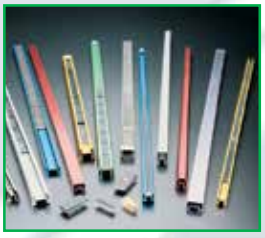
Boat Magazines


I. C. Trays - Multi-Channel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