Changing Market Requirements

Bring

New Challenges and Opportunities

Herb Reiter
eda2asic Consulting, Inc
herb@eda2asic.com  (408) 981 5831
MEPTEC* Luncheon, February 13, 2019

*: MicroElectronics Packaging and Test Engineering Council
Introduction

Key Market Data and Requirements

Multi-die ICs and Advanced Packaging

EDA Tools, Flows and Libraries

Summary
Herb Reiter's Alliance Management Work

EDA: Synplicity
Mentor Graphics
Berkeley DA
Handshake Solutions
CiraNova
ReShape
Flomerics
Gradient DA
Takumi
Mephisto DA

IP: S3 Group
GDA Technology
Adv. Packaging
GSA, SEMATECH, Si², ESD Alliance, Xperi, 3D InCites

SOI: Soitec
SOI Consortium
Innovative Silicon
Equipment: Hitachi SEMs

Fabless Biz Model

TSMC, UMC, Chartered // IBM, TI, LSI, Lucent, Fujitsu, NEC, Toshiba, Mitsubishi

NSC: MMI, DATA I/O, Prolog, Structured Design
Motorola, Daisy, Mentor, Valid
VLSI: Philips, ARM, ES2, EM, ZMD Dresden, IBM Endicott, Canal+ in France

1980

eda 2 ASIC Consulting
18 years, promoting
• EDA Tools
• Semiconductor IP
• Adv. IC Packaging

EDA Tools
5 years
• ViewLogic
• Synopsys
• Barcelona Design

ASIC Technologies
18 years
• National Semiconductor
• VLSI Technology

IDMs

TSMC, UMC, Chartered // IBM, TI, LSI, Lucent, Fujitsu, NEC, Toshiba, Mitsubishi
Herb’s 25 Years in the ASIC Business

- Name should have been CSIC, for CUSTOMER Specific Integrated Circuit!
- BUT, “CSIC” sounds too much like “SEASICK” and got rejected by marketing
- Got Acquired by larger companies
- Turned into Design Services and/or IP Vendors
- These ASIC Vendors evolved into ASSP Vendors, using ASIC Building Blocks for IC Design
- CHANGE is the only thing constant in our industry!
Introduction

Key Market Trends

Multi-die ICs and Advanced Packaging

EDA Tools, Flows and Libraries

Summary
ECOSYSTEM for Electronic Products & Semiconductors

Major Market Segments demanding Electronic System Solutions
Communication/5G, Computing, Industrial, Consumer/VR/AR, IoT, Automotive, Mil/Aero, ...

Electronic System Vendors
Samsung, Apple, Dell, Lenovo, Huawei, BBK, HP, LG, WD

Semiconductor Vendors
Samsung, Intel, SK Hynix, Micron, Qualcomm, Broadcom, TI, Toshiba, WD, NXP

Wafer Fabs
TSMC, GF, UMC, Samsung, SMIC,

OSATs
ASE, Amkor, JCET,

Semiconductor IP & EDA
ARM, SNPS, CDNS, Mentor,

IC Design Services
eSilicon, Open Silicon,

Materials and Equipment for Manufacturing, Metrology and Test
DowDupont, 3M, BASF, Henkel, AMAT, TEL, LAM, EVG, KLA, Nanometrics, Advantest,

Streamlining of ECOSYSTEM-wide cooperation is needed to create attractively-priced electronic products AND decent profit margins!!!
Following Moore’s Law Costs Time and Money

Source: Handel Jones, IBS
In Brian Bailey’s article:

AMAT’s Natarajan, 2/5/’19: “5 years to the next node, for ~20% performance gain.”
https://semiengineering.com/unsticking-moore’s-law/

Only economical for VERY high volume designs!
IC Market Growth Rates


Memories

Source: IC Insights

Gartner’s Revenue Growth Forecast Through 2022

Growth shifting toward commercial applications!
(Presented by Bob Johnson at ISS2019, updated Q4, 2018)
IC End-Use Markets ($B) and Growth Rates

Lower unit volume per design and HETEROGENEOUS FUNCTIONS

Source: IC Insights, Dec 2017

Availability of Heterogeneous Functions

SoC Process extensions for HETEROGENEOUS integration are always 2, 3 or more nodes behind Digital Logic!
This article looks at history, outlines our current challenges with China and suggests:

- **Work with allies to push back on unfair practices**
- **Foster domestic innovation**
- **Prepare for a world with pervasive and powerful Chinese chips**
Customers Demand System-level Solutions

**OLD:** Technology Driven
Selling Components (Cost Focus)

**NEW:** Applications Driven
Selling valuable SYSTEM Building Blocks

- Enabled by Moore’s Law
- Driven by new Applications

IC -> Pkg -> Board -> Rack -> SYSTEM

Application-specific requirements drive supply chain

Source: Stanford SystemX Alliance
# Market Requirements are Changing Significantly

<table>
<thead>
<tr>
<th>CRITERIA</th>
<th>Traditional, technology driven</th>
<th>New, applications driven</th>
</tr>
</thead>
<tbody>
<tr>
<td>Revenue Drivers</td>
<td>Few: PCs, Laptops, Smartphones</td>
<td>Many, Diverse: IoT, 5G, AI, Auto, FHE,...</td>
</tr>
<tr>
<td>Updating Flexibility</td>
<td>Only Software Updates practical</td>
<td>System Upgrades ➔ H/W Updates Too</td>
</tr>
<tr>
<td>Typical Life-time Volume</td>
<td>100,000s to Many Millions</td>
<td>100s to 100,000s, Rarely More</td>
</tr>
<tr>
<td>Functionality</td>
<td>Primarily Logic and RAM</td>
<td>Logic, RAM, NVM, RF, MEMS, Sensors</td>
</tr>
<tr>
<td>Formfactor / Power Diss.</td>
<td>Small / Low</td>
<td>Smaller / Very Low, Energy Harvesting</td>
</tr>
<tr>
<td>NRE / Time / Manpower</td>
<td>~500,000,000 / 1-3 Yrs / 200+ Eng.</td>
<td>&lt; Million / Months / 5-10 people</td>
</tr>
<tr>
<td>Unit Cost Sensitivity</td>
<td>VERY HIGH, <strong>Cost</strong>-driven</td>
<td>MUCH LOWER, <strong>Value</strong>-driven</td>
</tr>
<tr>
<td>Standards Support</td>
<td>Established Worldwide</td>
<td>Emerging, Regional, Appl. Specific</td>
</tr>
<tr>
<td>Ecosystem/User Experience</td>
<td>Mature / Well Trained Users</td>
<td>Emerging / <strong>Education Needed</strong></td>
</tr>
</tbody>
</table>
100 Million “Computers on Wheels” by ~2030 ...

Opportunities for:
- Logic
- Memory
- Misc sensors
- Actuators
- ADCs / DACs
- Displays & drivers
- Several radios
- LEDs & drivers
- Power electronics
- OFF-THE SHELF AND CUSTOM IC PACKAGES

Digital Functions  Heterogeneous Functions  PACKAGING ALTERNATIVES

https://www.machinedesign.com/motion-control/could-5g-be-missing-puzzle-piece-self-driving-cars?NL=MACD-001&Issue=MACD-001_20190206_MACD-001_515&sfvc4enews=42&cl=article_1_b&utm_rid=CPG05000000219930&utm_campaign=23153&utm_medium=email&elq2=37acfbd8bf8a410d971c464e65b3b678
Examples for “Re-Integration” Towards IDMs

Traditional silos re-integrate. Examples from industry. (Presented by Tim Olson, DECA Technologies) at ISS2019
Introduction

Key Market Data and Requirements

Multi-die ICs and Advanced Packaging

EDA Tools, Flows and Libraries

Summary
The 3D-IC Dream ~10 Years Ago

Lower System COST

Smaller FORM-FACTOR

Higher PERFORMANCE per WATT

BUT:
PI & HEAT MANAGEMENT
System-level Solutions in a Package

Value creation moves from single-die ICs to multi-die advanced packages!!! WHY?
Heterogeneous Functions, NRE, Unit Cost, Performance/Watt, Form-factor, Reliability,...

Second generation of TSMC’s Integrated Fan Out (InFO) Packaging for the Apple A11 processor for the iPhone X
SOURCE: YOLE Newsletter, February 2018


High density and high bandwidth chip-to-chip connections with 20μm pitch flip-chip on fan-out wafer level package
IMEC Paper at IWLPC 2018
## Technology Benefits, Challenges and Concerns

<table>
<thead>
<tr>
<th>2D-SoCs</th>
<th>2.5D-ICs</th>
<th>3D-ICs</th>
</tr>
</thead>
</table>
| • “That’s how we always designed ICs”, **BUT**<br>• NRE’s are exploding<br>• Time to Market => Years<br>• Mixing heterogeneous functions extremely costly<br>• Bug fixes very expensive<br>• Reliability @ <7nm<br>• IP availability & cost<br>• Sole source Si supply<br>• Customization difficult<br>• Design reuse difficult | • Lower total power<br>• Enables **modularity**<br>• Mostly: Logic & HBM, **BUT**<br>• *Si Interposer: $\$, <20 cm²<br>• Thin die warpage, stress<br>• Organic I/Po ➔ larger L/S<br>• Glass I/Po still not mature<br>• TSVs processing & area: $\$
**Thermal management**<br>• Interaction between dies<br>• Power and Signal Integrity | • Lowest total power<br>• Unlimited B/W, **BUT**:<br>• Primary use memories<br>**Thermal management**<br>• Interaction between dies<br>• W-2-W ➔ same die size<br>• **Testability**, redundancy<br>• Yield management<br>• Vertical bus standards<br>• NO planning, design & verification tools yet<br>• Monolithic 3D for logic? |

Also: Design and Manufacturing of Wafer and Panel-level single and multi-die packaging is rapidly maturing!<br>Announced WLP/PLP platforms: TSMC’s InFO // Samsung’s ePLP // Nepes’ RCP // Shinko’s MCeP
Two Decades of Direct Bonding Proliferation

ZiBond® Direct Bonding
Direct Bond w/o Interconnect

DBI® Hybrid Bonding
Direct Bond w/ Interconnect

Significantly Improved Thermal Management

Ziptronix founded: Spun-off from RTI to commercialize bonding technology

Cloudtronix

Courtesy of Javi DeLa Cruz, Xperi
Wide Range of 2.5/3D-IC Applications Using Hybrid Bonding
DBI® Die-to-Wafer Readiness

- Some devices do not lend themselves well to wafer-to-wafer bonding
- Throughput 10x faster than TCB
- Only viable way to achieve 16-high HBM3 stacks with height restriction
- Production ready process available for tech-transfer
Data Rate Trends in Gbps per Pin

- Data rate of high-speed channel in DRAM is continuously increasing for higher bandwidth
- Maintaining signal integrity in the high-speed channel is crucial for higher data bandwidth

Source: Youngwoo Kim, Post-Doc at KAIST’s Terabyte Labs. Presented at DesignCon 2019
Apple’s iPAD Pro with A12X Applications Processor
Passives, Passives, Passives and a few ICs

https://electroiq.com/chipworks_real_chips_blog/2019/01/16/the-packaging-of-apples-a12x-is-weird/#
UC Austin’s Professor Heath highlighting the high frequencies needed for 5G technology. DesignCon 2019
Heterogeneous Integration of CHIPLETs (‘‘LEGO Blocks’’)

AND: Resistors, Capacitors, Inductors, Image/ Temp / Pressure / Vibration Sensors, Batteries, Energy Harvesters, ...

Assembly & Test Houses have an inherent advantage (vs Fabs) when a mix of dies from multiple foundries is needed!
Introduction
Key Market Data and Requirements
Multi-die ICs and Advanced Packaging
EDA Tools, Flows and Libraries
Summary
Importance of EDA Tools, Design Flows, PDKs & ADKs

- EDA Tools & Flows and
- Encrypted PDKs & ADKs enable – versus 2D SoCs:
  ✓ Higher Design Productivity
  ✓ Tighter Design Margins
  ✓ Better Testability
  ✓ First Time Success
  ✓ Lower Development Cost
  ✓ Shorter Time to Market
  ✓ Better Reliability
  ✓ Faster Production Ramps
  ✓ Higher Production Yields
  ✓ Lower Unit Cost
  ✓ Higher Profits
  ✓ Easier IP & Design Reuse

The outputs of EDA Tools and Design Flows are only as accurate & valuable as their inputs! They rely on:
- Accurate and up-to-date Process Design Kits (PDK)
- Accurate and up-to-date Assembly Design Kits (ADK) (Materials, equipment and manufacturing flow capabilities)

COST

RELIABILITY
Characterization of IC Packaging Materials for ADK*

Material
- Interposer
  - RDL, Vias, Power Planes
- Underfill
- Bond wires
- Micro balls, C4 balls
- Copper studs
- Pkg Substrate
  - RDL, Vias, Power Planes
- Molding Compound
- UBM
- Heatsink, PCB, etc...

Test Vehicle
- Develop suitable test structure(s) & methodologies to capture all relevant material characteristics for rigid and flex

Characterizing
- Capture relevant characteristics, e.g.
  - Operating temp range
  - Aging mechanisms
  - Thermal conductivity
  - Expansion coefficient
  - Young’s modulus
  - Poisson ratio
  - Dielectric loss
  - Behavior if stretched, compressed, bent, twisted, warped,...
  - Chemical resistivity

Modeling
- Describe all these materials behavior with equations, graphs, tables, ...
- Get accurate and up-to-date inputs for EDA tools

Encrypting
- Encrypt generated data, so that only authorized EDA tools can interpret suppliers’ proprietary information.
- Convey all material capabilities and constraints to the IC & package designers for planning, design and exhaustive verification.

Feedback to Manufacturing

Assembly Design Kit (ADK)

ACCURATE materials characterization and modeling ➔ ACCURATE simulation results

*ADK = Package Assembly Design Kit
EDA and Packaging experts develop jointly – with customer(s) inputs:

- **Die – Package – Board bi-directional Reference Design Flow:**
  - Recommends tools for design planning, implementation and verification steps for multi-die ICs
  - Describes hand-off criteria from designers to manufacturing partner’s assembly and test team
  - Outlines logistics and inputs needed for wafer-probe, interim and final test
  - Suggests how and who to cooperate with in EDA as well as at the assembly and test partner(s)
  - Lists additional info sources: Web-pointers, industry standards, white papers, books, ... 
  - Describes best practices for data exchange between die(s) and package; encourages CO-design

---

**Die(s) Design**
- **GDSII Output**
  - Workstations and PCs with mostly LINUX-based Design Tools

**Package & Board Design**
- **GERBER Format**
  - PCs with Windows-based Design Tools

---

**Maturity of design & manufacturing steps influences when to automate which design step(s) !**
Multi-die IC EcoSystem Cooperation (1)

MANUFACTURING

Wafer fabs provide:
Design Data For Individual Dies
(PDKs)

Assembly & Test house:
Data for CO-design of
Dies, Pkg, Board and Test
Program Development
(ADK)

EDA

(Sub)system-level planning and
partitioning into dies
“Pathfinding”

DESIGN

Application requirements

Planning of the Individual Dies,
Wafer Probe and Production Tests

Implementation & Verification of
Individual Dies and Test-programs

Dies, Package, Board CO-design and
Verification of Designs and Test-programs

No more trial & error prototyping loops ➔ ➔ ➔ Iterations are moving to the design space!
ANSYS Chip Package System Eco System for Power/Thermal/Signal Integrity

: Reproducing Silicon/System Validation Environment

HFSS 3DLayout
Slwave
System Design Parasitic Extraction

Icepak
Chip & Package Aware HTC Generation
Interconnect Joule Heating Generation

ANSYS Mechanical

System Aware
Chip Power Integrity

Chip Aware System
Power Integrity

Chip & System Level
Signal Integrity

CPS Thermal Aware Reliability Analysis

RedHawk-CPA
Chip&PKG Co-analysis & Visualization

ANSYS CMA
Full PDN CPM Generation & Simulation

ANSYS CSM
Full Chip IO Model Generation & Simulation

RedHawk-CTA (Fasttherrm for Self-Heating)
- System & chip aware package thermal analysis
- CPS thermal aware power EM
- CPS thermal aware self-heating with wire & device temperature

ProfilePower
For Early Stage CPM

PowerArtist
RTL Power Estimation & Optimization

Standalone CTA

Package Thermal Profile Generation
IC/Interposer/Package/PCB Cross-Domain Solution System Planning

Assembly, Planning, and Optimization Level

Sigtry
Pre-Layout Signal Integrity
Post-Layout EM Extraction
SI and PI

OrbitIO™
IC Floorplanning, BGA Ball-Map Planning, and System-Level Interconnect Optimization

Digital IC
Analog/RF IC
Interposer
Package
PCB

Innovus™
Digital RTL-to-GDS Implementation and Signoff

Virtuoso®
Analog/RF IC Design Platform

SiP Layout
Advanced IC Packaging

Allegro® PCB
PCB Design

PVS
Verification

Implementation Level

Courtesy of Bill Acito and John Park, Cadence Design Systems
Mentor current design flow for Advanced Packaging

Source data (AIF, LEF/DEF, GDSII, etc)

In-line DRC Rules

2D/3D Interconnect models (RLGC, S. Param)

Xpedition Substrate Integrator
System connectivity prototyping and design management

Xpedition Package Designer
Physical Implementation

HyperLynx FAST3D
Package extraction

HyperLynx DRC
In-process first-pass DRC

Windows & Linux Platforms

Xpedition PCB

Calibre DRC/LVS 3DSTACK
Verification

Calibre RVE
Results visualization

Calibre xACT
Parasitic extraction

Calibre PERC
Reliability analysis

Linux Platforms

OSAT Alliance Program
PDK/ADK enablement

Sign-off rule decks

Courtesy of Keith Felton from Mentor, A Siemens Business
Multi-die IC EcoSystem Cooperation (2)

**MANUFACTURING**
- 1. Tools & Methods for Characterizing, Modeling and Encrypting
- 2. Foundry Process(es) Capabilities and Constraints (encrypted)
- 3. Dies Manufacturing and Test Data

**Models**
- Characteristics of Wafer Materials
- Wafer Fabs Manufacture Proprietary Dies

**EDA**
- Application requirements
- Planning, CO-Design and Verification of Dies AND Test-Program(s) Development
- Soft, Hard and Die-level
- 3rd party IP, IP Blocks

**AUTOMATION**
Multi-die IC EcoSystem Cooperation (2)

**MANUFACTURING**

1. Tools & Methods for Characterizing, Modeling and Encrypting
2. Foundry Process(es) Capabilities and Constraints (encrypted)
3. Dies Manufacturing and Test Data
4. Tools and Methods for Characterizing, Modeling and Encrypting Package Data
5. Assembly/Test Capabilities & Constraints and OSAT's Pkg/Platforms Data (encrypted)

**EDA**

Planning, CO-Design and Verification of Dies AND Test-Program(s) Development

**Automation**

- Dies, (Interposer), Pkg, Board and Test-Program(s) CO-Optimization
- Die(s) Data needed for Pkg & Board Design AND Test-Program(s)

**Application Requirements**

Soft, Hard and Die-level IP Blocks

3rd party IP

If needed: Data about commercially available Packages / Platforms

**Wafer Foundries’ PDKs**

- Models
- Characteristics of Wafer Materials

**Wafer Fabs Manufacture Proprietary Dies**

**OSAT’s ADK**
Multi-die IC EcoSystem Cooperation (2)

**MANUFACTURING**
- 1. Tools & Methods for Characterizing, Modeling and Encrypting
- 2. Foundry Process(es) Capabilities and Constraints (encrypted)
- 3. Dies Manufacturing and Test Data
- 4. Tools and Methods for Characterizing, Modeling and Encrypting Package Data
- 5. Assembly/Test Capabilities & Constraints & OSAT’s Pkg/Platforms Data (encrypted)
- 6. Package Assembly Data AND Test Program(s)

**EDA**

**AUTOMATION**

**DESIGN**
- Planning, CO-Design and Verification of Dies AND Test-Program(s) Development
- Planning, Design and Verification of multi-die IC Package, Board AND Test-Program(s) Development
- Dies, (Interposer), Pkg, Board and Test-Program(s) CO-Optimization
- Die(s) Data needed for Pkg & Board Design AND Test-Program(s)
- If needed: Data about commercially available Packages / Platforms

**Models**
- Characteristics of Wafer Materials
- Characteristics of Materials used for Package & Board

**Wafer Fabs Manufacture Proprietary Dies**

**OSAT’s ADK**

**Pkg Assembly & Test House (OSAT)**

**3rd party IP**
- Soft, Hard and Die-level IP Blocks
- Assembly Data of all 3rd Party Die-level IP Building Blocks in the Package (HBMs,...)
**Multi-die IC Ecosystem Cooperation (3)**

**OSATs need to expand relationships with multiple**

- **CMOS, GaAs, SiGe, SiC, InP, GaN, SOI,... advanced and traditional wafer foundries**
- **CHIPLET sources to integrate die-level IP building blocks into multi-die ICs**
- **MEMS and Sensors suppliers as well as wafer-probe & test experts**
- **Interposer suppliers (silicon, organic, high-res Si) and low-cost litho for substrate**
- **Miniature passives (RLC) suppliers and Flexible Hybrid Electronics (FHE) partners**
- **EDA vendors to**
  - model and encrypt your materials and equipment capabilities for ADK
  - develop reference design flows for your off-the-shelf platforms
  - improve IC test programs, self-test capability, built-in redundancy
  - utilize Software as a Service (SaaS) business model = rent EDA tools by the minute
Introduction
Key Market Data and Requirements
Multi-die ICs and Advanced Packaging
EDA Tools, Flows and Libraries
Summary
50+ years of following Moore’s Law has reached many economical and technical limits

% growth and margins of smartphones are declining → no longer innovation drivers

Lower volume, customer specific solutions offer higher value and better profit margins

Closer and structured supply chain cooperation is needed to meet customer requirements

Designers, Wafer-fabs, Assembly & Test Houses (OSATs) need to become equal partners

Multi-die ICs offer modularity, enable heterogeneous integration, lower NRE & risk

Multi-die ICs increase Performance/Watt, but power density & thermal challenges increase

Study system requirements; leverage your core competence; offer unique solutions

It’s not the strongest of the species that survives, nor the most intelligent. It is the one that is most adaptable to change.

Charles Darwin
~1900: Ford designed and manufactured every Model T component and assembled all the pieces in house.

~2000: Ford’s eco-system partners design and mass-produce most of the Ford Focus components! Ford designs and manufactures ONLY core components and assembles / markets / sells the final product.

The Semiconductor Ecosystem is likely to develop in a very similar way --- in the next few decades!

➔ Leveraging modularity, flexibility, $ savings, time to profit...
Technology AND Business Model = SUCCESS

HETEROGENEOUS Functions ➔ Multi-die IC

APPLICATIONs drive the requirements

Walk the fine line between COST & REL with EDA

It’s COMPLICATED

Nobody spends an annual salary on a car any more
Thank You!
BEFORE deciding your 2019 strategy, please click here and read:

• Brian Bailey’s “Chip Dis-Integration” at
  https://semiengineering.com/chip-dis-integration/

• Ed Sperling’s “Advanced Packaging Confusion” at
  https://semiengineering.com/advanced-packaging-confusion/

• Mark LaPedus’ “Extending the IC Roadmap” with An Steegen’s comments at

• Brian Bailey’s “Design for Advanced Packaging” at
  https://semiengineering.com/design-for-advanced-packaging/

• Herb Reiter’s “The Great Divide Between Semiconductor Design and Manufacturing”
  https://www.3dincites.com/2016/08/the-great-divide-between-semiconductor-design-and-manufacturing/