



Government Investment in Heterogeneous Integration

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 **Innovate Forward**

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100 YEARS

Government Investment in Heterogeneous Integration

- Past
 - Background and history
 - DAHI (Diverse Accessible Heterogeneous Integration)
- Present
 - CHIPS (Common Heterogeneous Integration and IP Reuse Strategies)
 - ERI (Electronics Resurgence Initiative)
- Future
 - Security and Trust Issues
 - MINSEC (Microelectronics Innovation for National Security and Economic Competitiveness)
 - SHIP (State of the art Heterogeneous Integrated Packaging)



Past



No "Perfect" Material

		← device materials →					integration
Parameter	Why?	Unit	Si	GaAs	InP ¹	GaN ²	COSMOS / DAHI
Electron Mobility	Carrier velocity	10 ³ cm ² /V·s	1.4	8.5	12	<1	InP
V_{peak}	Transit time	10 ⁷ cm/s	1	2	2.5	2.5	InP / GaN
E_{BK}	Voltage swing	10 ⁵ V/cm	5.7	6.4	4	40	GaN
E_g	Charge density	eV	1.12	1.42	0.74	3.4	GaN
κ	Heat removal	W/cm·K	1.3	0.5	0.05	2.9	GaN / Si
Maturity	Circuit complexity		Excellent	Good	OK	Limited	Si + GaN + InP (heterogeneous)
DARPA Investment			~\$100M	~\$600M	~\$200M	~\$300M	~\$180M
Programs			Portions of GRATE, ADRT, LPE, and TEAM	MIMIC	SWIFT, TFAST, THz Electronics, SMART	GaN Title III, WBGSRF, NEXT, MPC, NJTT	COSMOS, DAHI

Materials and device parameters favor a diversity of semiconductors

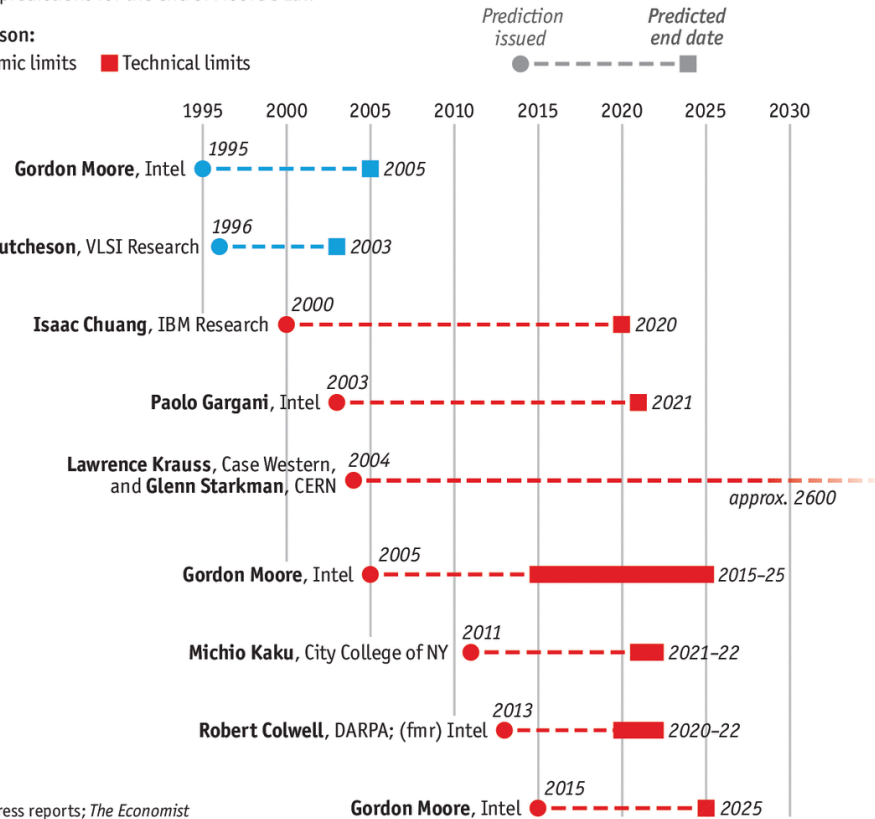
1. InGaAs channel
2. SiC substrate

Faith no Moore

Selected predictions for the end of Moore's Law

Cited reason:

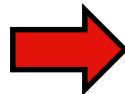
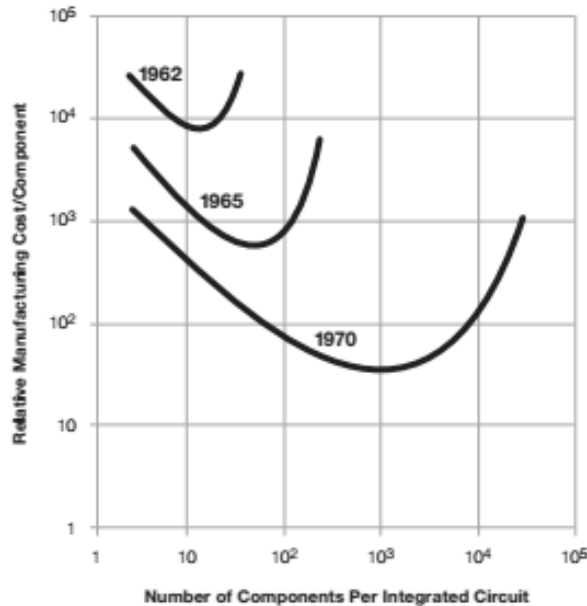
■ Economic limits ■ Technical limits



Sources: Press reports; *The Economist*

Economist.com

Moore's Law



Changes in silicon industry will be felt by compound semiconductors



Moore's paper INCLUDES Heterogeneous Integration

It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected. The availability of large functions, combined with functional design and construction, should allow the manufacturer of large systems to design and construct a considerable variety of equipment both rapidly and economically.

The experts look ahead

Cramming more components onto integrated circuits

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

By Gordon E. Moore

Director, Research and Development Laboratories, Fairchild Semiconductor Division of Fairchild Camera and Instrument Corp.

The field of integrated electronics is the focus of electronics itself. The advantages of integration will see a proliferation of electronics, pushing this science into many new areas.

Integrated circuits will lead to such wonders as heart computers—or at least terminals connected to central computers—automatic controls for automobiles, and personal portable communications equipment. The electronic revolution is only a decade to be lived.

One of the biggest potential lies in the production of large systems. In telephone communications, integrated circuits in digital filters will separate channels in complex equipment. Integrated circuits will also switch telephone circuits and perform data processing.

Computers will become powerful, and will be organized in completely different ways. For example, massive banks of integrated electronics may be distributed throughout the

room instead of being concentrated in a central cabinet. The improved reliability made possible by circuits will allow the construction of larger systems. Machines used for those in existence today will have one or two with their own second.

Present and future

The integrated electronics, I mean all the silicon chips which are referred to as microcircuits, will see an additional one that results in a cost that is applied to the same as individual silicon chips. It was first investigated in the late 1950s just as the microcircuit electronics equipment is currently complex electronic functions in their minimum weight. Several approaches evolved, reasonably techniques for individual component functions and semiconductor integrated circuit approaches.

Each approach arrived rapidly and cost with such borrowed techniques from another. Many believe the way of the future is a combination of approaches.

The advantages of semiconductor integrated circuits using the improved characteristics of silicon by applying such films directly to a silicon substrate. These advances in technology are now developing sophisticated techniques in most of the semiconductor industries in the present.

Such approaches have varied with cost and are in equipment today.

Electronics, Volume 38, Number 8, April 19, 1965

The establishment

Integrated electronics is established today. The techniques are almost mandatory for new military systems, since the reliability, size and weight required by some of these is achievable only with integration. Study programs at Apple, for example, have shown how to make the reliability of integrated electronics by showing that complete circuit designs are as fast as those in the best individual manufacturers.

Microcomputers in the commercial computer field have machines in design or in early production employing integrated electronics. These machines cost less and perform better than those which use "conventional" electronics. Experiments of various sorts, especially the rapidly increasing number employing digital techniques, are starting to see integration become a vital part of both manufacturing and design.

The use of linear integrated circuitry is still restricted primarily to the military. Such integrated functions are expensive and not available in the variety required to make a major fraction of linear electronics. But the first applications are beginning to appear in commercial electronics, particularly in equipment which needs low-frequency amplification of small size.

Reliability costs

In almost every case, integrated electronics has demonstrated high reliability. Even at the present level of production—low compared to that of discrete components—it offers reduced system cost, and in many systems improved performance has been realized.

Integrated electronics will make electronic techniques more generally available throughout all of society, performing more functions that practice is not adequately met by other techniques or not done at all. The principal advantages will be lower cost and greatly simplified design—especially from a ready supply of low-cost functional packages.

For most applications, semiconductor integrated circuits will predominate. Semiconductor devices are the only reasonable candidates presently in existence for the active elements of integrated circuits. Passive semiconductor elements look attractive too, because of their potential for low cost and high reliability, but they can be used only if practice is not a prime requisite.

Silicon is likely to remain the basic material, although others will be of use in specific applications. For example, gallium arsenide will be important in the ground environment. Band-gap, the silicon will predominate at lower frequencies because of the technology which has already evolved around it and its wide application. It is an abundant and relatively inexpensive starting material.

Costs and curves

Reduced cost is one of the big attractions of integrated electronics, and the cost advantage continues to increase as the technology evolves. The production of larger and larger circuit functions on a single silicon chip is obvious. For example, a single, third-generation assembly recently prepared for the number of components, the result of the

equivalent price of semiconductor in the equivalent package containing more components. The as components are added, the circuit yields more than components for the complexity, tending to make the cost per component decrease a minimum cost every generation to the cost of the technology. At present, it is reached when 30 units are used per circuit, but the minimum is being achieved by the end of second generation, being over graphically look about five years, a plot of cost suggests that if

mean cost per component might be expected to rise about 1,000 components per circuit (including and functions can be produced in moderate quantities, if the manufacturing cost per component can be kept only a tenth of the present cost.

The complexity for minimum component cost, counted at a rate of roughly a factor of two per generation (not per year). Certainly over the short term can be expected to continue, if not to increase. I doubt that the rate of increase is a bit more rapid than that in a second generation, but it is not constant for most 10 years. The trend by 1975, 10 years of components per integrated circuit for minimum cost is 65,000.

I believe that such a large circuit can be built on a single chip.

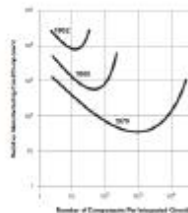
Two- and three-dimensional

With the dimensional reduction already being used in integrated circuits, reduced high performance can be built in a system to the thousands of an inch square.

On the silicon wafer currently used, used by an inch or more in diameter, there is ample room for such a structure if the components can be closely packed with no space wasted for interconnection patterns. This is possible, since efforts to achieve a level of complexity above the present level (table integrated circuits) are already underway using multilayer metalization patterns deposited by automatic means. Such a density of components can be achieved by present optical techniques and does not require the more exact techniques, such as electron beam exposures, which are being studied to make even smaller structures.

Increasing the yield

There is no fundamental obstacle to achieving device yields of 100%. At present, packaging costs are the second most of the manufacturing structure itself that there is no incentive to improve yields, but they can be raised to high



Electronics, Volume 38, Number 8, April 19, 1965

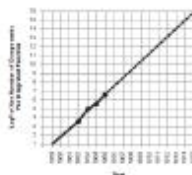


A two-inch square area also contains several thousands of microcircuits or a few diodes. This allows at least 500 components per linear inch or a quarter million per square inch. Thus, 65,000 components need occupy only about one-tenth a square inch.

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It is economically justified. The interconnection equipment, it is not even necessary to do any fundamental research to replace present processes. Only the engineering effort is needed.

In the early days of integrated electronics, when yields were extremely low, the cost of integrated circuits was high compared with those obtained on individual electronic devices. The same pattern will make integrated electronics economical, if other conditions make such units desirable.

Power problems

SPIC will be possible to overcome the heat generated by tens of thousands of components in a single silicon chip? If we could shrink the size of the components themselves, we could expect to dissipate heat. But it will happen with integrated circuits. Since integrated electronics are two-dimensional, they have a surface area of heat generation. Heat dissipation, power is needed primarily in three dimensions. As long as a silicon chip is confined to a small area on a wafer, the amount of heat-dissipating dimensions on integrated structures is restricted. It is possible to operate the structure at higher speed for the same power per unit area.

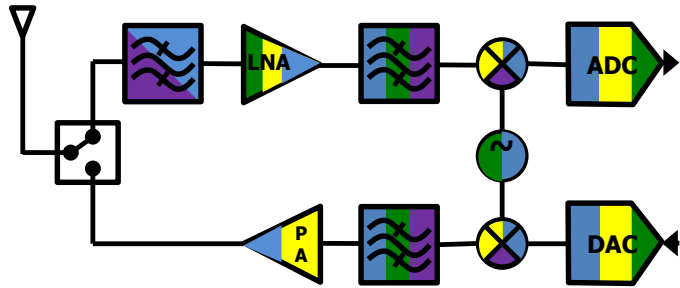
Cost of packaging

Clearly, we will be able to build such component-integrated equipment. Now, we ask under what circumstances we should do it. The cost of making a particular system function must be minimized. To do so, we could simulate the engineering over the assembly of large functions so that as disproportionate cost has been borne by a particular army. Perhaps newly devised design systems to procedures could be used to speed up the engineering process. It may prove to be more economical to build large

G. E. Moore is one of the new breed of electronic engineers, schooled in the physical sciences rather than in electronics. He earned a B.S. degree in chemistry from the University of California and a Ph.D. degree in physical chemistry from the California Institute of Technology. He was one of the founders of Fairchild Semiconductor and has been Director of the research and development laboratories since 1959.

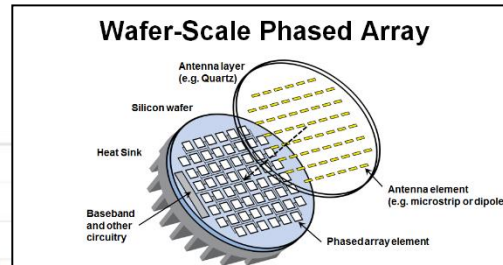
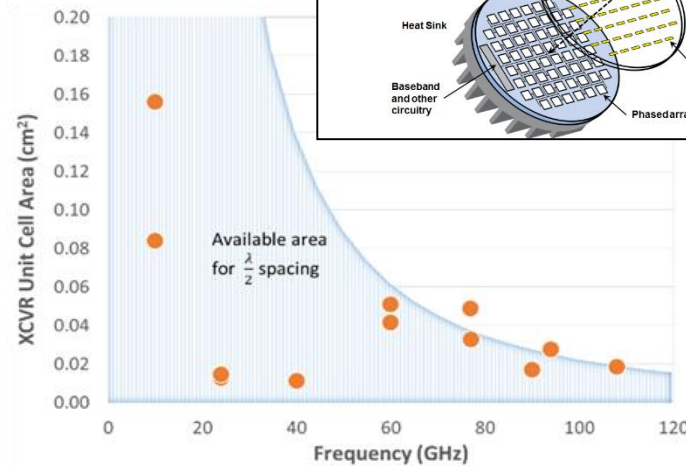


Why Heterogeneous Integration?

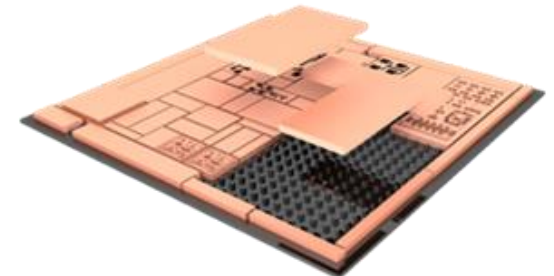


- Si CMOS/SiGe BiCMOS
- InP HBTs/HEMTs
- GaN HEMTs
- RF MEMS/High-Q passives

Best of breed technology



Density of integration

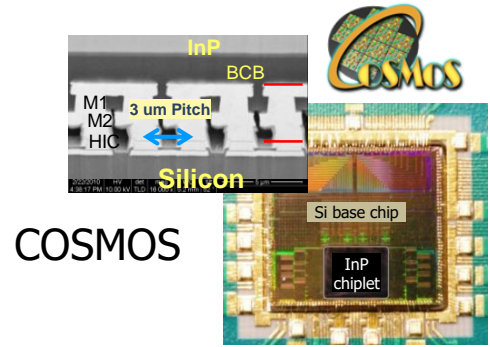
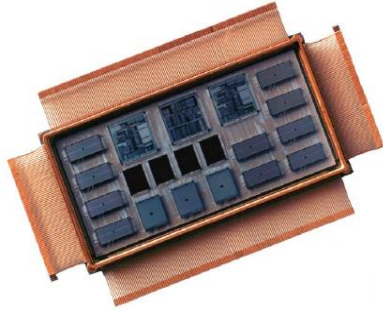


Modular design

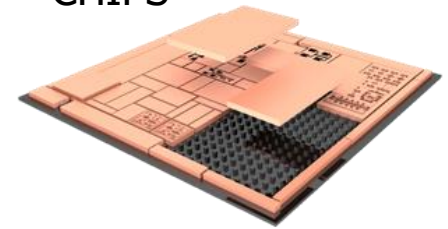


DARPA's long history of innovation in integration

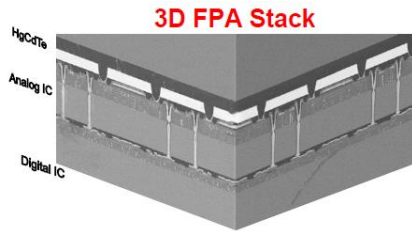
ASEM



CHIPS



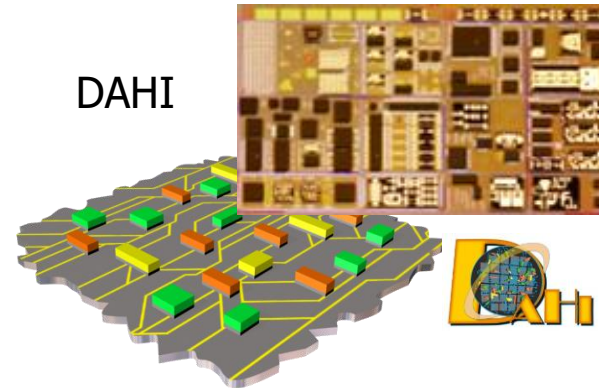
VISA



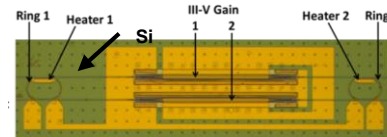
3D-IC



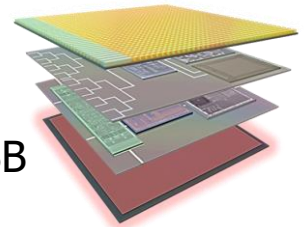
DAHI



E-PHI



MOABB



- ASEM: Application Specific Electronic Modules
- E-PHI: Electronic-Photonic Heterogeneous Integration
- VISA: Vertically Integrated Sensor Arrays
- COSMOS: Compound Semiconductor Materials on Silicon
- DAHI: Diverse Accessible Heterogeneous Integration
- MOABB: Modular Optical Aperture Building Blocks
- CHIPS: Common Heterogeneous Integration and IP Reuse Strategies

1990s

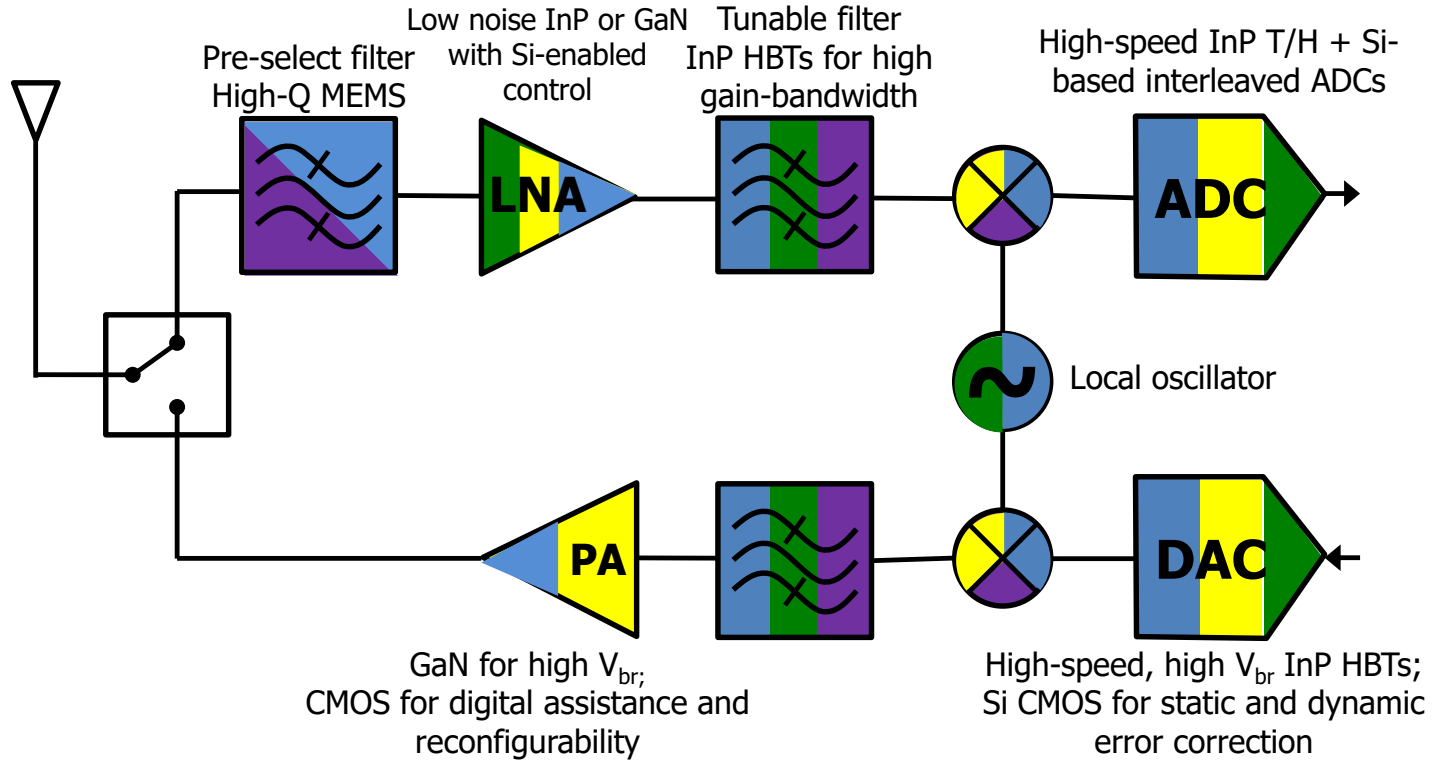
2000s

2010s

2020s



Vision for Representative Transceiver: 4+ Device Technologies

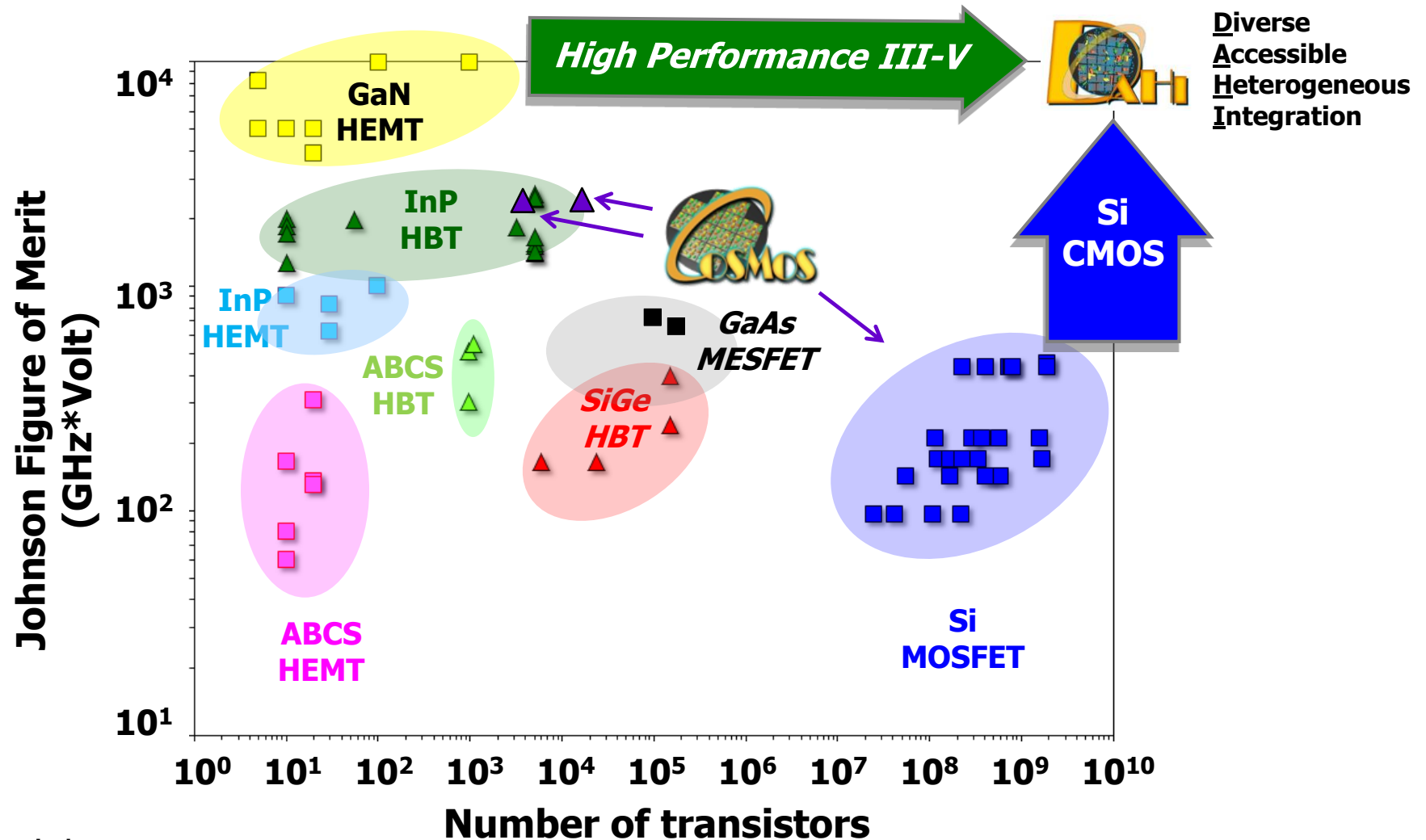


Legend:

- Si CMOS/SiGe BiCMOS
- InP HBTs/HEMTs
- GaN HEMTs
- RF MEMS/High-Q passives



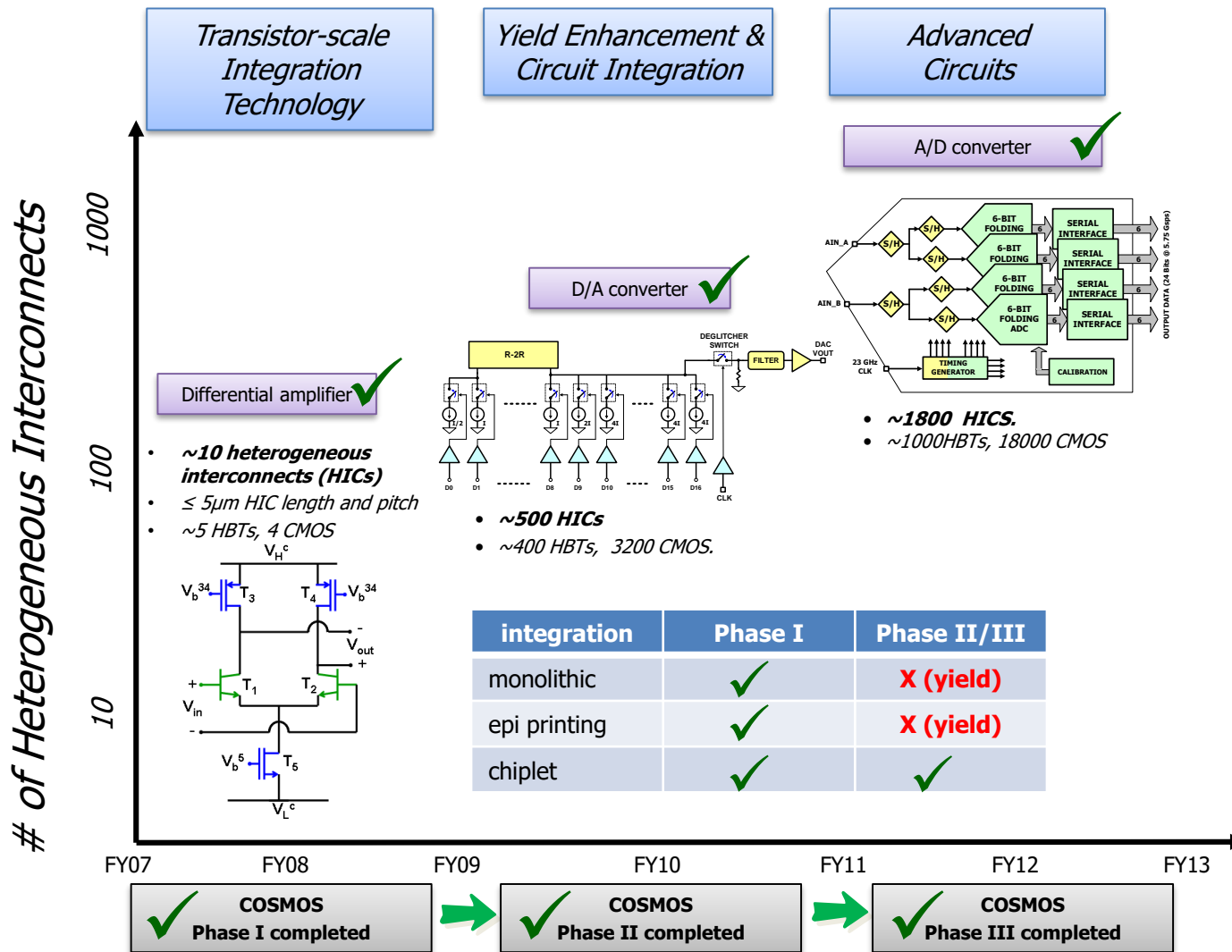
Heterogeneous Integration: DAHI Broadens the Device Material Options



Terminology:

InP = indium phosphide, GaN = gallium nitride, SiGe = silicon germanium, ABCS = antimonide-based compound semiconductor
HBT = heterojunction bipolar transistor, HEMT = high electron mobility transistor, CMOS = complementary metal oxide semiconductor
COSMOS = Compound Semiconductor Materials on Silicon

COSMOS Program Showed the Promise of Heterogeneous Integration



COSMOS¹:

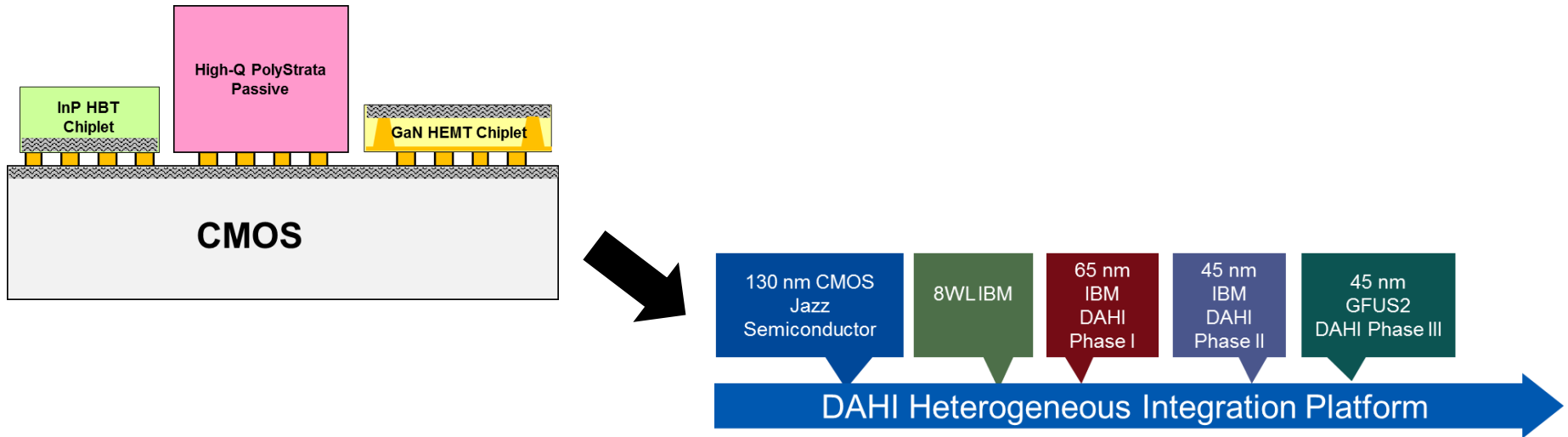
1. Developed technology for intimate integration of III-Vs and Si.
2. Demonstrated world-record capabilities with heterogeneous circuits:
 - a. Differential amplifier gain-bandwidth
 - b. DAC SFDR
3. Clarified benefits of integration processes that:
 - a. are scalable,
 - b. use finished devices, and
 - c. leverage industry efforts.

¹Compound Semiconductor Materials on Silicon

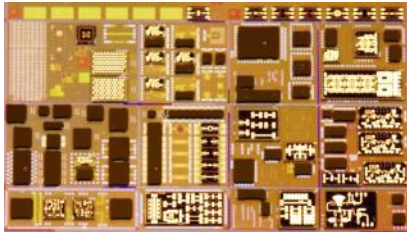
Phase II/III: Demonstrated benefits of integration of completed devices.



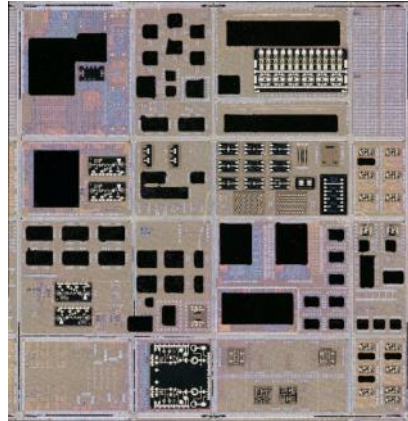
DARPA's DAHI program: Silicon CMOS as integration platform



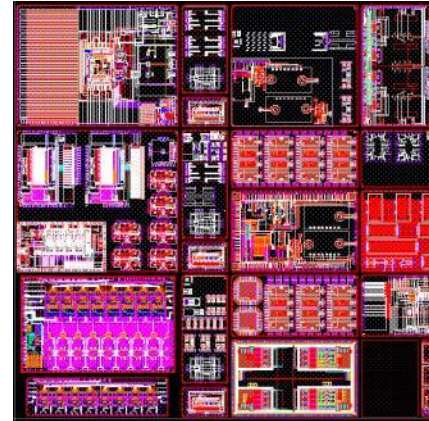
MPW0



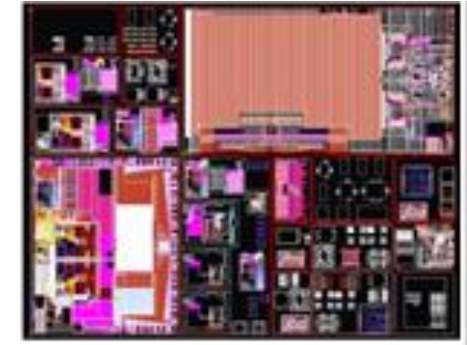
MPW1



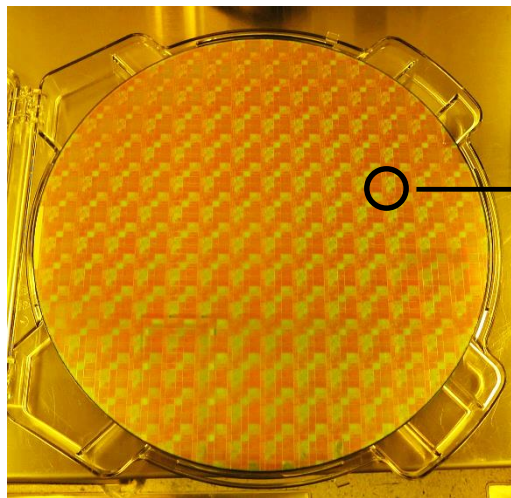
MPW2



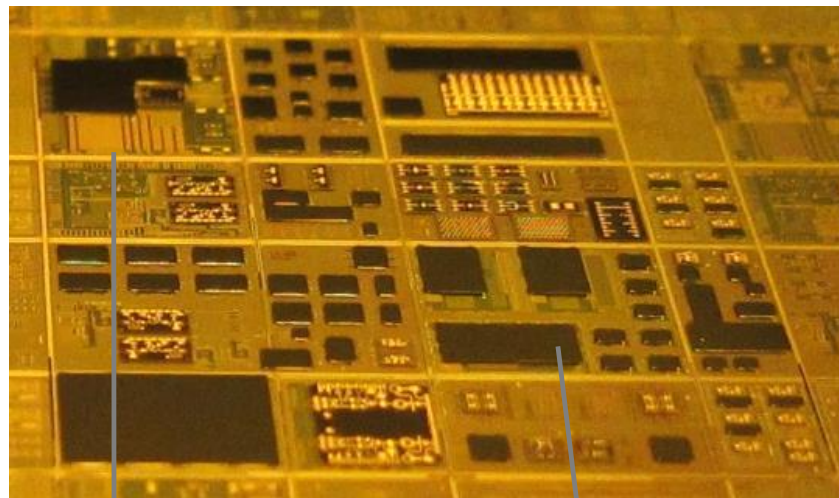
MPW3



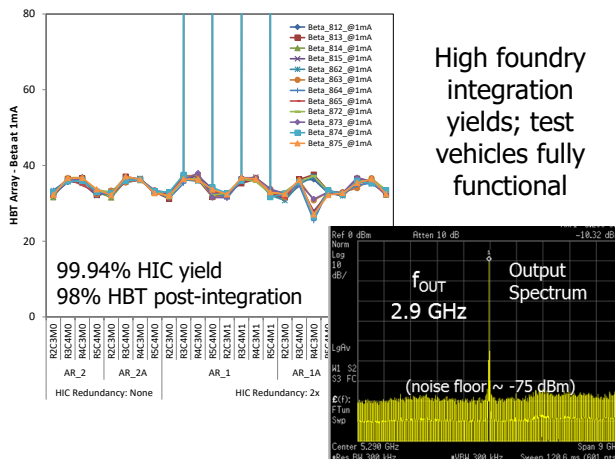
DAHI snapshot: Excellent yield, demonstrated RF performance



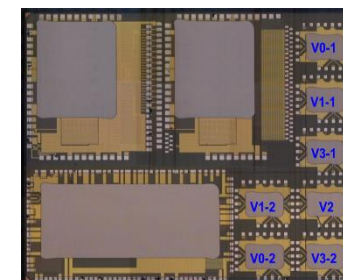
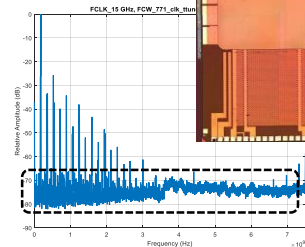
300mm diameter Si CMOS wafer (45nm node)



DAHI integration: Si (45nm), InP (TF5 HBT), GaN (GaN20 HEMT)



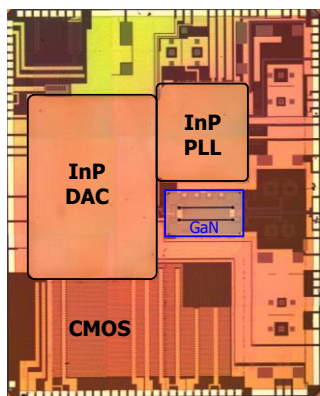
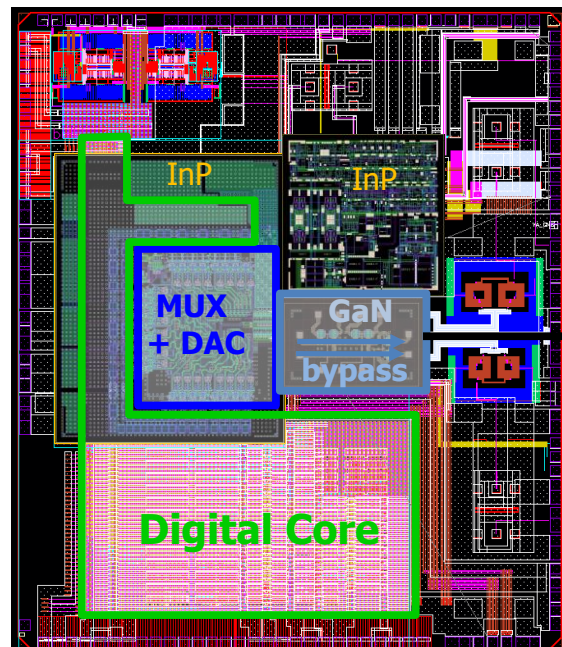
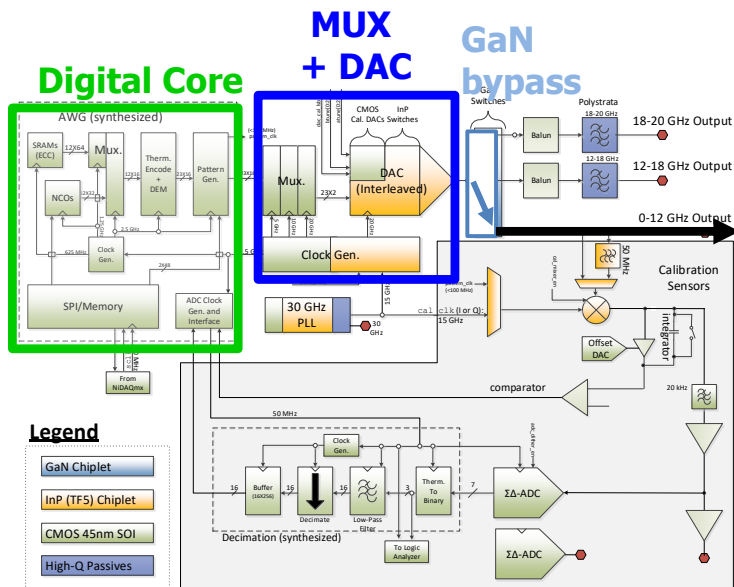
DAC with very low digital noise (-70dBc)



Successful testing identified optimal S/H circuit for ADC (>65dB SFDR @ 2GHz)

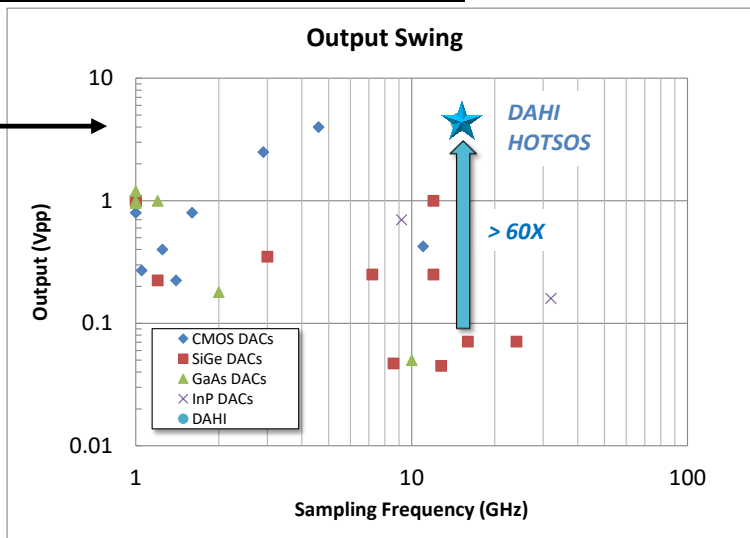
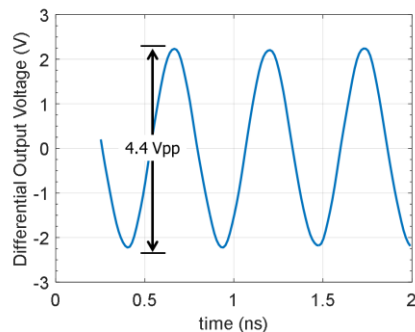
Sources: DARPA, Northrop Grumman

DAHI MPW1: Arbitrary Waveform Generator Enabled by Heterogeneity



InP + GaN + Si CMOS

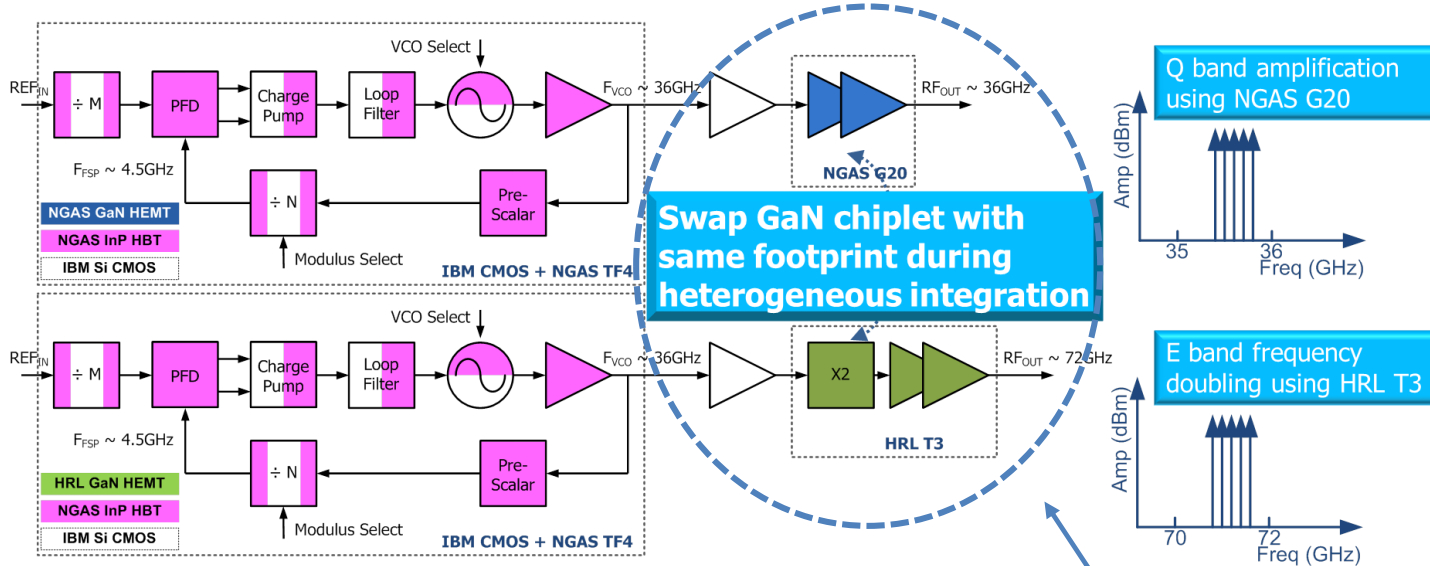
Heterogeneous integration enables unprecedented output swing





DAHI MPW1: Dual-Band Frequency Synthesizer Demonstrates Modularity

MPW1 Q/E Dual Band Frequency Synthesizer (36 and 72 GHz)

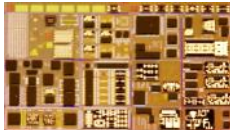
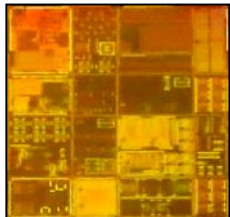
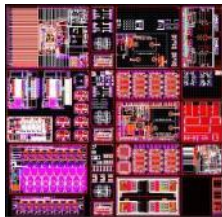
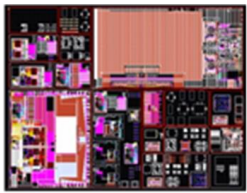


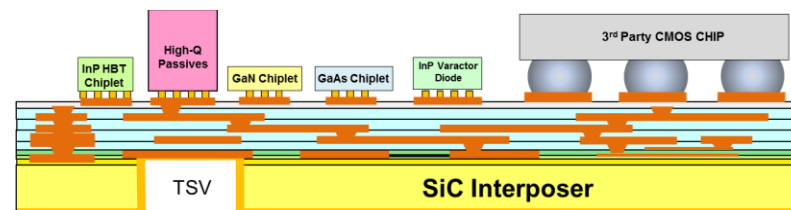
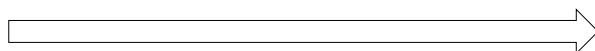
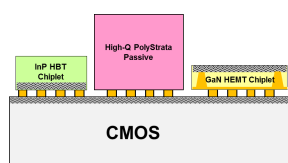
		Technology				
	Function	Freq (GHz)	CMOS 12SOI	InP TF4	GaN G20	GaN T3
A	Amplifier	36			✓	
	Frequency Doubler	72				✓
B	Buffer	36	✓			
C	Buffer + Amp	36	✓		✓	
	Buffer + FD	72				✓
D	VCO + Buffer + Amp	36	✓	✓	✓	
	VCO + Buffer + FD	72	✓	✓		✓
E	Frequency Synthesizer	36	✓	✓	✓	
	Frequency Synthesizer	72	✓	✓		✓

Integration of diverse device technologies enables modular functionality.

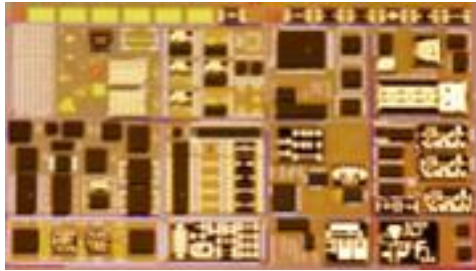


DAHI simplicity enables rapid evolution

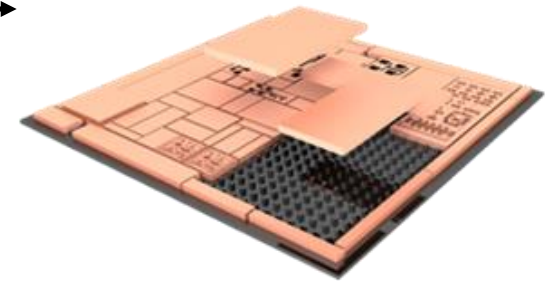
Technology	MPW0	MPW1	MPW2	MPW3	Future MPWs
CMOS	IBM 65nm	GF 45 nm	GF 45 nm	GF 45 nm	GF 45 nm
InP HBT	TF4 (2 metals)	TF4 (3 metals)	TF4 (4 metals)	TF4 (4 metals)	TF4 (4 metals)
		TF5 (3 metals)	TF5 (4 metals)	TF5 (4 metals)	TF5 (4 metals)
InP Varactor Diode					AD1
GaN HEMT	GaN20	GaN20	GaN20	GaN20	GaN20
	T3 (HRL)	T3 (HRL)	T3 (HRL)	T3 (HRL)	T3 (HRL)
GaAs HEMT				P3K6	P3K6
Passive Components		PolyStrata (Nuvotronics)	PolyStrata (Nuvotronics)	PolyStrata (Nuvotronics)	PolyStrata (Nuvotronics)
Base Substrate	CMOS	CMOS	CMOS	CMOS	CMOS
				SiC (IWP5)	SiC (IWP5)
					(in design)



Sources: DARPA, Northrop Grumman



CHIPS: modular design

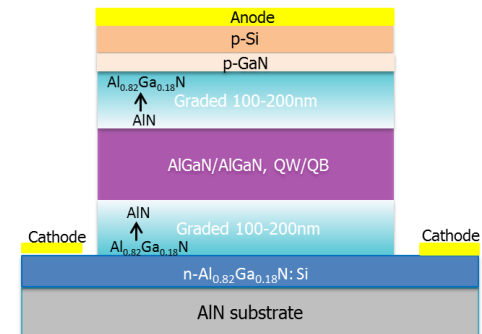
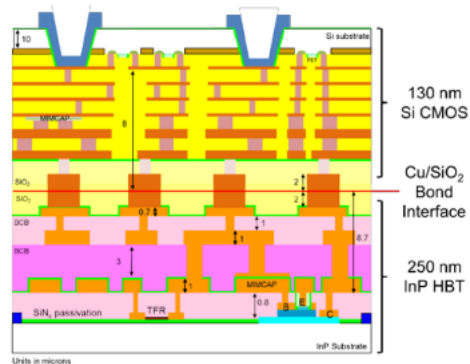


Heterogeneous devices

DAHI: RF power



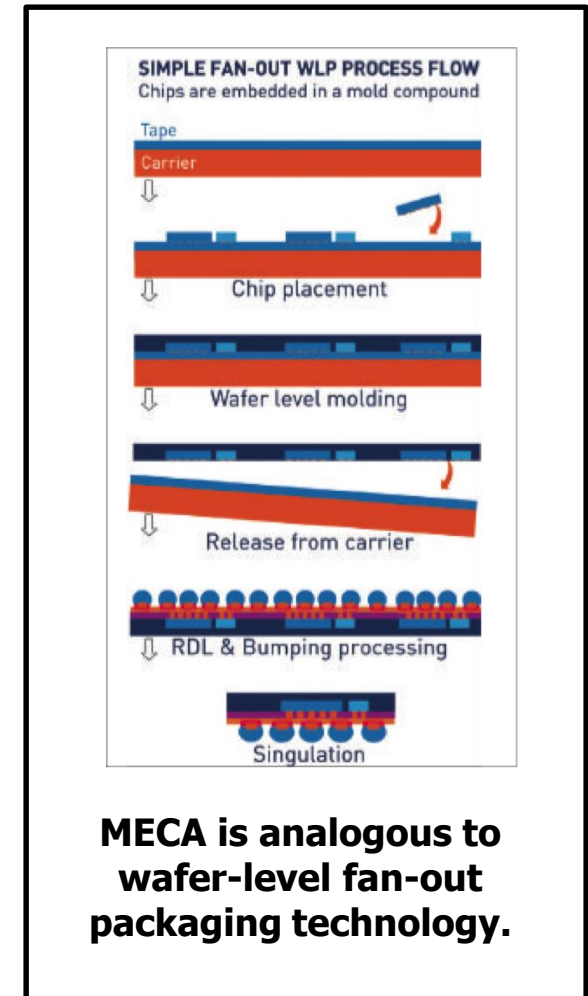
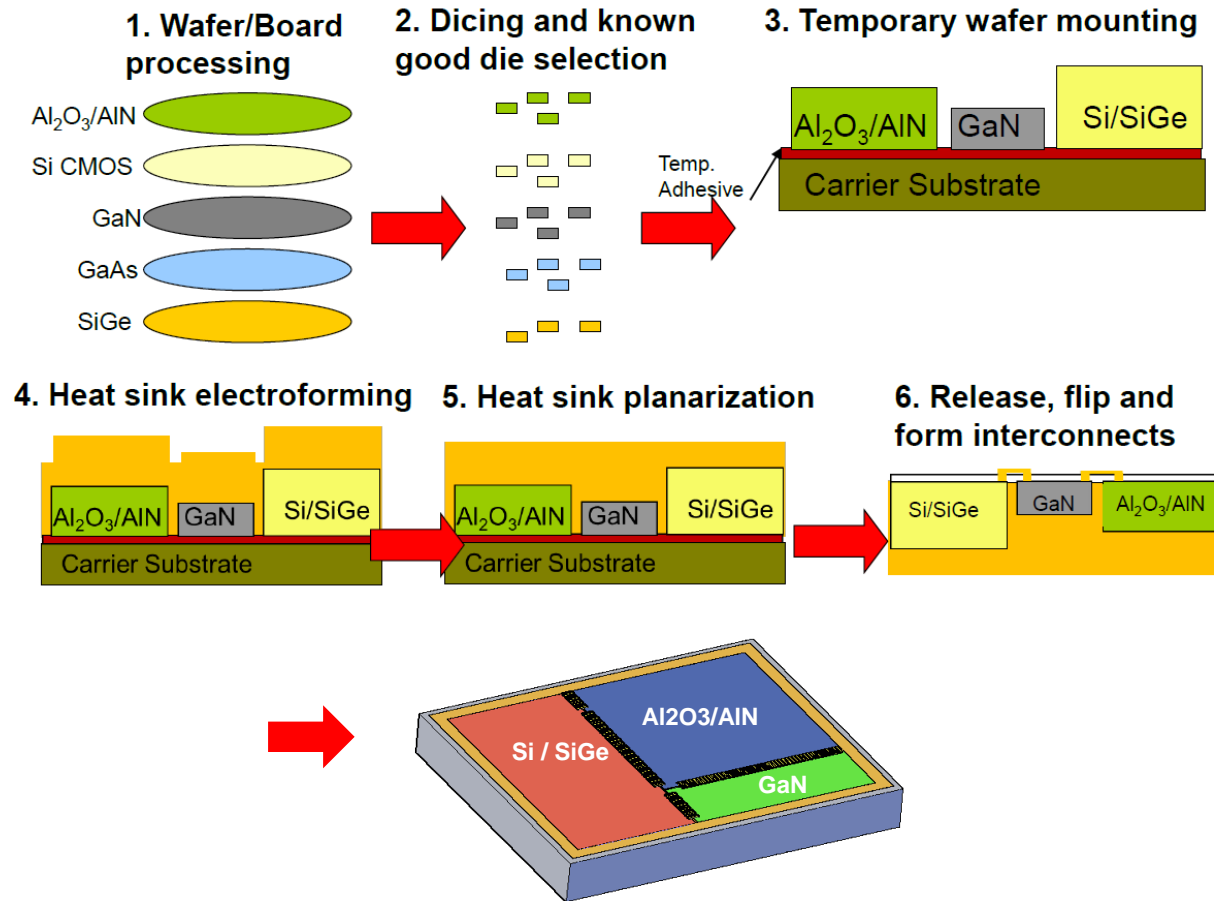
DAHI: wafer scale





Metal Embedded Chip Assembly (MECA)

MECA enables heterogeneous integration with a metal interconnect platform for high-power requirements.

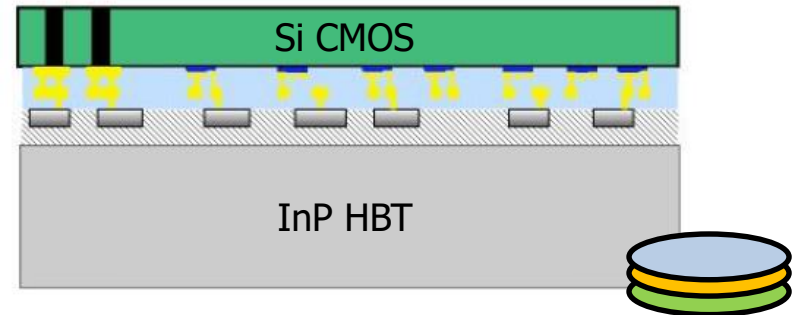


Sources: HRL, Solid State Technology

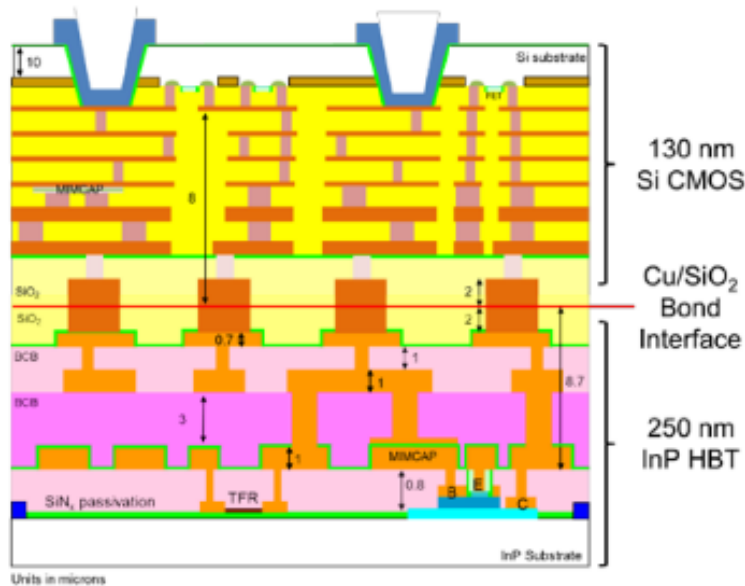
Heterogeneous integration for mm-wave: Phased array beamformers

- Can maintain $\lambda/2$ channel spacing as frequencies increase
- CMOS control circuitry closely integrated with RF chain
- Improved channel performance and efficiency with addition of III-V devices
- Fully integrated beamformer channels demonstrated with integrated InP devices and Si control electronics
- >100mW Pout Tx channel, 4.5 dB NF Rx

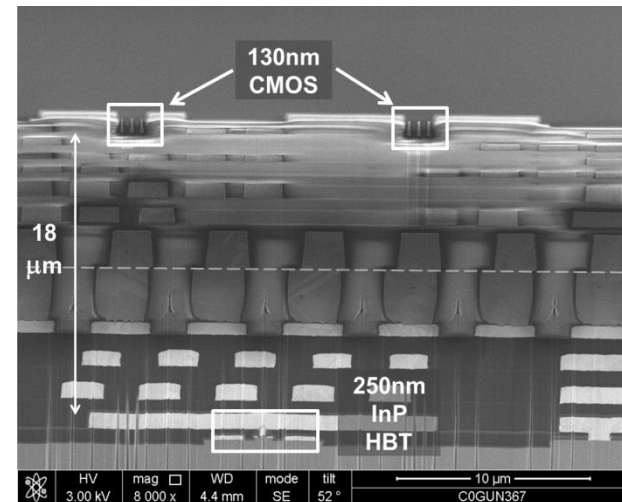
Wafer-level heterogeneous integration



Integration schematic

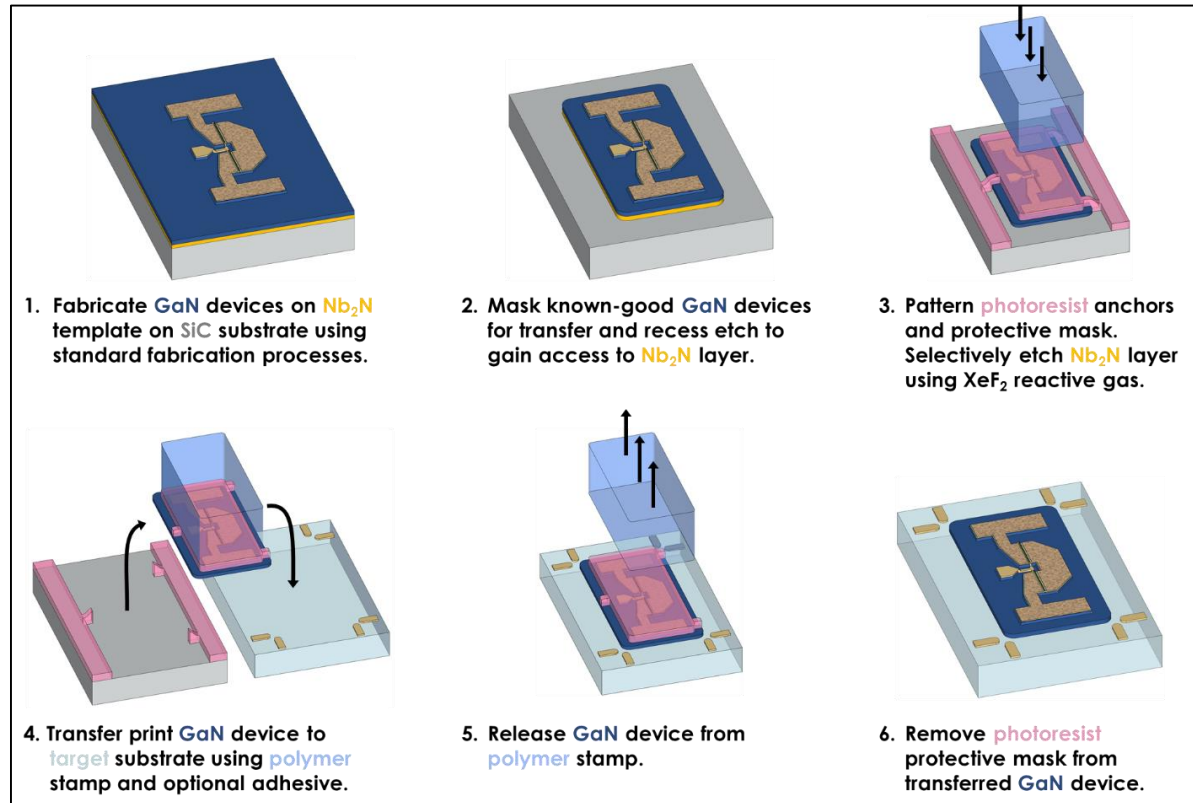
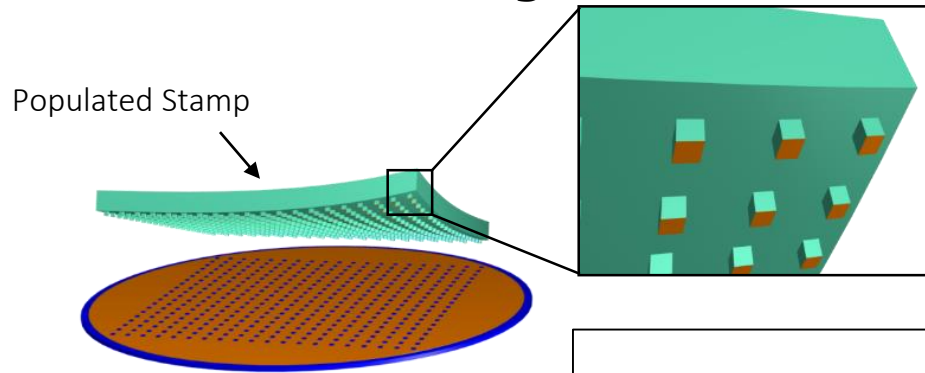


InP/CMOS with DBI Process



DBI = Direct Bond Interconnect

Microtransfer Printing

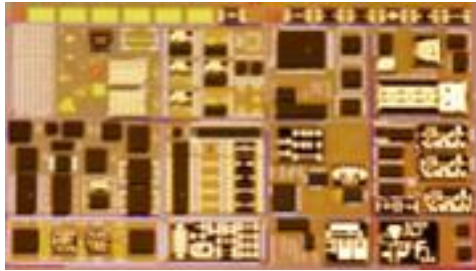




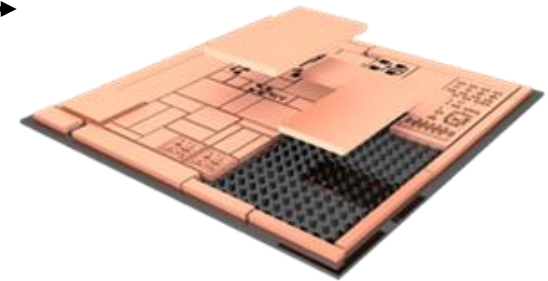
Present



Common Heterogeneous Integration and IP Reuse Strategies: CHIPS as the next step in heterogeneous integration



CHIPS: modular design



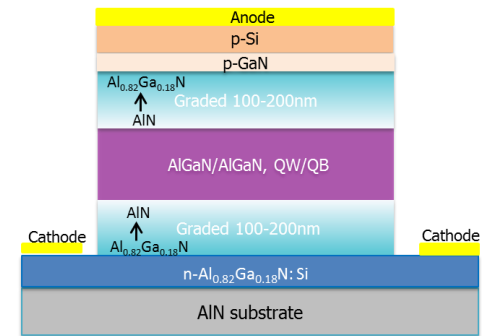
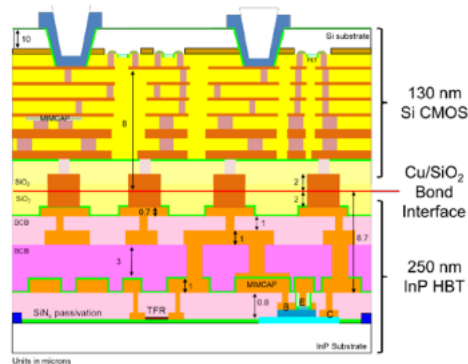
Integration technologies

Heterogeneous devices

DAHI: RF power



DAHI: wafer scale





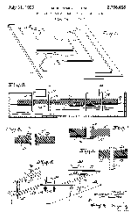
"Printed circuit board" invented by Paul Eisler.



Early PCB demo in a radio.



First HVM PCBs enable proximity fuze during WWII.



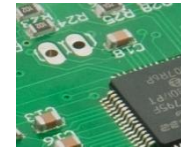
Patent to US Army for PCB assembly.



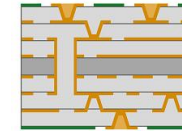
IPC (Institute for Printed Circuits) founded; standards follow.



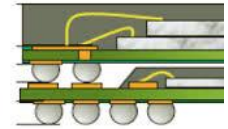
Image: Intel Multi-layer PCB invented.



Surface Mount Technology on PCBs revolutionizes manufacturing.



HDI / Microvia technology enables further integration.

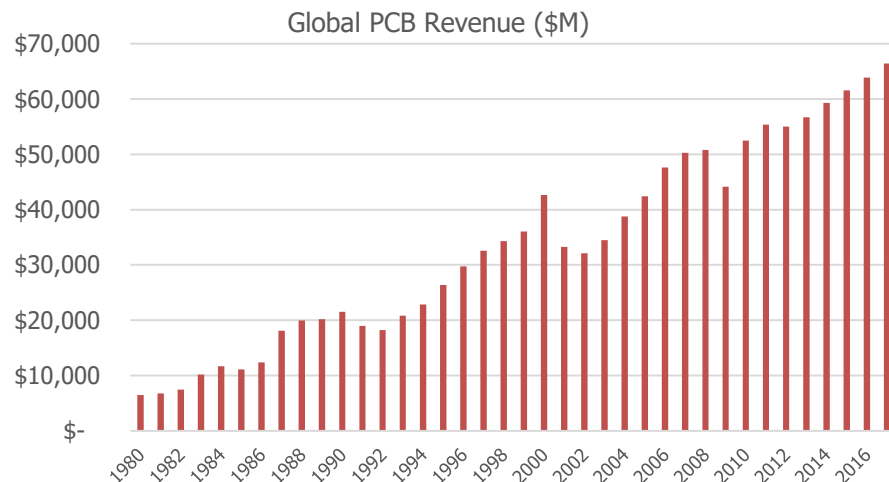


First package-on-package standard from JEDEC

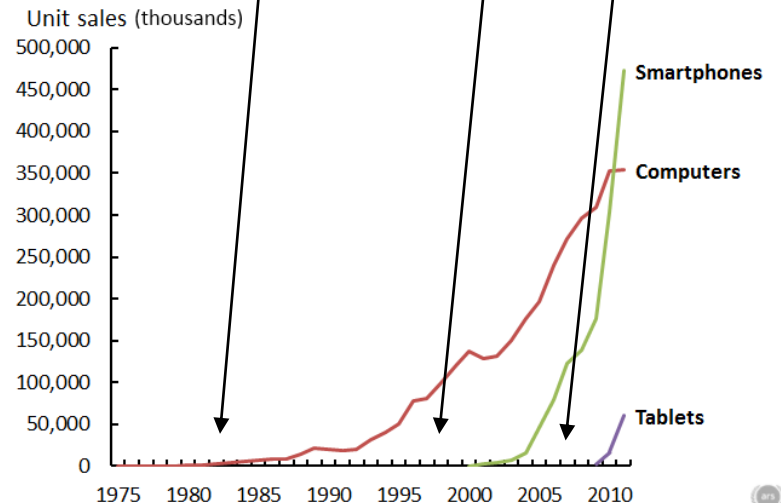
DoD jump-start

1936 1941 1943 1956 1957 1960 1980s 1995 2006

PCB industry sees steady expansion with DoD origins, standardization, and technology development.

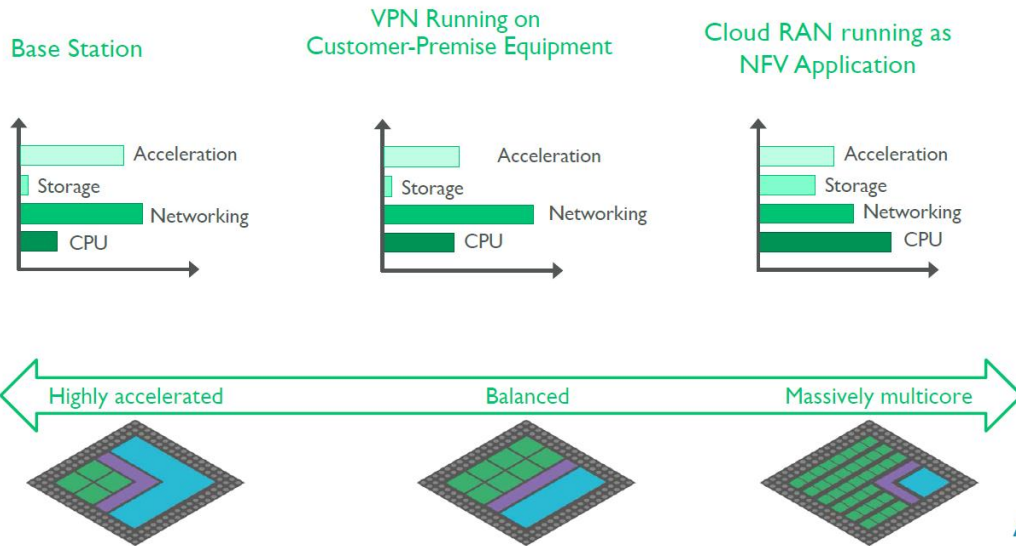


Computers, smartphones, and tablet sales: 1975-2011

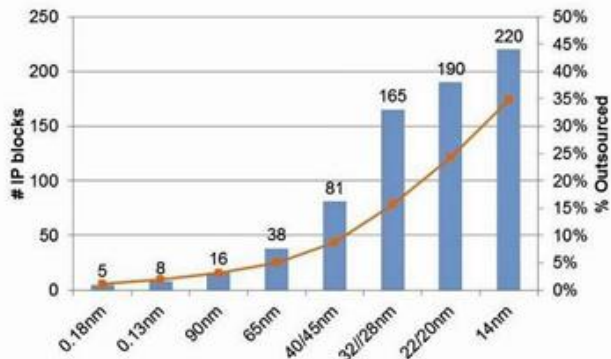
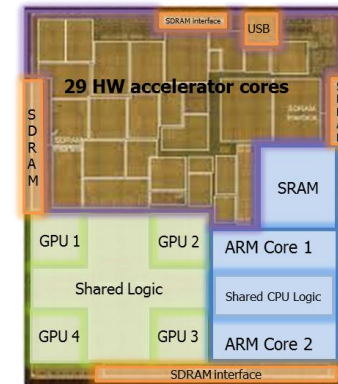


IP business model is based on chip modularity

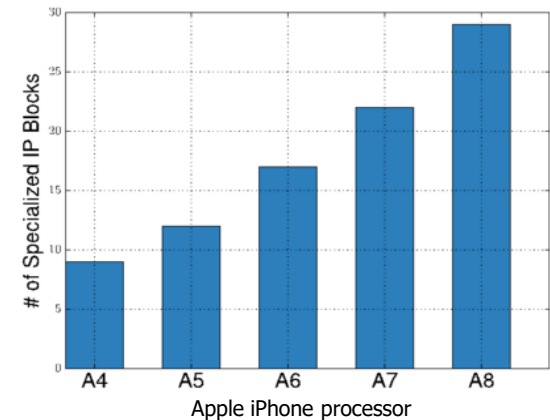
Analysing workloads to optimize the SOC



Apple A8



IP usage grows with node progress and design updates.

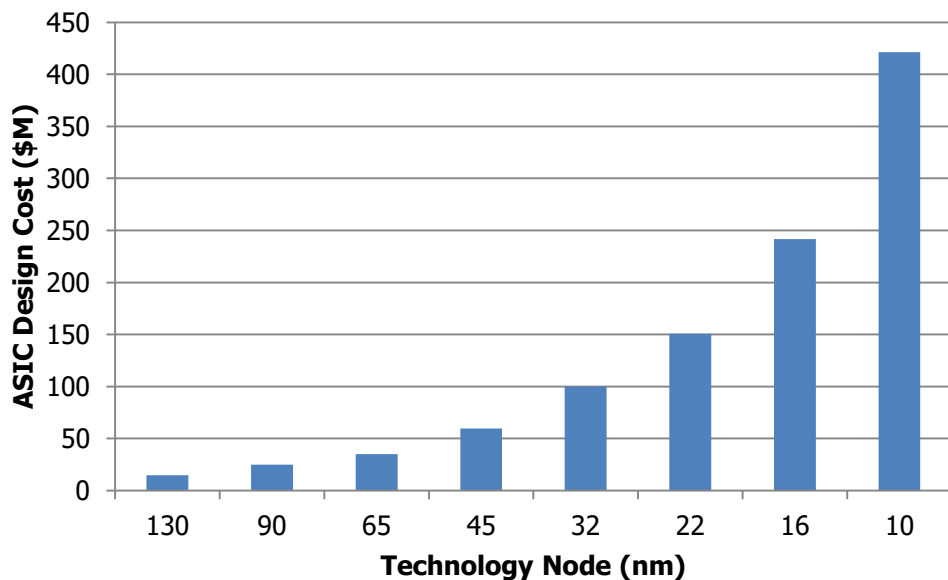


Modular semiconductor IP reduces chip design effort (time AND cost)



But Advanced Si is Still Expensive to Design and Fab

Expensive to design at advanced nodes ...



... which some commercial products can support ...



© apple.com

Fab cost for commercial electronics amortized over **one day's** worth of iPhones

... but DoD cannot.

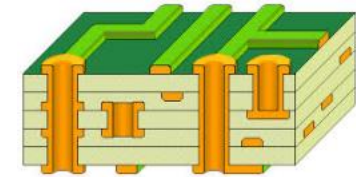
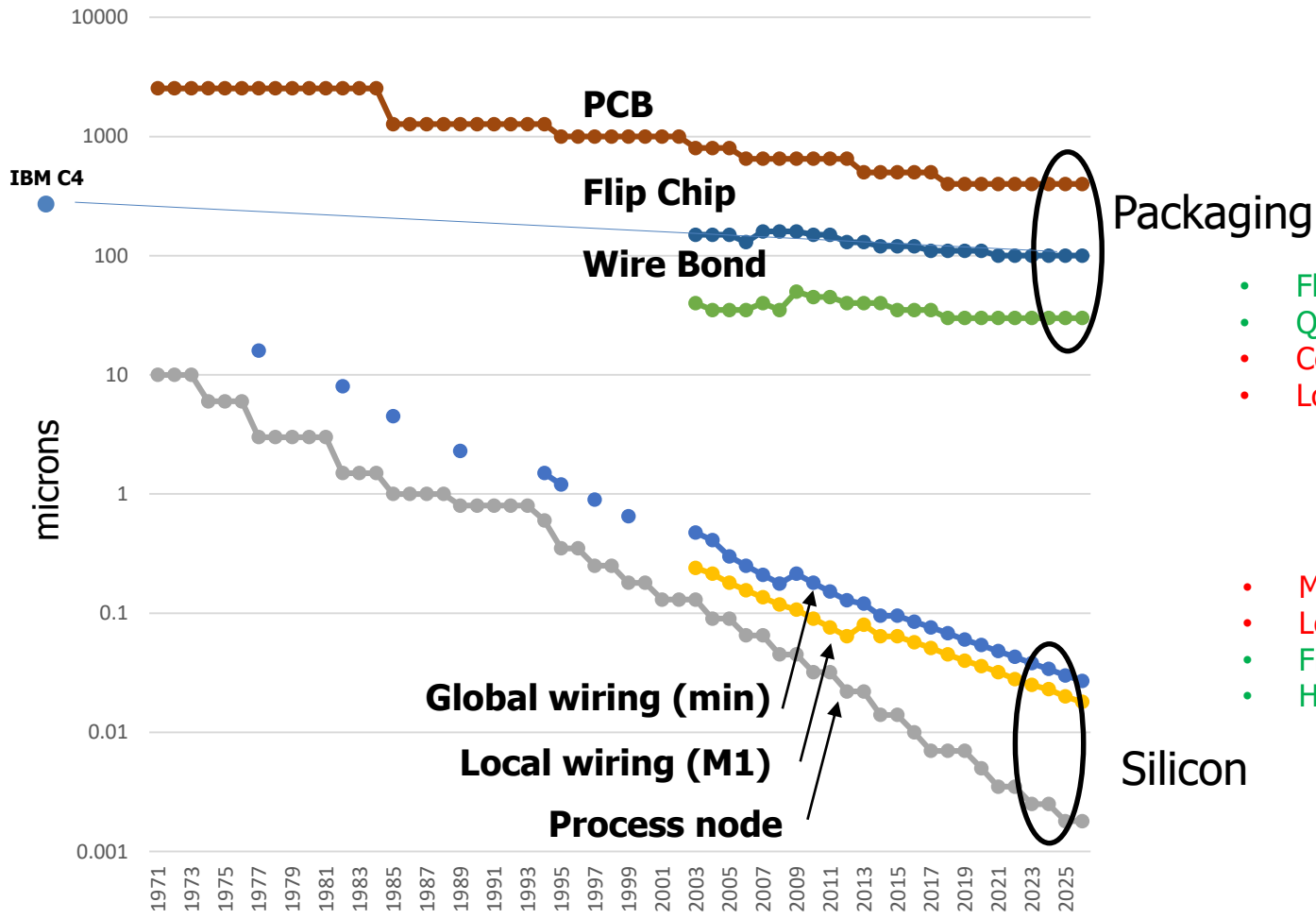


Fab cost for a DoD IC amortized over **entire 29 year** acquisition of JSF

Source: "Cashing in with Chips" AlixPartners Semiconductor R&D outlook report, 2014.



Conventional Assembly Has Attractive Features Too ... But Isn't Keeping Up on Pitch and Performance



- Flexible heterogeneous integration
- Quick design / manufacturing turns
- Coarse pitch
- Lower performance

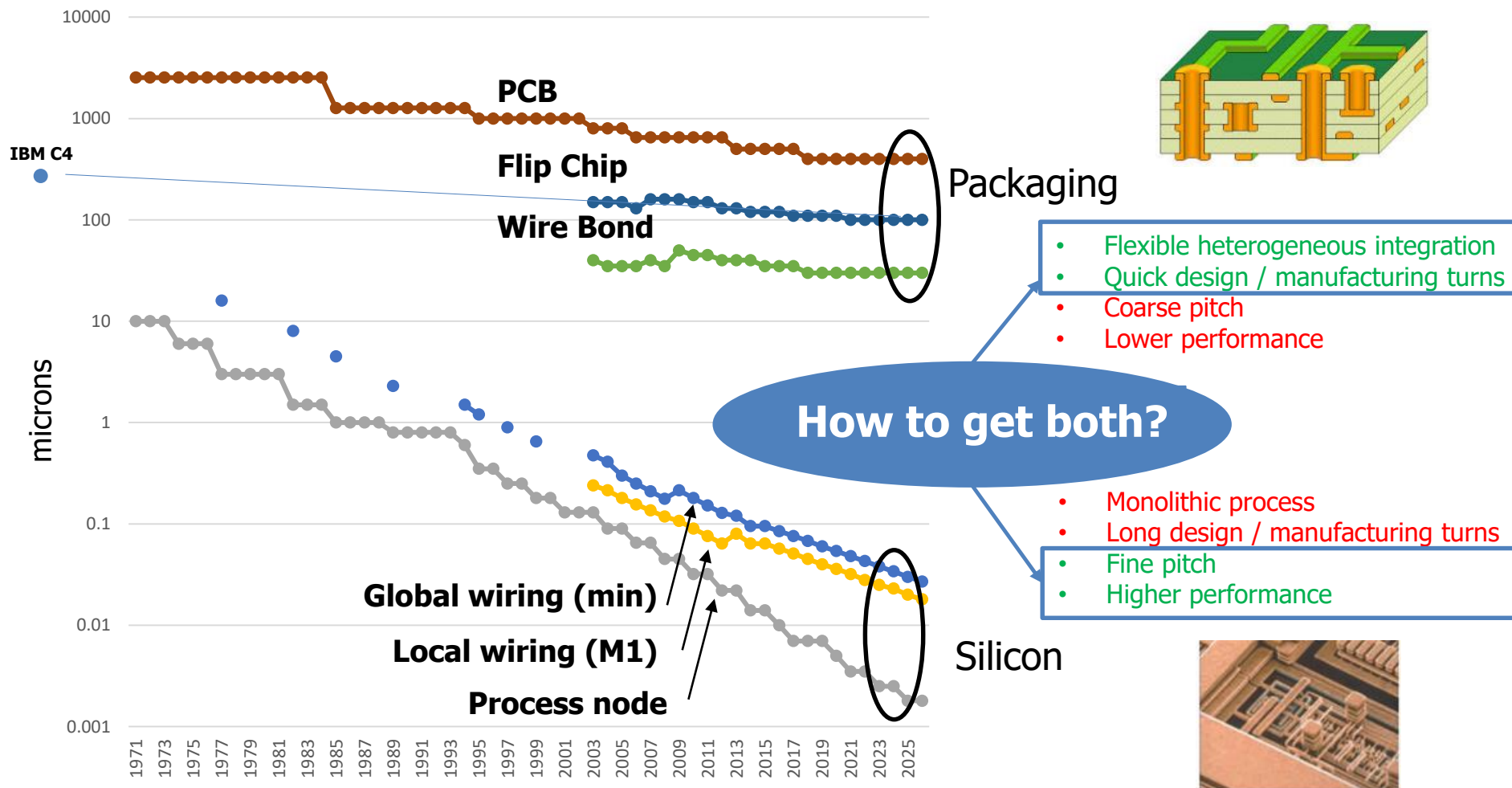
- Monolithic process
- Long design / manufacturing turns
- Fine pitch
- Higher performance



Need to combine speed and flexibility of packaging with pitch and performance of advanced heterogeneous device technology.



Conventional Assembly Has Attractive Features Too ... But Isn't Keeping Up on Pitch and Performance

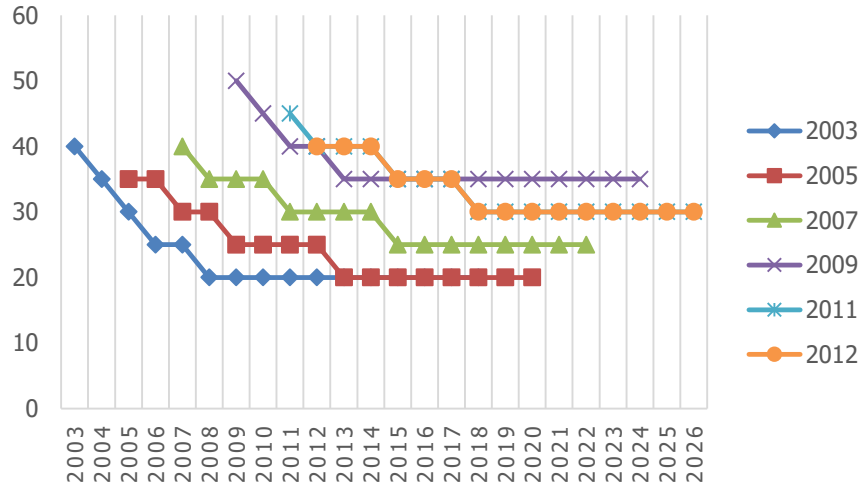


Need to combine speed and flexibility of packaging with pitch and performance of advanced heterogeneous device technology.

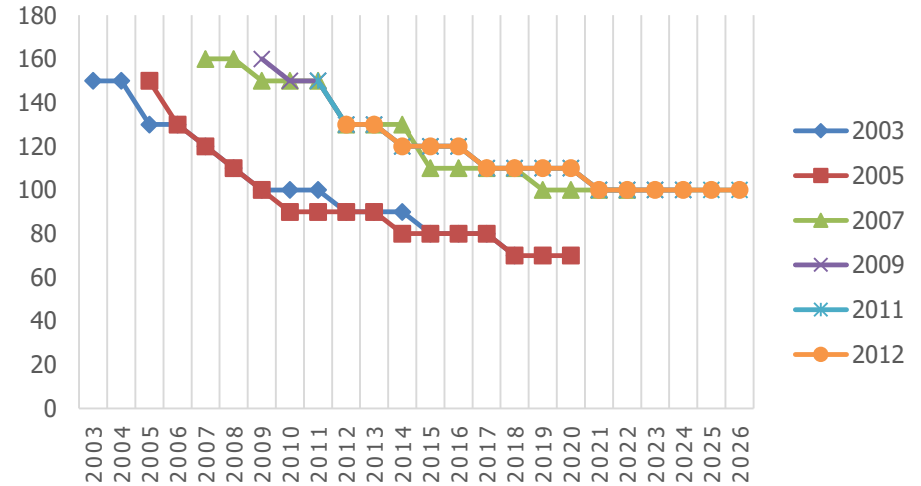


Interconnect Pitch Progress Has Lagged Projections

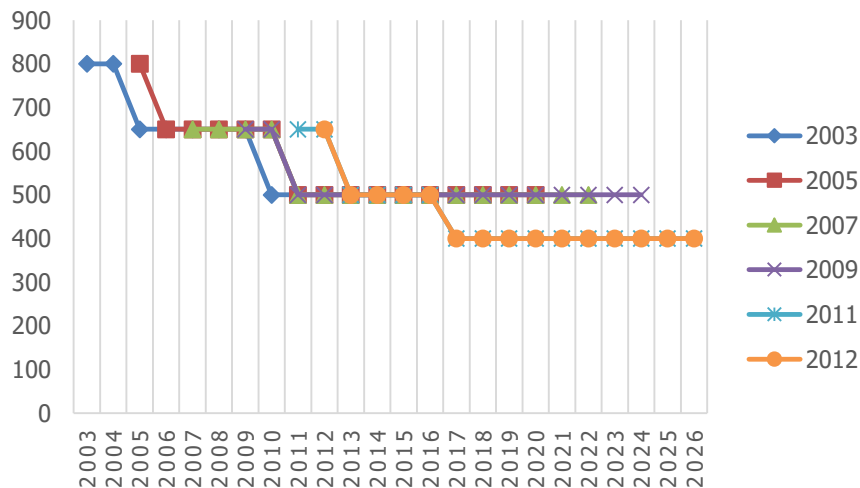
Wire Bond Pitch by ITRS Version



Flip Chip Area Array Pitch by ITRS Version



PCB Solder Ball Pitch by ITRS Version



Notes:

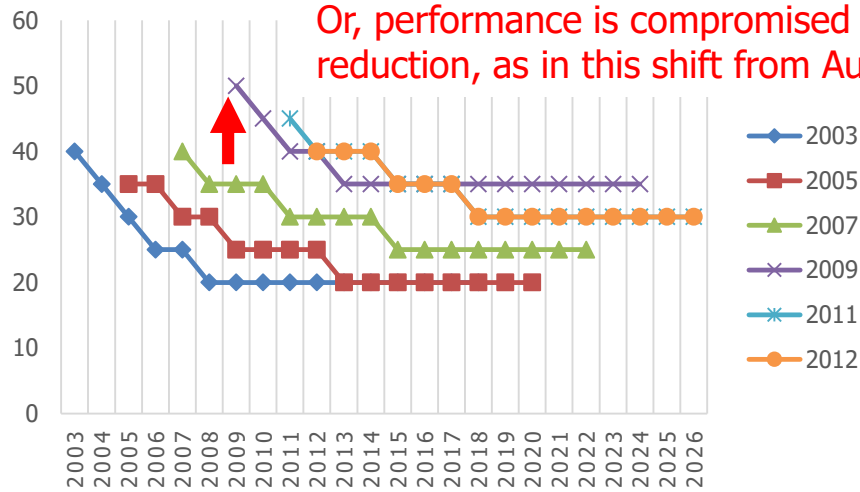
- Dimensions in microns.
- Wire bonding:
 - Discontinuity in 2009 due to shift to Cu as mainstream wire material.
 - Data is for "single in-line." Multi-tier first appeared in 2005 roadmap.
- Flip chip:
 - Discontinuities due to shifting ITRS product/application categories.
 - Data is for "GPU/CPU/Chipset" in 2007, "high-performance" in 2009, and "cost-performance" in 2011-12.
- PCB:
 - Data is for "cost-performance" category.
 - Data is for "conventional system board" application starting in 2007.

Can address the growing interconnect gap with standardized, fine pitch interconnects.

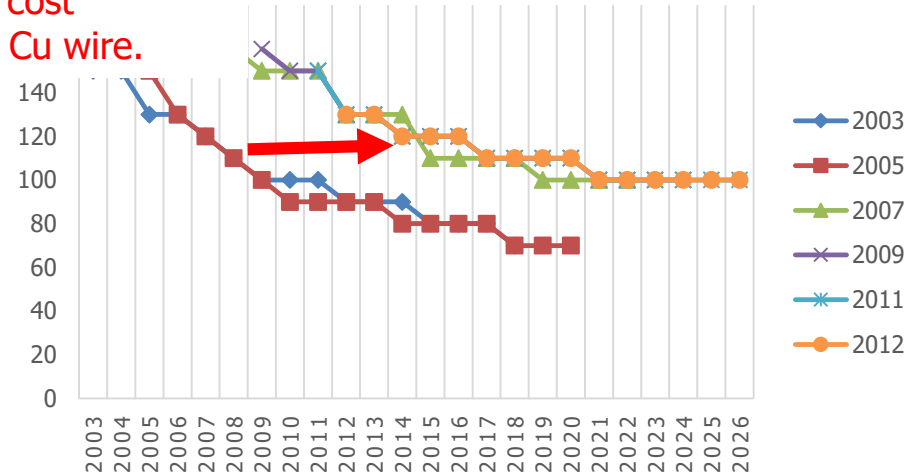


Interconnect Pitch Progress Has Lagged Projections

Wire Bond Pitch by ITRS Version



Flip Chip Area Array Pitch by ITRS Version



PCB Solder Ball Pitch by ITRS Version



Progress is typically pushed out in subsequent roadmap updates.

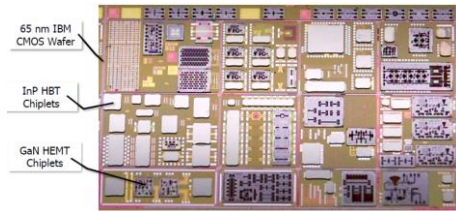
Notes:

- Dimensions in microns.
- Wire bonding:
 - Discontinuity in 2009 due to shift to Cu as mainstream wire material.
 - Data is for "single in-line." Multi-tier first appeared in 2005 roadmap.
- Flip chip:
 - Discontinuities due to shifting ITRS product/application categories.
 - Data is for "GPU/CPU/Chipset" in 2007, "high-performance" in 2009, and "cost-performance" in 2011-12.
- PCB:
 - Data is for "cost-performance" category.
 - Data is for "conventional system board" application starting in 2007.

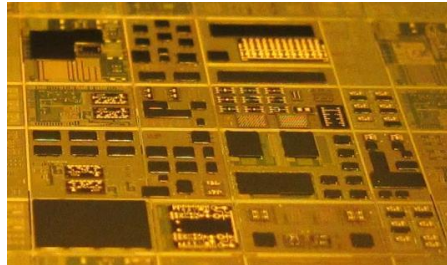
Can address the growing interconnect gap with standardized, fine pitch interconnects.



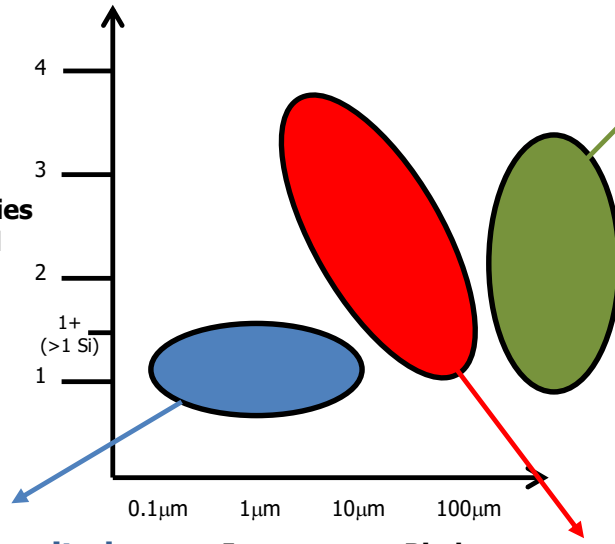
Heterogeneous Integration: Bridging the Gap



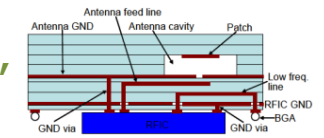
DAHI MPW0



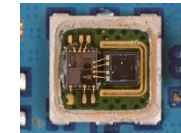
DAHI MPW1



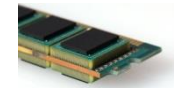
Package-based:
Mature and flexible,
but not scalable



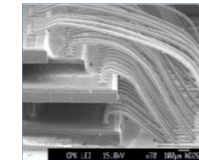
Advanced PCB



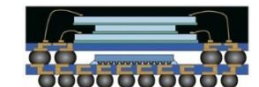
MEMS + ASIC



PoP memory

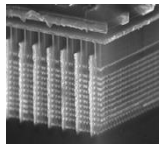


Stacked die (WB)

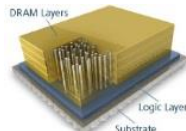


Processor + memory PoP

Technologies Integrated

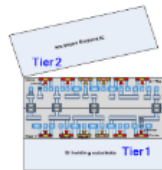


Monolithic 3D NAND

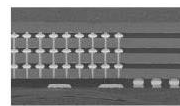


Processor + memory TSV

TSV / Wafer-scale:
Immature or not well-suited
for Heterogeneous Integration



F2F wafer-bond

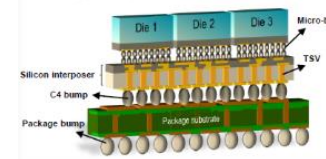


NAND/DRAM TSV



Image sensor TSV

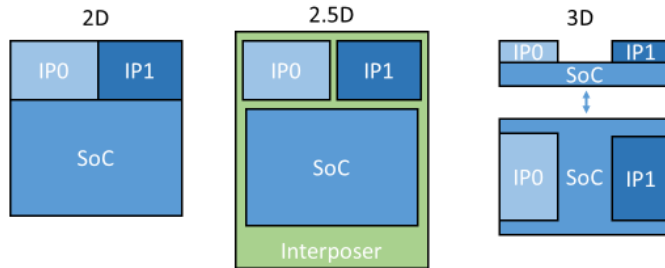
Interposer-based:
Scalable and flexible



2.5D Si interposer

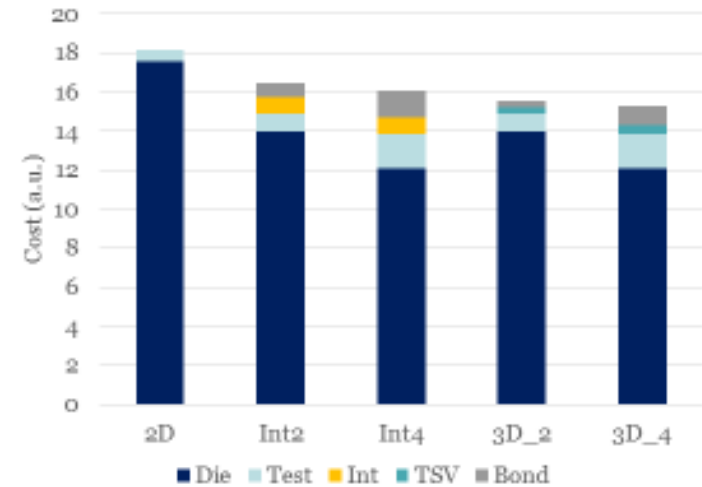
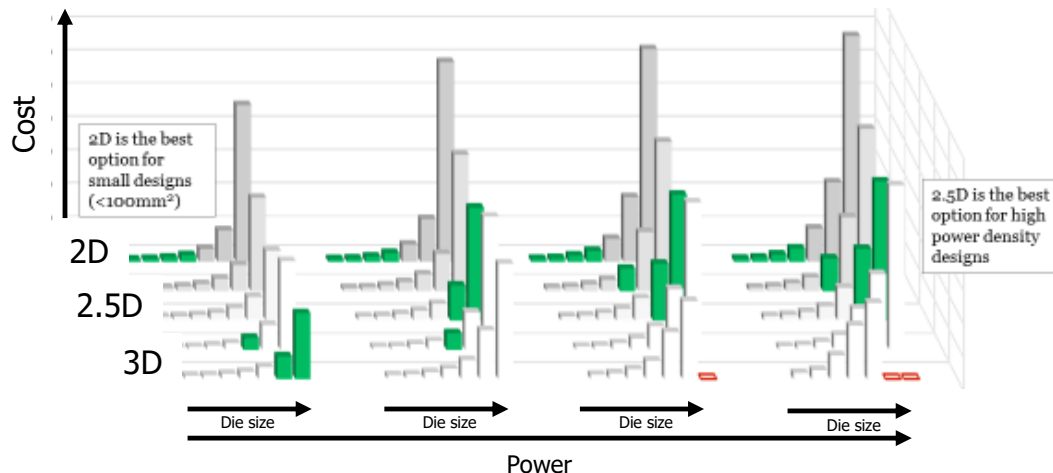
DAHI creates integration capabilities beyond current advanced interconnect technologies.

Case Study Scenario



Many factors affect optimal integration approach:

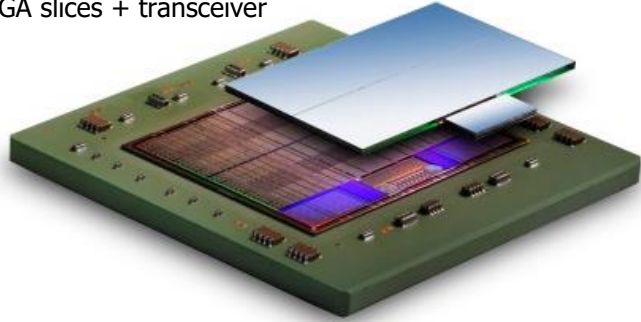
- size of IP blocks
- % IP reuse
- licensing cost
- die size
- process yield / maturity
- relative cost of nodes
- power / cooling options
- gate count



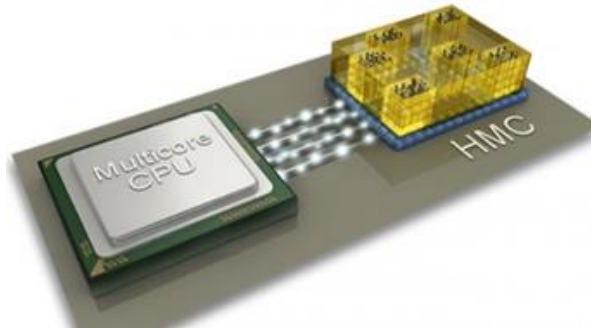
The die cost dominates, independent of integration approach, so chip cost reduction via IP reuse is beneficial in all scenarios.

2.5D is typically the best option for high power, high complexity designs.

Xilinx Virtex-7 H580T
2 FPGA slices + transceiver



Increases Yield



Links High Bandwidth
Memory to Processor



Enables IP Reuse

But everything is a point solution!



What is CHIPS?

CHIPS will develop design tools, integration standards, and IP blocks required to demonstrate modular electronic systems that can leverage the best of DoD and commercial designs and technology.

Today – Monolithic

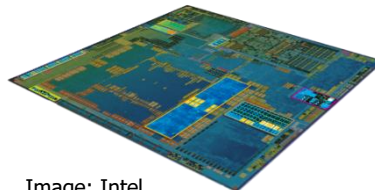
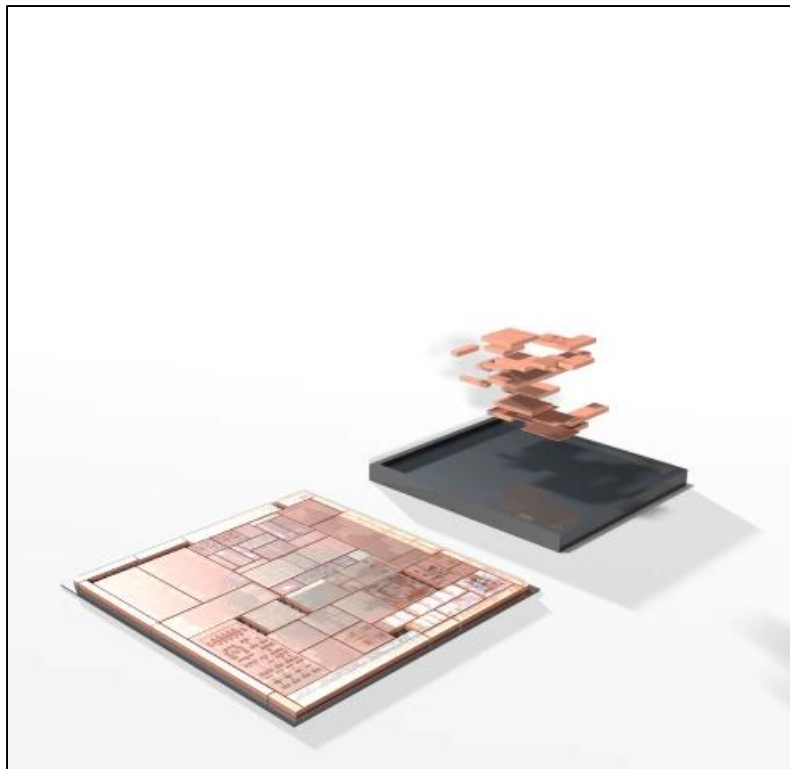
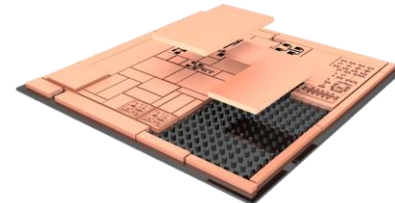


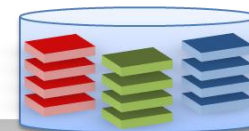
Image: Intel

Tomorrow – Modular

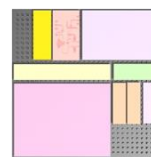
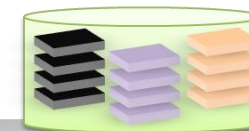


CHIPS enables rapid integration of functional blocks at the chiplet level

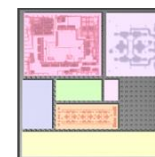
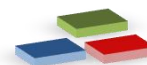
Custom chiplets



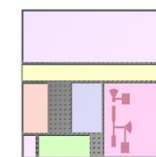
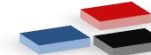
Commercial chiplets



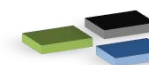
COMM



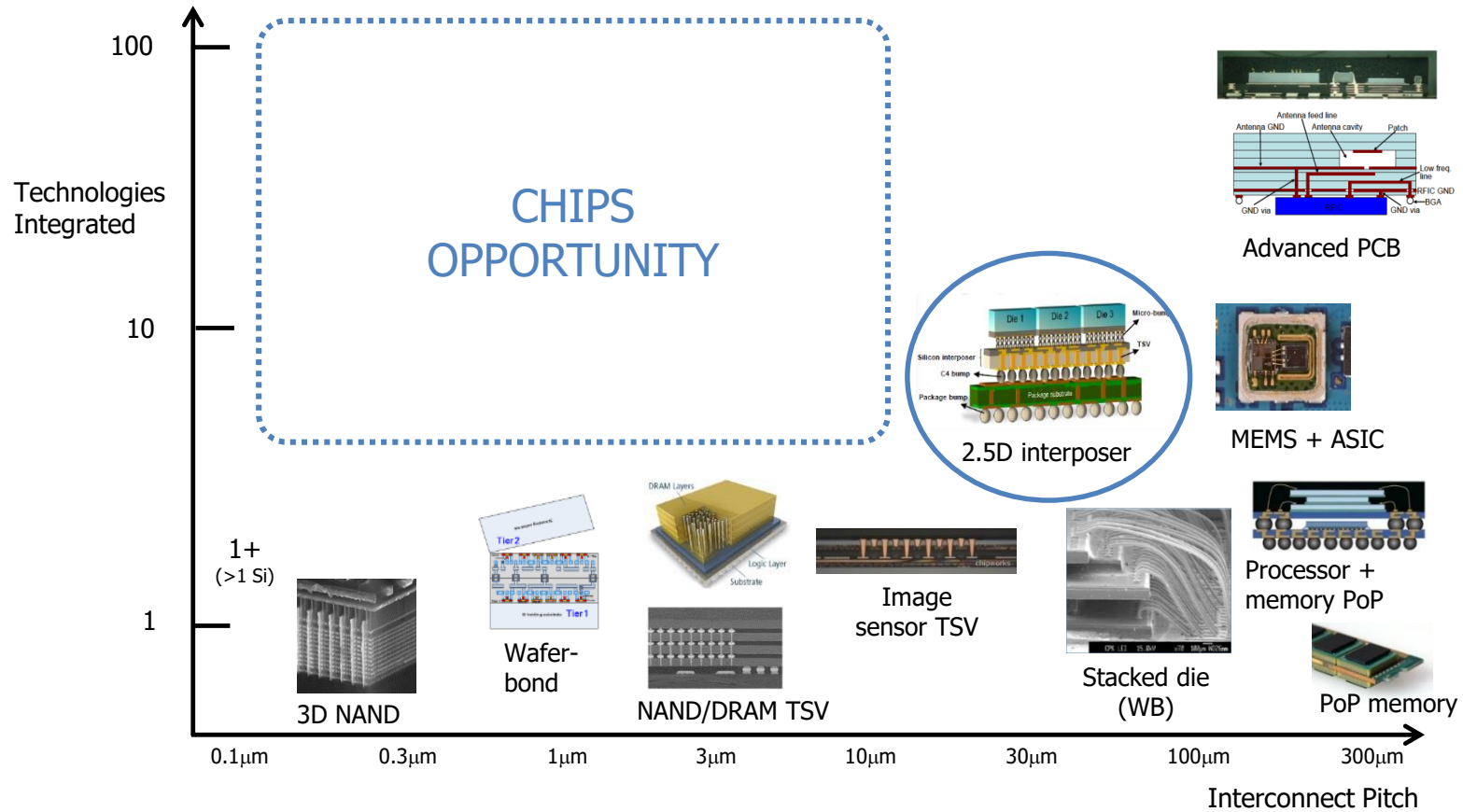
RADAR EW



SIGINT

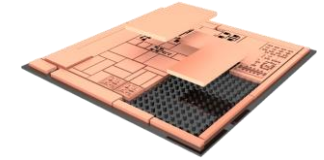


Adaptive filter	SerDes	SerDes
Beam forming	Beam forming	Adaptive filter
QR Decomp.	QR Decomp.	QR Decomp.

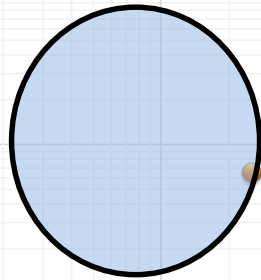
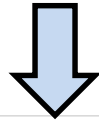




CHIPS developing interface standard

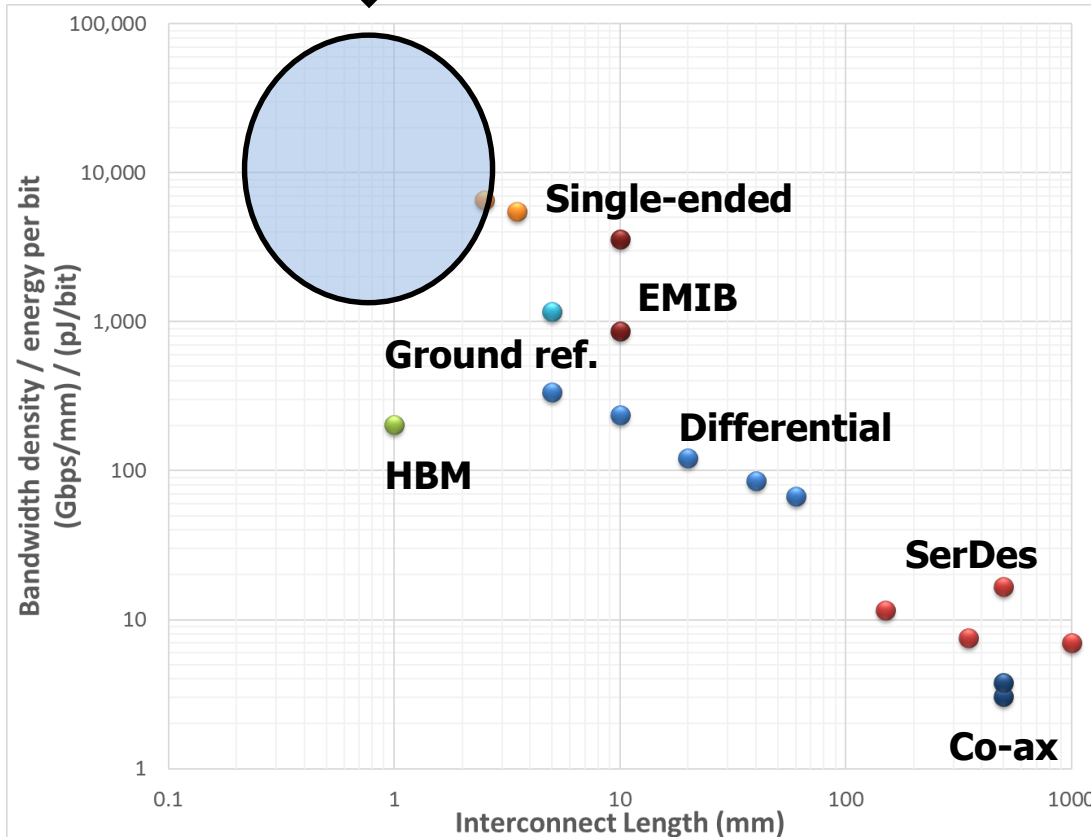


CHIPS Target



CHIPS Program Interface Standard Metrics

Data rate	10 Gbps
Energy efficiency	< 1 pJ/bit
Latency	< 5 ns
Bandwidth density	> 1000 Gbps/mm




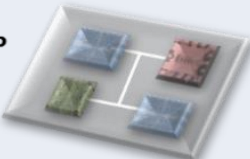
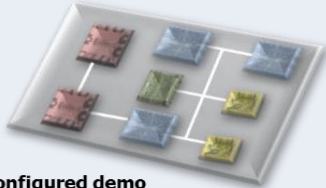
- 28nm SOI, Single-ended, Al on Si
- 28nm, ground-ref., single-ended, organic PCB
- 45nm SOI, differential, Cu on Si
- 32nm, differential, 32AWG cable
- EMIB
- 14nm SERDES, PCB
- 14nm HBM

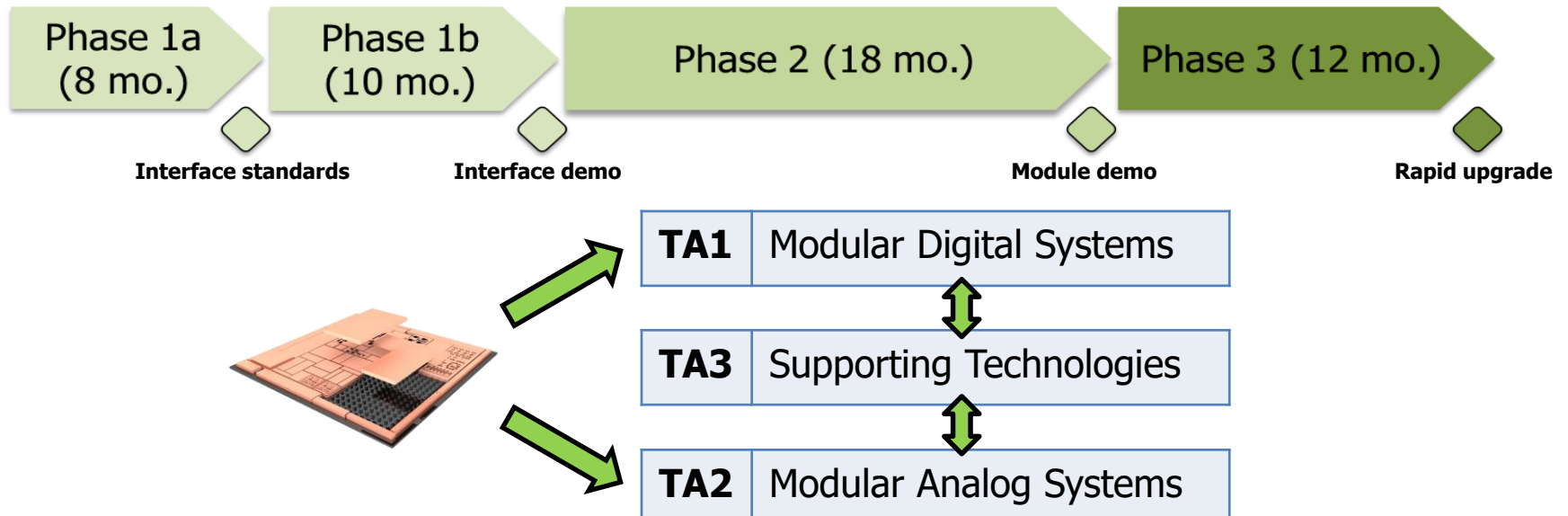
Sources:
 1. 2016 *JSSC*, Dehlaghi
 2. 2013 *JSSC*, Poulton
 3. 2012 *JSSC*, Dickson
 4. 2013 *JSSC*, Mansuri
 5. 2016 *ECTC*, Mahajan

CHIPS interface is one of many possible routes for efficient interdie communications

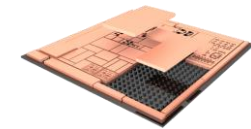


CHIPS program: structure and timing

PHASE 1	PHASE 2	PHASE 3
Interface and IP Block Demo	Module Demo with IP Blocks	Rapid Module Upgrade
 Integration platform Interface demo	Full system IP reuse demo 	 Reconfigured demo



Seeking CHIPS collaboration to help drive a common interface



CHIPS Team

Designs

- Boeing
- Intel
- Lockheed Martin
- Northrop Grumman
- Univ. of Michigan

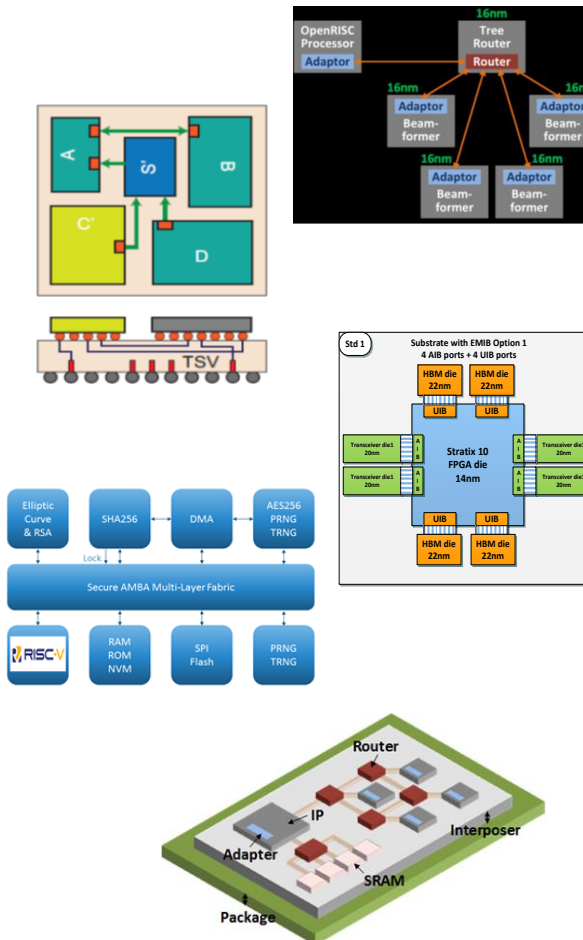
Chiplets

- Intrinsix
- Jariet
- Micron
- North Carolina State
- Synopsys

Tools

- Cadence
- Georgia Tech

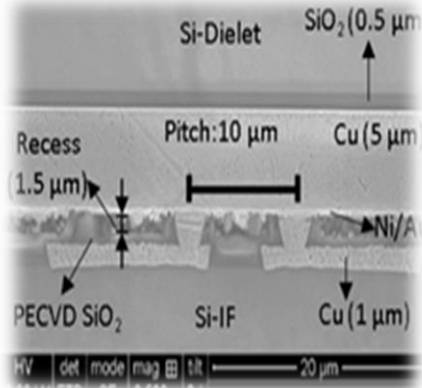
CHIPS Approach Modularity Standards



CHIPS Results Fast Cost-Effective Best-in-Class

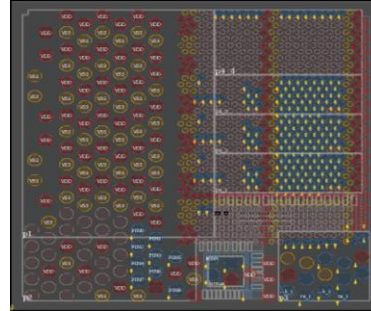


Manufacturing



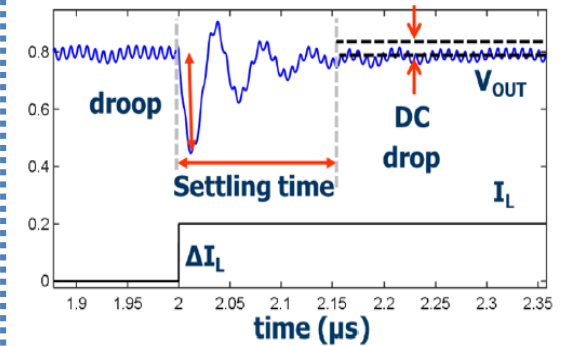
Intel
Northrop Grumman
Micross
UCLA

Chiplets



Jarriet
Synopsys
Micron
Intrinsix
Lockheed Martin
Michigan
NCSU
Ferric

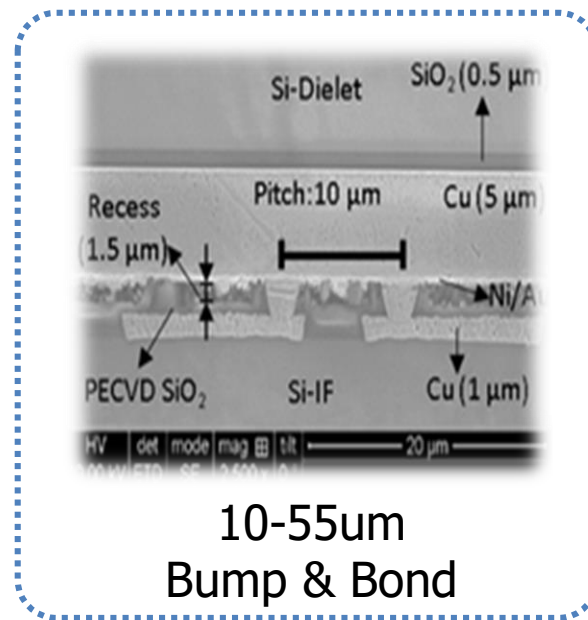
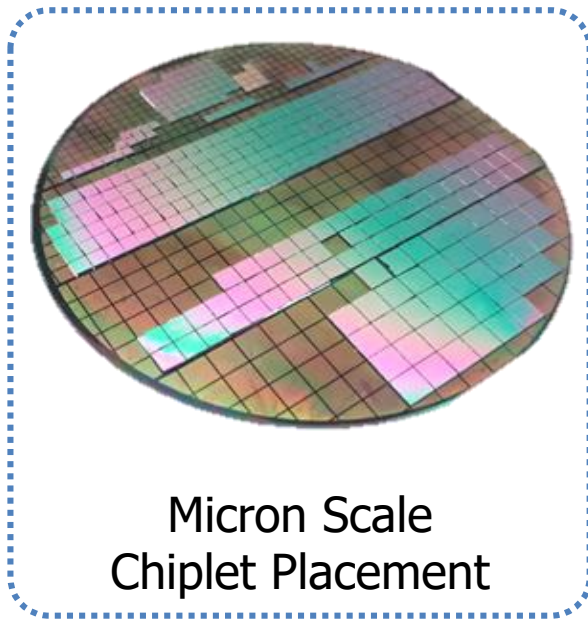
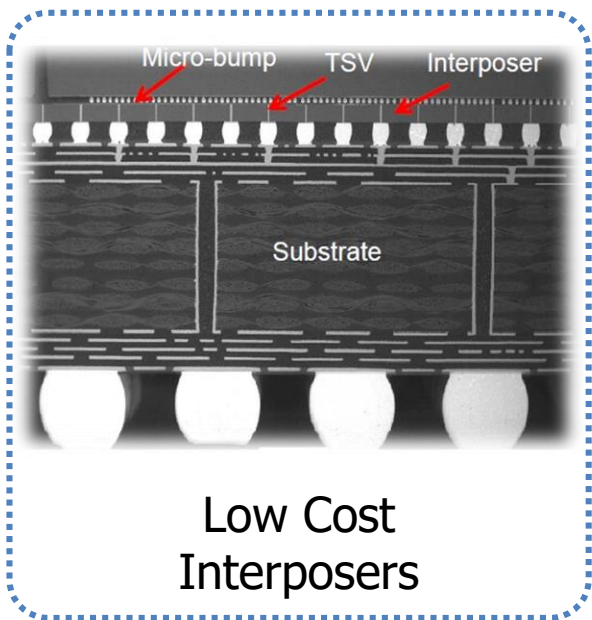
Tools



Cadence
Georgia Tech



Current Focus of CHIPS: Interface Standard and Manufacturing

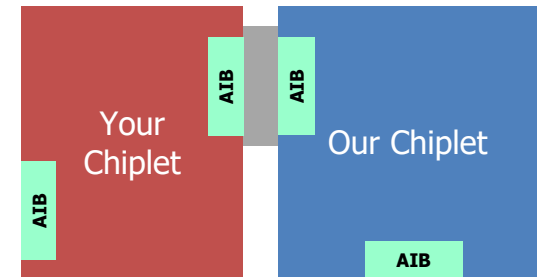


CHIPS is targeting solutions suitable for low volume (<100K units) trusted manufacturing needed for national security requirements.



CHIPS Interface Standard Based on Intel's AIB

- **AIB (Advanced Interface Bus)** is a PHY-level interface standard for **high bandwidth, low power** die-to-die communication
 - AIB is a clock-forwarded parallel data transfer like DDR DRAM
 - High density with 2.5D interposer (e.g., CoWoS, EMIB) for multi-chip packaging
 - AIB is PHY level (OSI Layer 1)
 - Can build protocols like AXI-4 or PCI Express on top of AIB
- **AIB Promoters** agreed to promote AIB as a die-to-die interface standard
- Public information available from Intel at:
<https://intel.ly/2LISZcr>



ADC/DAC
Machine Learning
Memory
Processors
Adjacent IP
Etc. ...

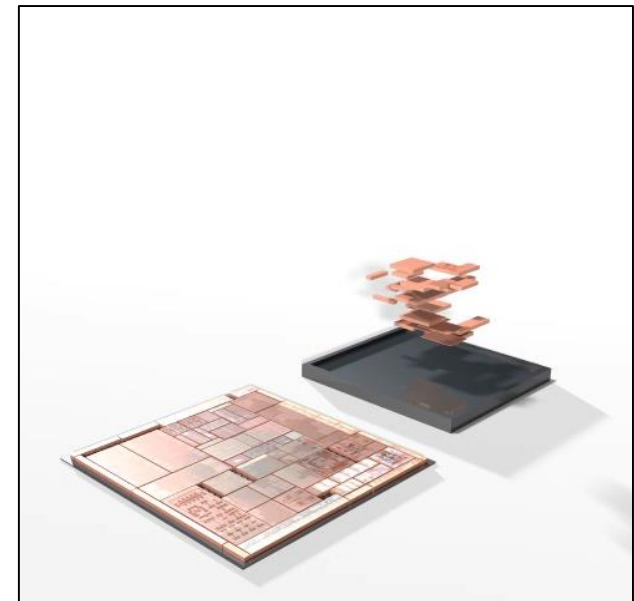
AIB Promoters:

-Boeing
-Intrinsix
-Synopsys
-Intel
-Lockheed Martin
-Sandia
-Jariet
-NCSU
-U. of Michigan



The CHIPS Vision: Ethernet for Chips

- **Modularity:** A ubiquitous chiplet interface standard “Ethernet for chiplets”
- **Speed:** Board manufacturing time scales (days) possible with a library of hundreds of COTS chiplets
- **Performance:** 1pJ/bit and 1Tbit/mm WILL disrupt the computing landscape
- **Security:** CHIPS disaggregation offers a pathway to high assurance electronics





DARPA MTO Electronics Resurgence Initiative

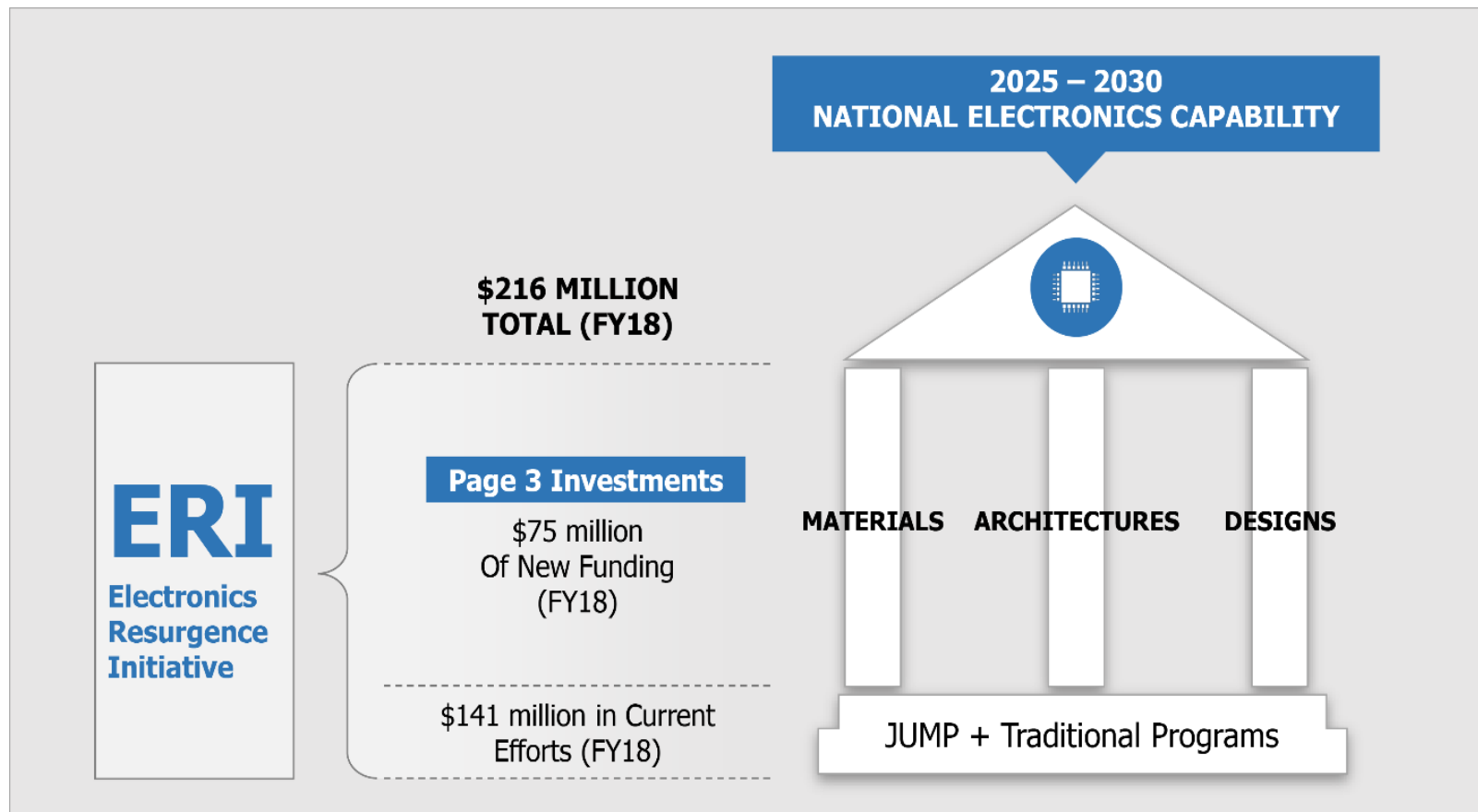
Most presentations from the July 2018 and July 2019 ERI Summits are available as links from the agenda pages:

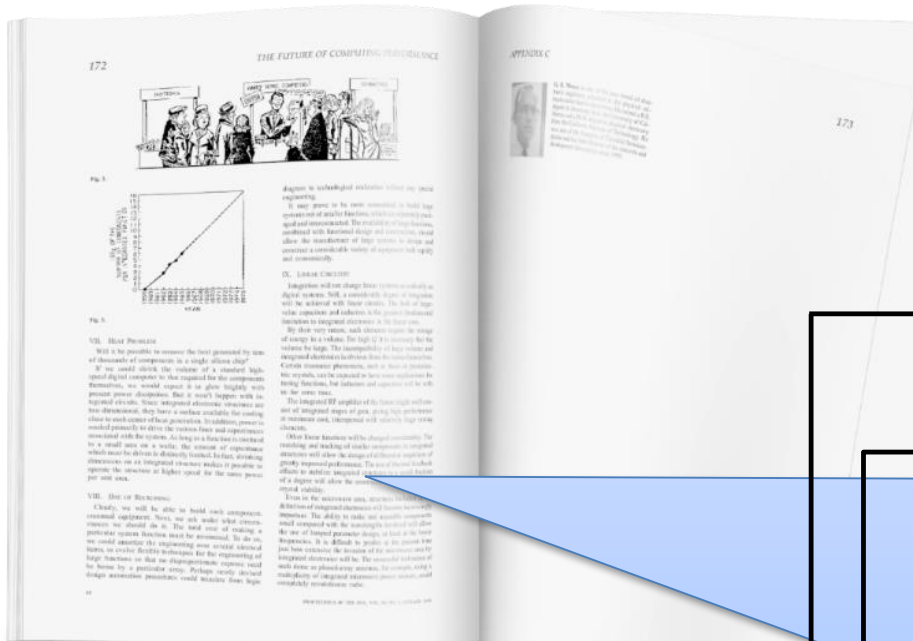
<http://www.eri-summit.com>



Electronics Resurgence Initiative

- ERI—creating an electronics capability that will provide a foundational contribution to national security
- Three thrust areas: Materials and Integration, Architectures, Designs





Electronics, April 19, 1965: Cramming More Components into Integrated Circuits; Gordon Moore

P.3

Architecture
Maximizing specialized functions

Design
Quickly enabling specialization


VIII. DAY OF RECKONING

Clearly, we will be able to build such component-crammed equipment. Next, we ask under what circumstances we should do it. **The total cost of making a particular system function must be minimized.** To do so, we could amortize the engineering over several identical items, or **evolve flexible techniques for the engineering of large functions** so that no disproportionate expense need be borne by a particular array. Perhaps **newly devised design automation procedures could translate from logic diagram to technological realization** by special engineering.

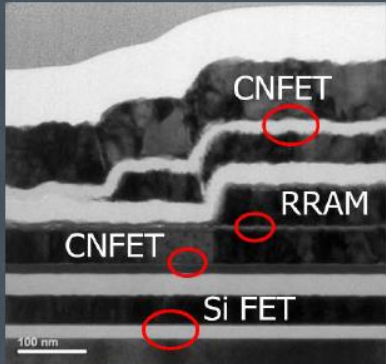
It may prove to be **more economical to build large systems out of smaller functions, which are separately packaged** and interconnected. The availability of large functions, combined with functional design and construction, should allow the manufacturer of large systems to design and construct a considerable variety of equipment both rapidly and economically.

Materials & Integration

Adding separately packaged novel materials and using integration to provide specialized computing

 **Materials & Integration Thrust**

3DSOC

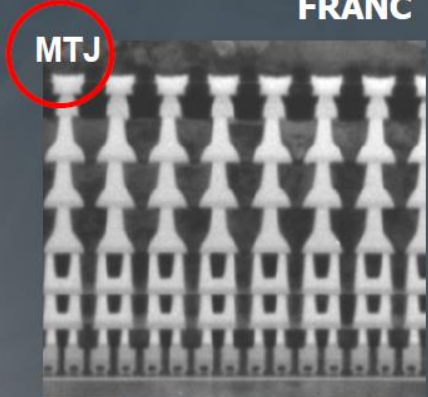


CNFET
RRAM
CNFET
Si FET

100 nm

Images: Stanford, MIT

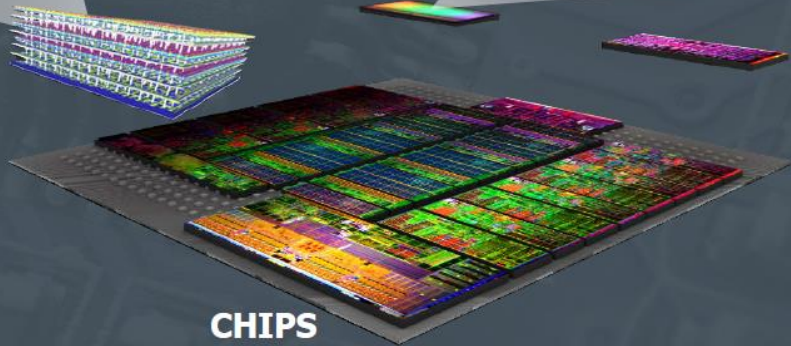
FRANC



MTJ

Image: GLOBALFOUNDRIES

CHIPS



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Designs Thrust

```

52 // calculate products as in * tap
53 val products = DspContext.withTrimType(dsptools.NoTrim) {
54   io.taps.reverse.map { tap => in.map { i =>
55     ShiftRegister(i * tap, config.multiplyPipelineDepth)
56   }}}

```

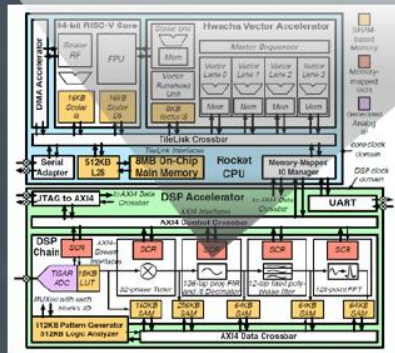
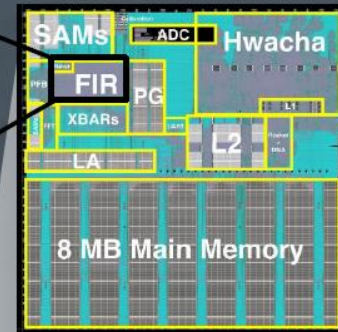
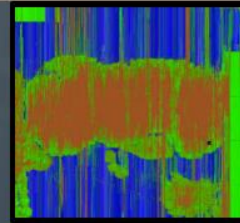
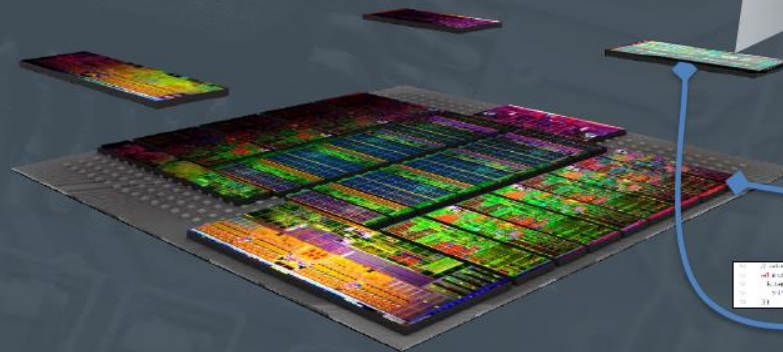


Image: UC Berkeley **CRAFT**

CRAFT

"Perhaps newly devised design automation procedures could translate from logic diagram to technological realization without any special engineering"



GitHub



POSH

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Architecture Thrust

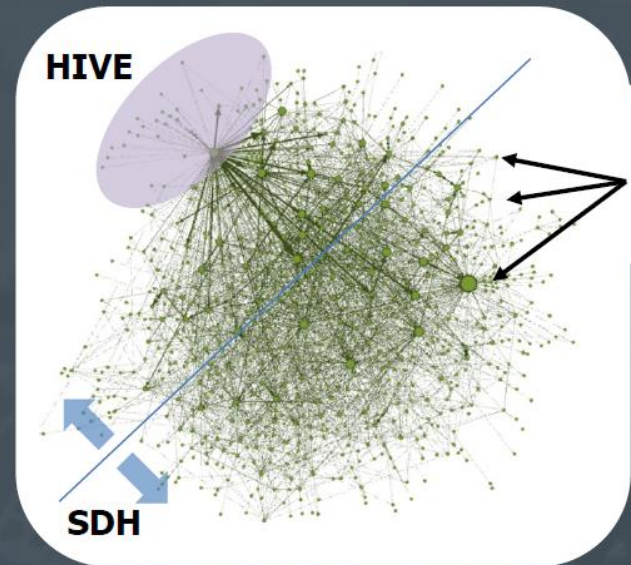


Image: Drexel Univ.

Array of sensors

DSSoc

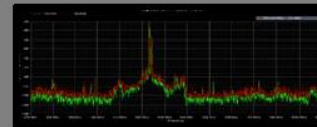
HIVE

"...amortize the engineering over several identical items, or evolve flexible techniques for the engineering of large functions..."

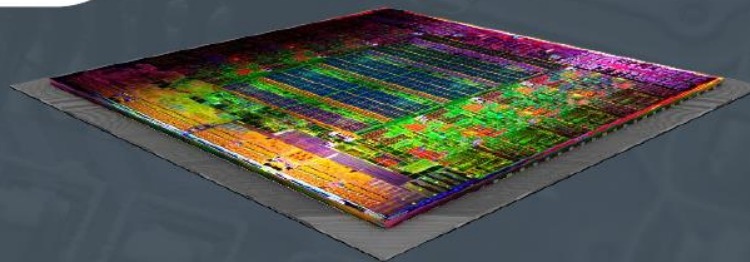
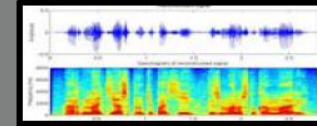
LiDAR



RF



Audio



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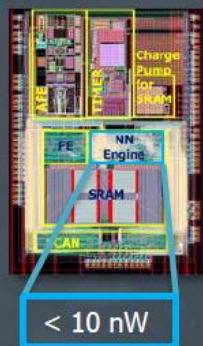


ERI Applications



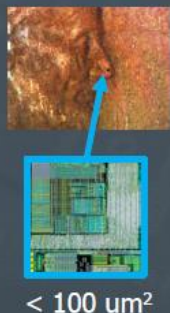
Driving Applications

N-ZERO



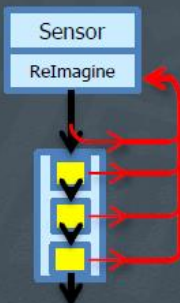
No Power Operation

SHIELD



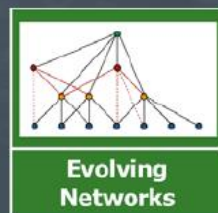
Art of the Small

ReImagine



Saliency

L2M



In Field Learning

SC2



Learning Cooperation through Edge Intelligence

SSITH



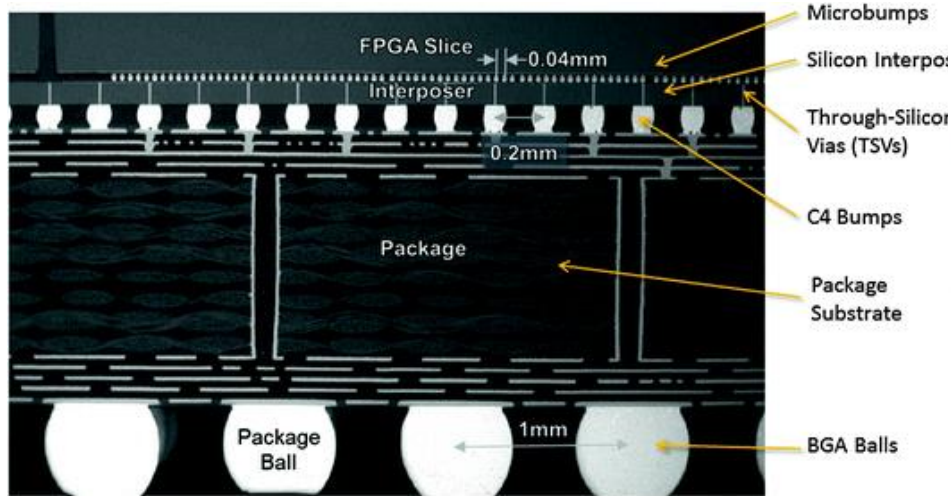
Hardware as the Foundation of Security

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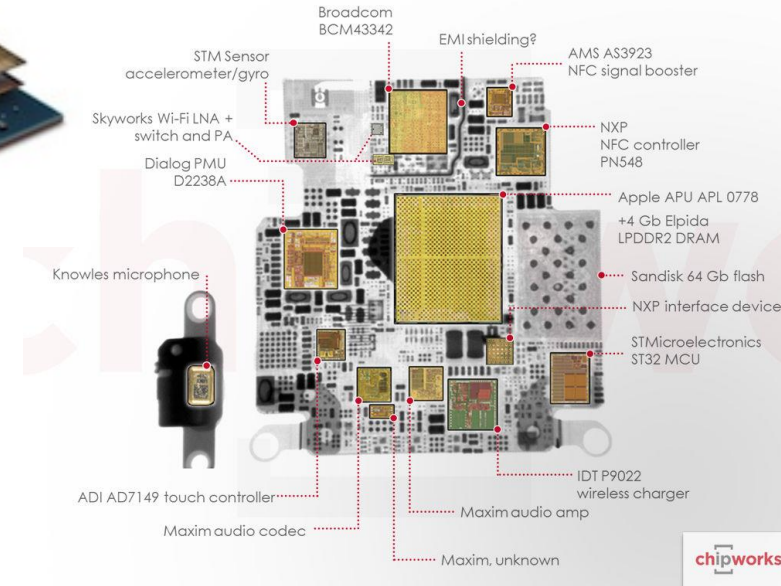


Future

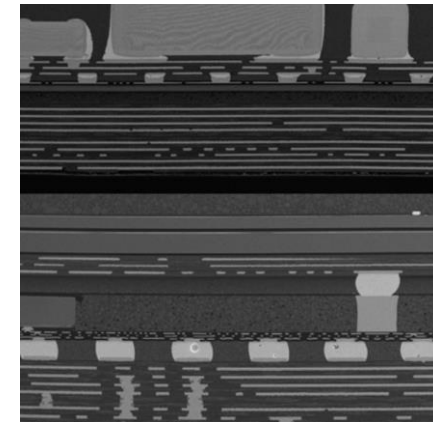
Semiconductor Packaging Landscape: Examples of leading edge capabilities available at commercial scales



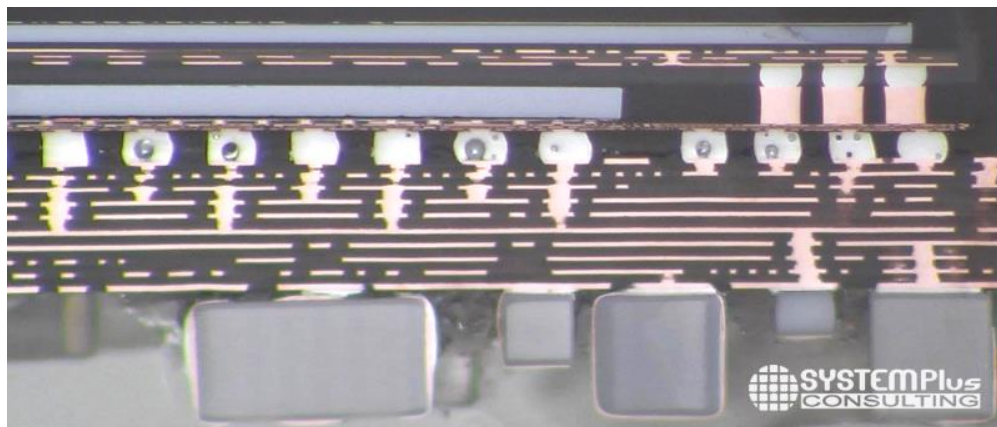
Amkor / Ibiden / TSMC Silicon interposers and through silicon vias (TSVs) for Xilinx FPGA



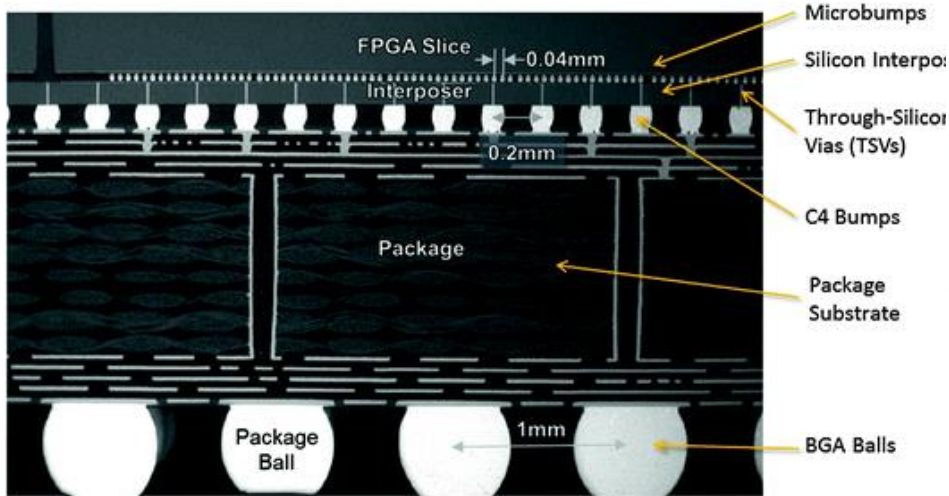
ASE System-in-Package in Apple Watch



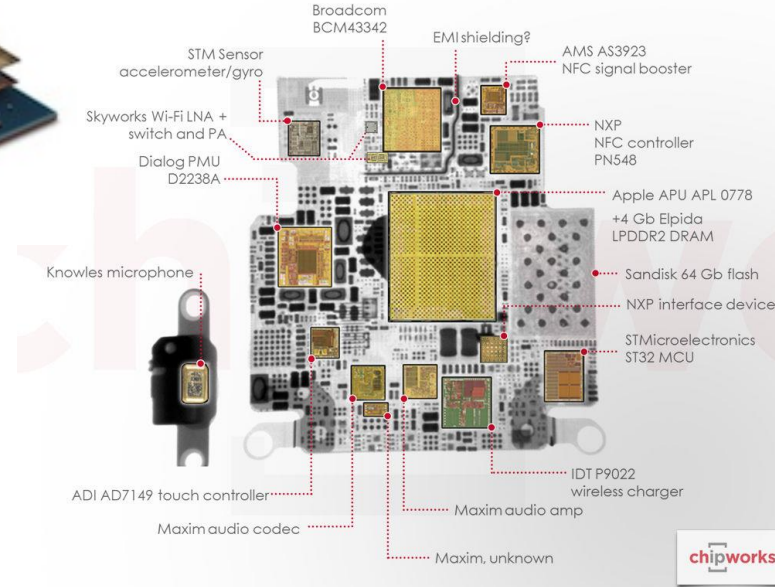
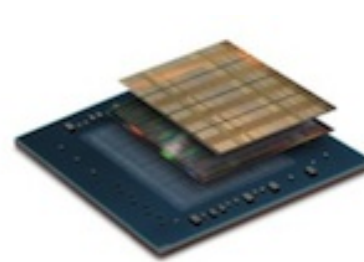
TSMC Integrated fan-out (InFO) packaging of A10 processor in iPhone7



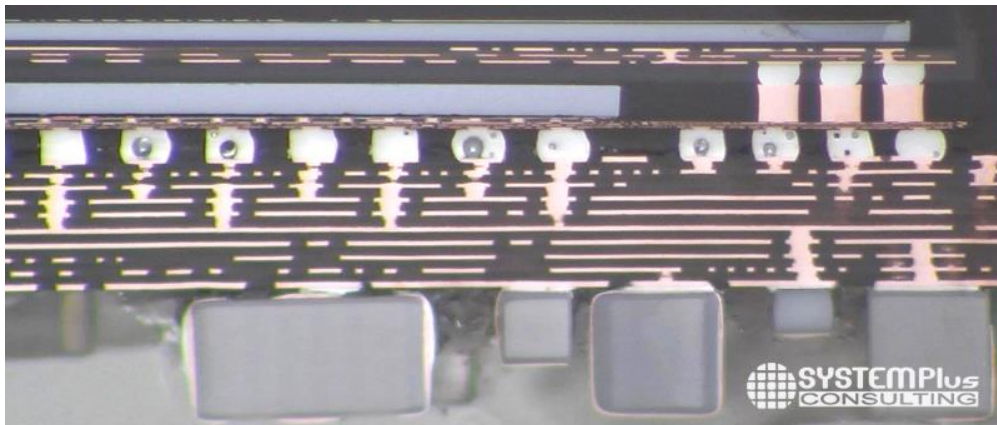
Semiconductor Packaging Landscape: Examples of leading edge capabilities **not** available to the DoD



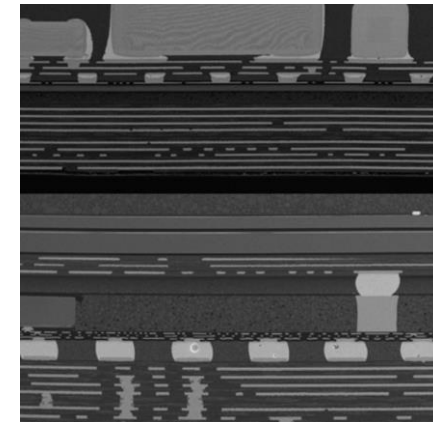
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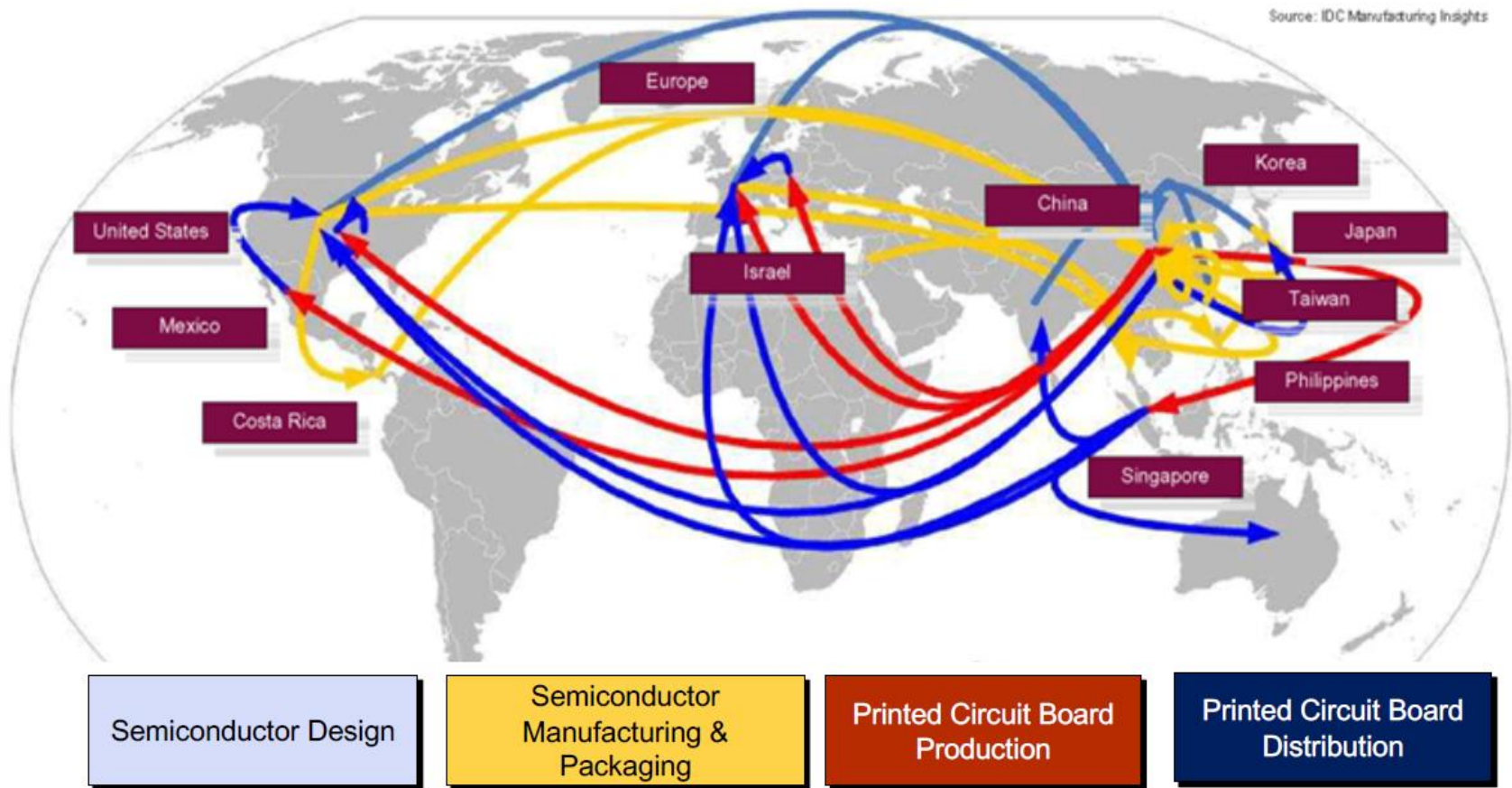
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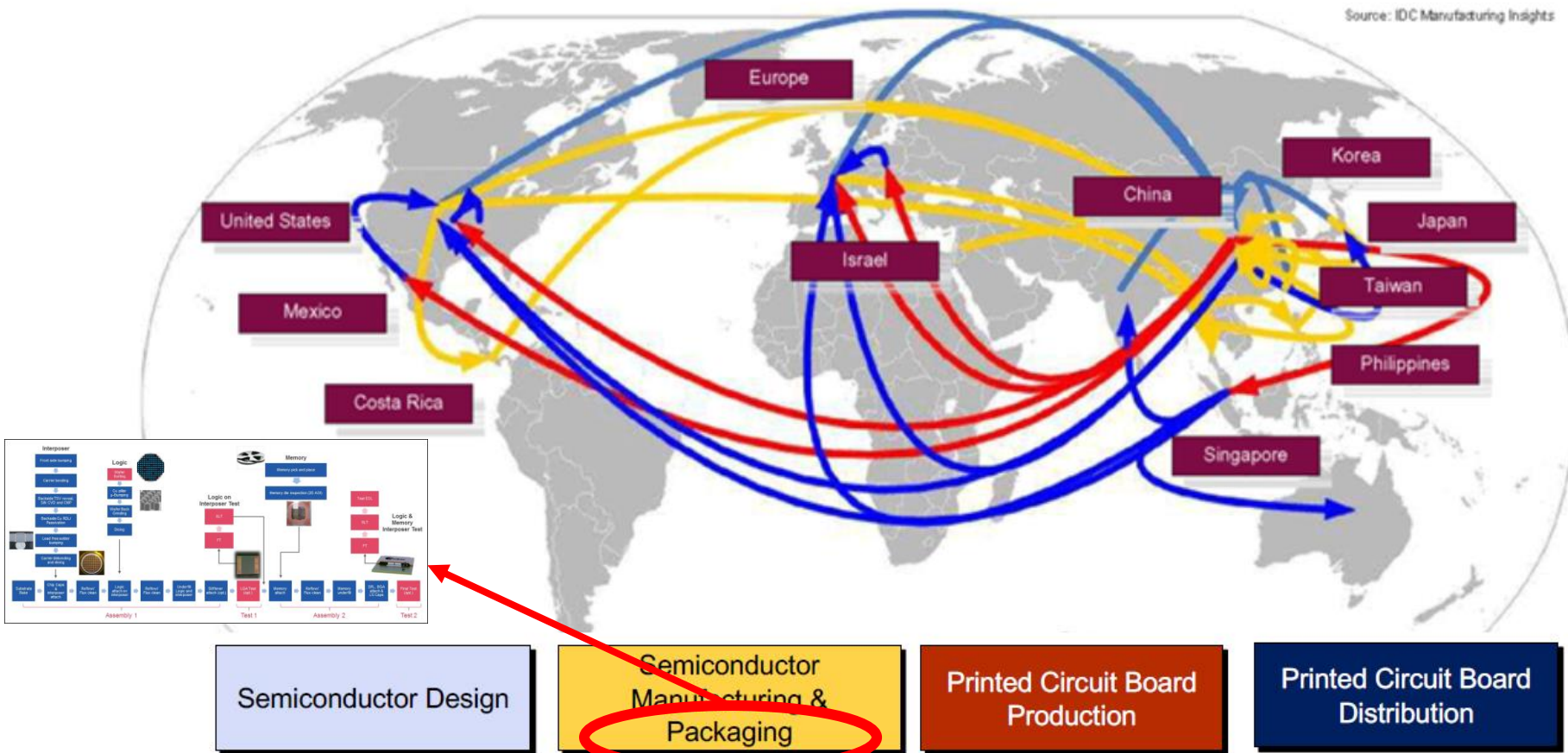
Electronic Manufacturing Supply Chain: Unavoidably international, even for DoD



Lifecycle for a single Joint Strike Fighter component,
which changes hands 15 times before final installation

Electronic Manufacturing Supply Chain: Unavoidably international, even for DoD

Source: IDC Manufacturing Insights



Semiconductor Design

Semiconductor Manufacturing & Packaging

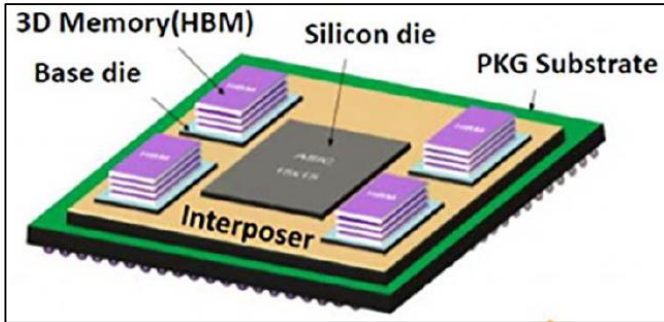
Printed Circuit Board Production

Printed Circuit Board Distribution

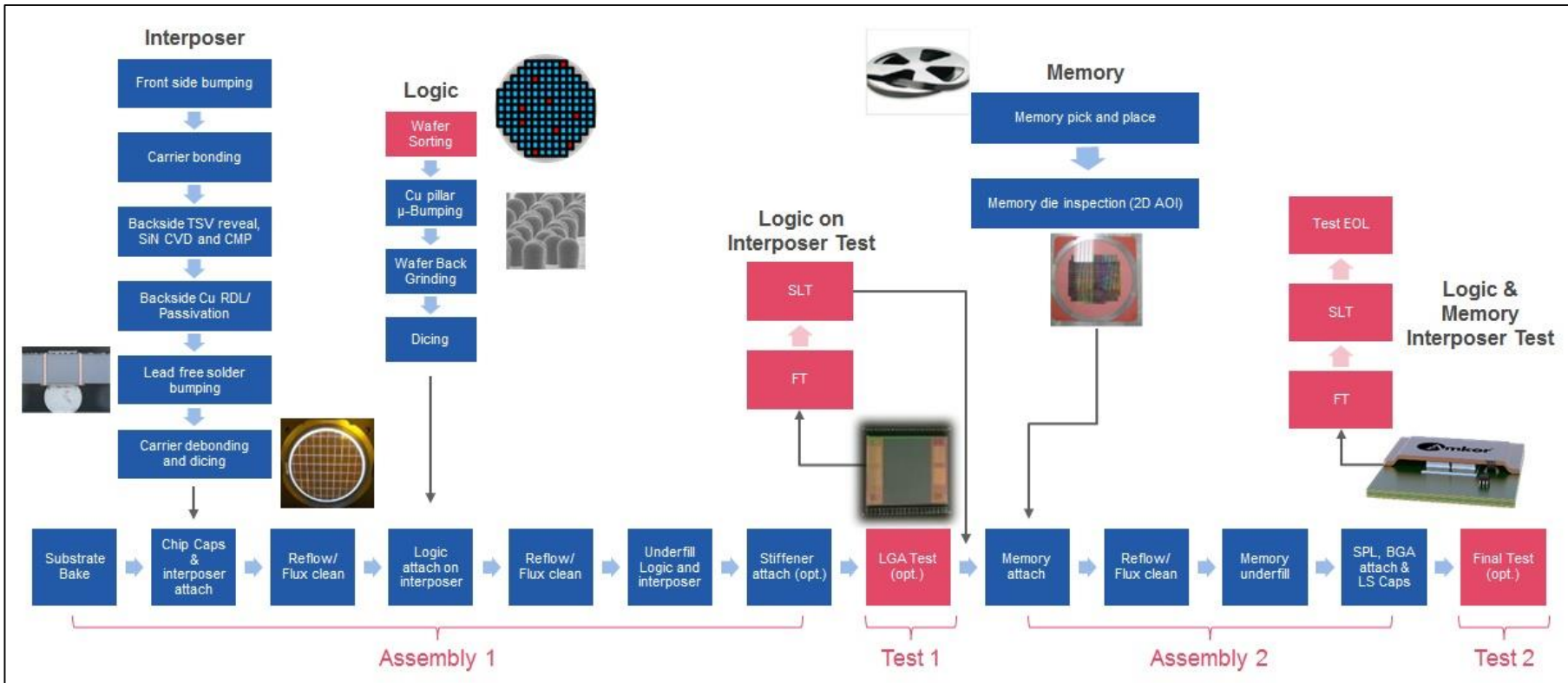
Source: IDC Manufacturing Insights & Booz Allen analysis

Lifecycle for a single Joint Strike Fighter component, which changes hands 15 times before final installation

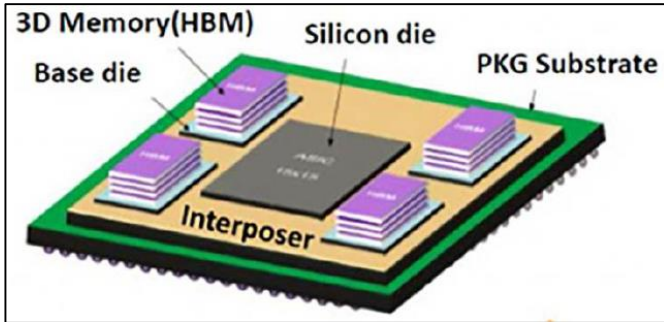
Semiconductor Assembly Example (2.5D HBM)



How many people have access throughout the supply chain?

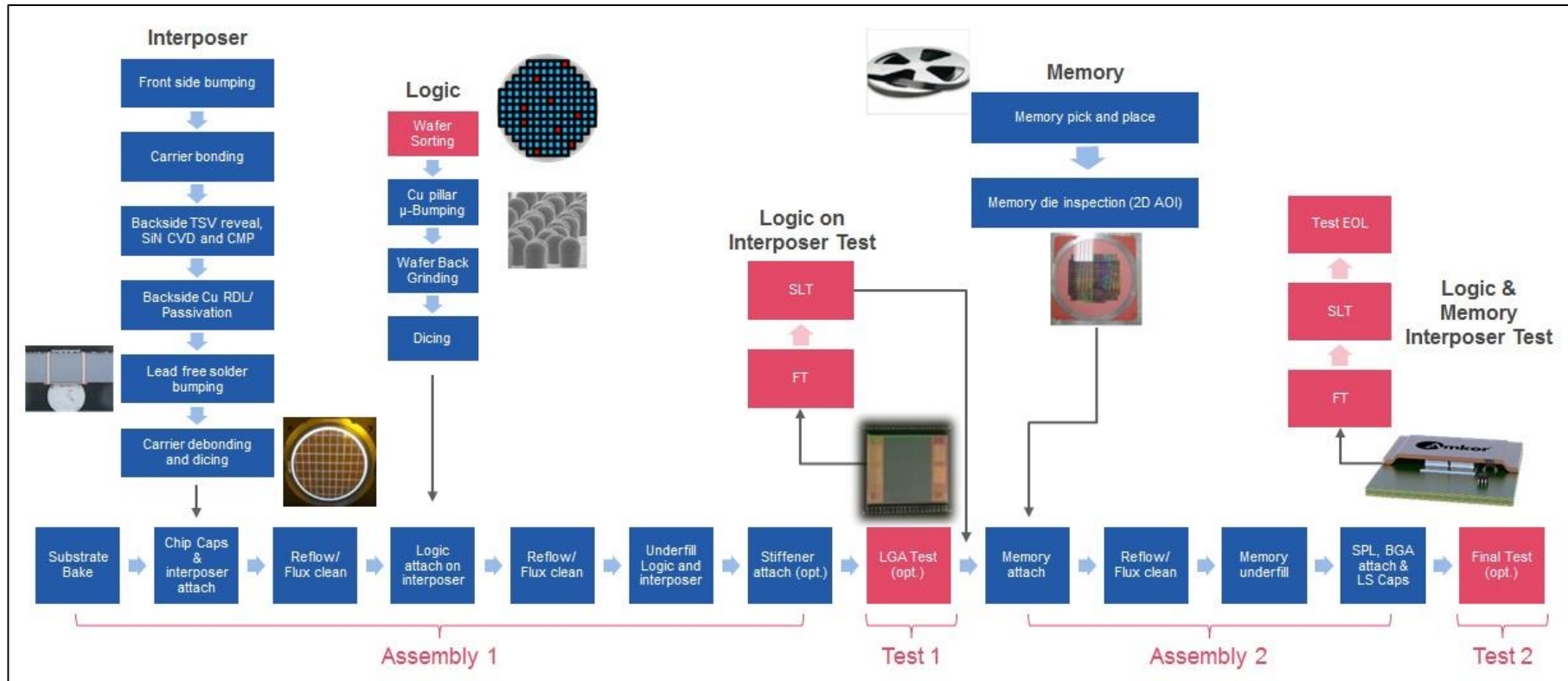


Semiconductor Assembly Example (2.5D HBM): How many people have access throughout the supply chain?



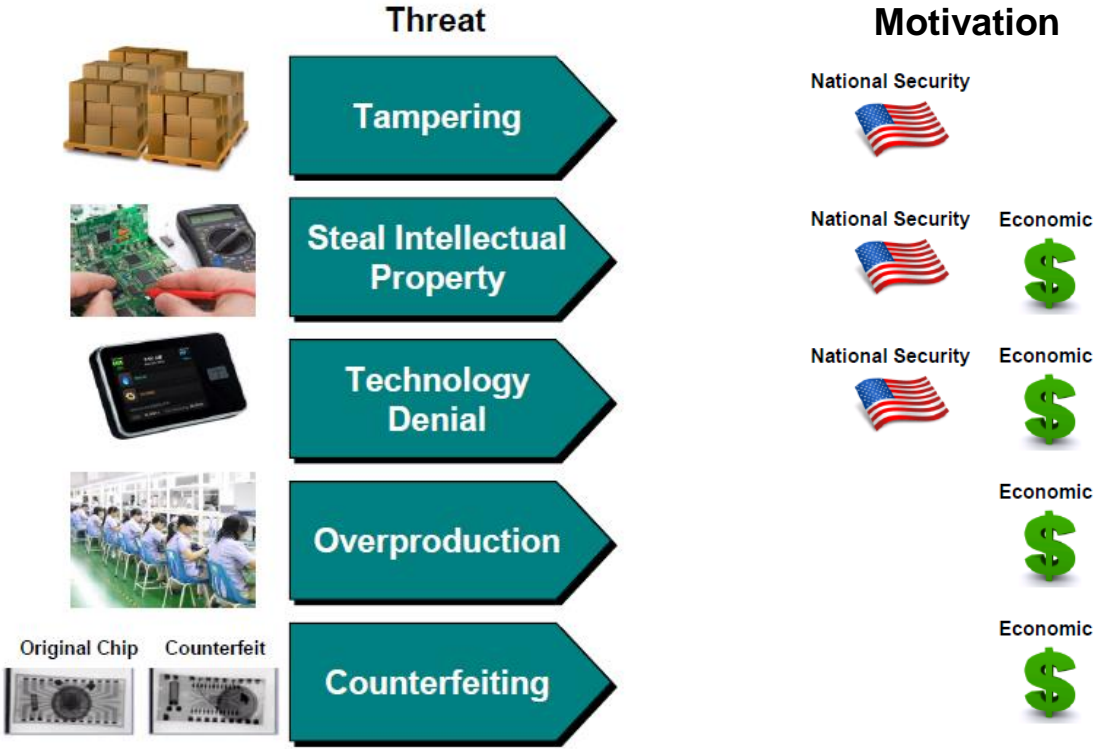
Can't control every step
=> Need combination of trusted resources and in-line checks

Optimal solution varies by assembly flow
=> Need semiconductor packaging process knowledge

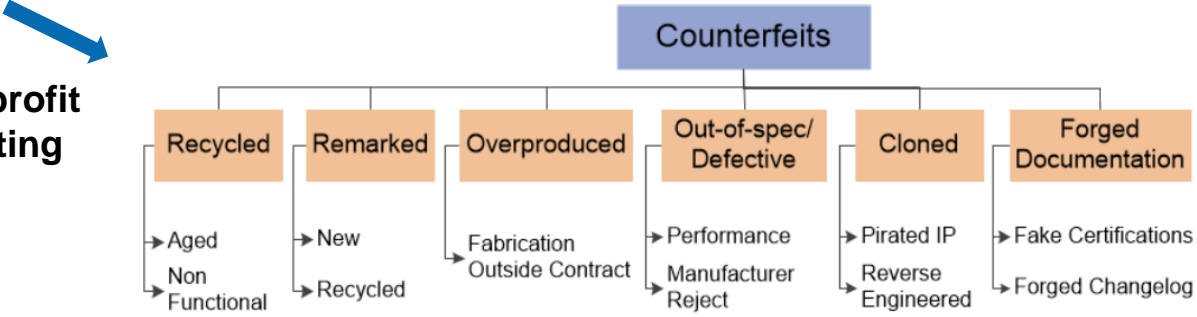


Semiconductor Security Vulnerabilities:

Many types of threats, motivated by financial and malicious interests



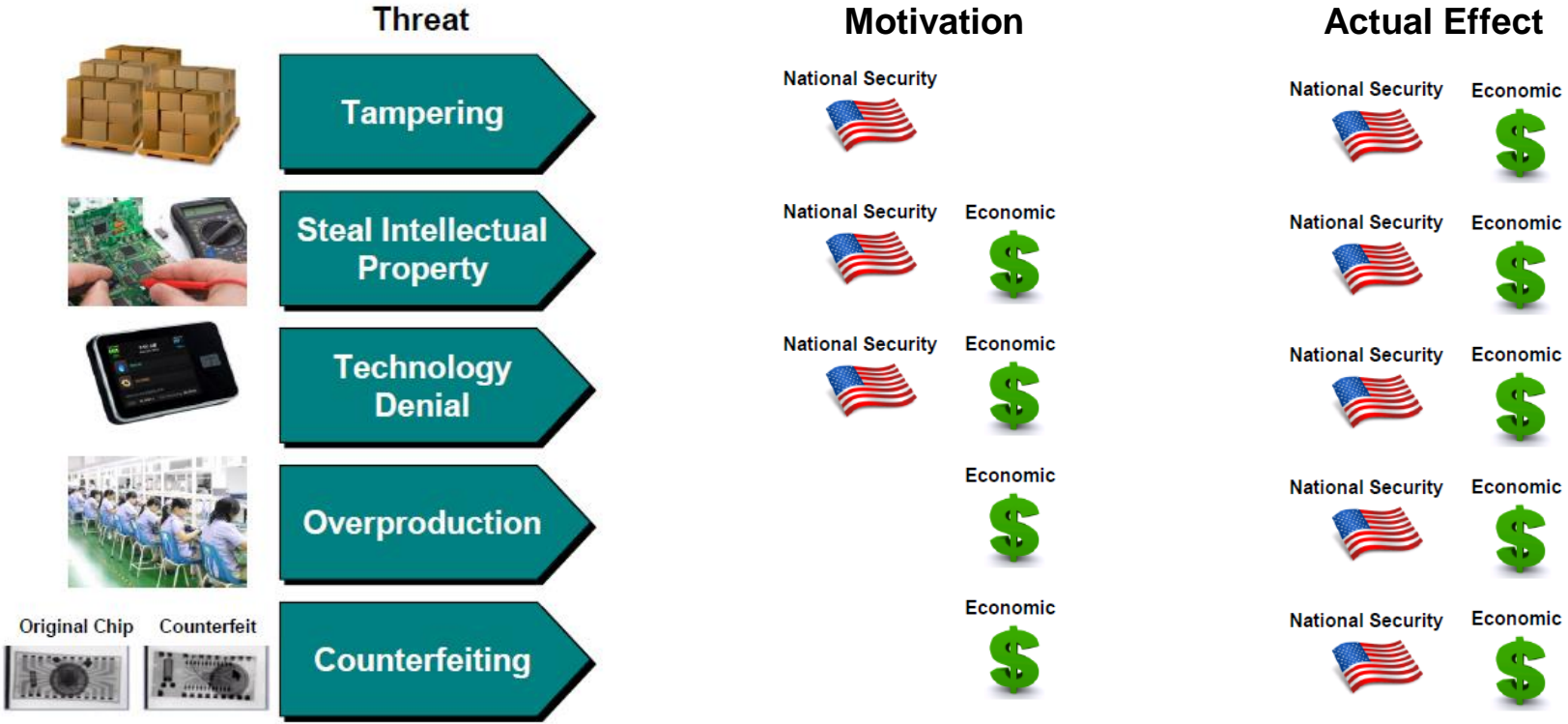
Many ways to profit via counterfeiting



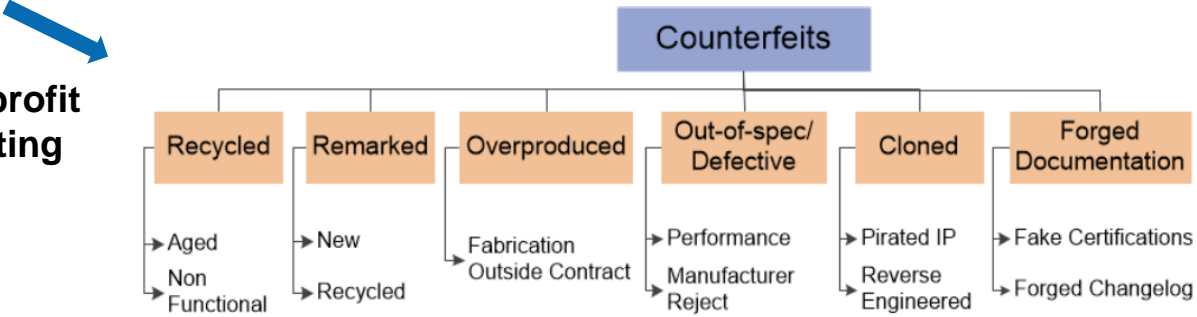
Source: Mark Tehranipour, "Counterfeit Detection and Avoidance," April 2018.
 Source: "Supply Chain Hardware Integrity for Electronics Defense (SHIELD)," Serge Leef, Software and Supply Chain Assurance Winter Forum, Dec. 2018

Semiconductor Security Vulnerabilities:

Many types of threats, motivated by financial and malicious interests



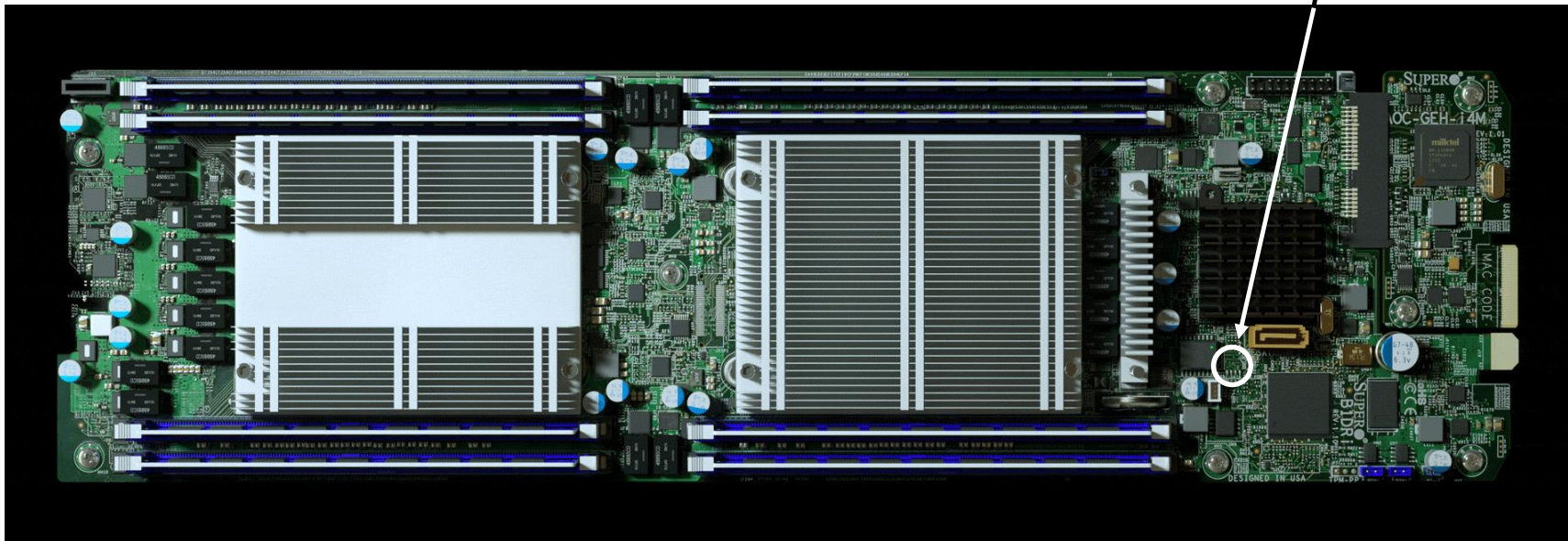
Many ways to profit via counterfeiting



Source: Mark Tehranipour, "Counterfeit Detection and Avoidance," April 2018.
 Source: "Supply Chain Hardware Integrity for Electronics Defense (SHIELD)," Serge Leef, Software and Supply Chain Assurance Winter Forum, Dec. 2018

Supply Chain Vulnerability: Headline-worthy hacking – full story still TBD, but illustrates the risk

- Recent reports of malicious interdiction in Supermicro server boards assembled in China
- Very broadly used in commercial and government systems (Amazon, Apple, CIA, etc.)
- High functionality components miniaturized, hidden, and disguised as other components
- Enable third party to control hardware, apparently done in parallel with SW/FW attacks



Government Focus on Semiconductor Packaging Security

DARPA Microsystems Technology Office (MTO) PMs: Areas of interest => significant interest in security / packaging



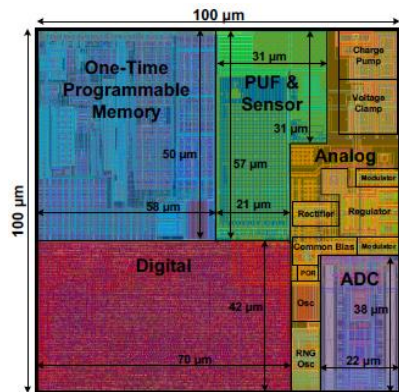
		Areas of Interest (https://www.darpa.mil/about-us/people)																						
		Adaptability	Automation	Communications	Cyber	Decentralization	Electronics	EW	Imagery	Integration	ISR	Leadership	Manufacturing	Materials	Microstructure	Microsystems	Photonics	PNT	Processing	Quantum	Security	Sensors	Spectrum	
MTO PM	Joined	2	2	2	2	1	8	3	2	3	1	1	3	5	1	5	3	2	1	1	2	5	7	Packaging Interests
Griffin, Ben	Oct-18						1							1								1	1	extreme environments
Rebello, Keith	Oct-18				1		1							1		1								
Burke, John	Aug-18							1		1							1	1		1		1		
Leef, Serge	Aug-18						1					1				1					1			Supply Chain, Security
Trimberger, Steve	Aug-18		1				1									1					1			Security
Mason, Whitney	Nov-17								1													1	1	
Chen, YK	Sep-17													1		1	1					1		Heterogeneous integration, materials
Keeler, Gordon	Aug-17						1			1						1	1							Photonics
Polcawich, Ron	Aug-17			1									1	1				1						MEMS
Olofsson, Andreas	Jan-17		1				1					1							1					HI, standards, automation, manufacturing
Hancock, Tim	Sep-16					1	1	1															1	Heterogeneous integration
Rondeau, Tom	May-16	1		1																			1	
Plaks, Ken	Jan-15				1			1						1										Security
Tilghman, Paul	Dec-14										1												1	
Lewis, Jay (DD)	Nov-14								1													1	1	
Salmon, Linton	Sep-14						1					1												Manufacturing, foundries
Chappell, Bill (OD)	Jun-14	1								1		1											1	

Another Approach to Trust: SHIELD uses advanced assembly technology to verify a full assembly

Challenge and response to verify presence of trusted SHIELD dielet within



SHIELD Key Components

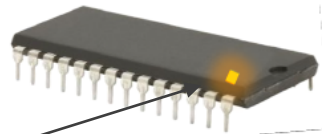


Dielet floorplan (Northrop Grumman)
14nm CMOS

Key SHIELD Specifications

- Unique Key Storage
- Full 256-bit AES encryption engine
- Unpowered, passive intrusion sensors
- RF power and communication
- Transfer fragility
- 100µm x 100µm
- 50 µW Total Power
- Operating temp < 120°C
- Cost < \$0.01 per dielet

Dielet



Programmed on-reticle after manufacture

Installed on or within host IC package

- Embedded within package
- Custom package
- Epoxy to surface

No impact to host IC performance or reliability

Reader



Transmits at 5.8GHz to power dielet; 3.6GHz for data transfer

USB connection to smartphone, tablet or computer

Can be configured for high-volume interrogation (transaction time < 1 sec)

Remote Server



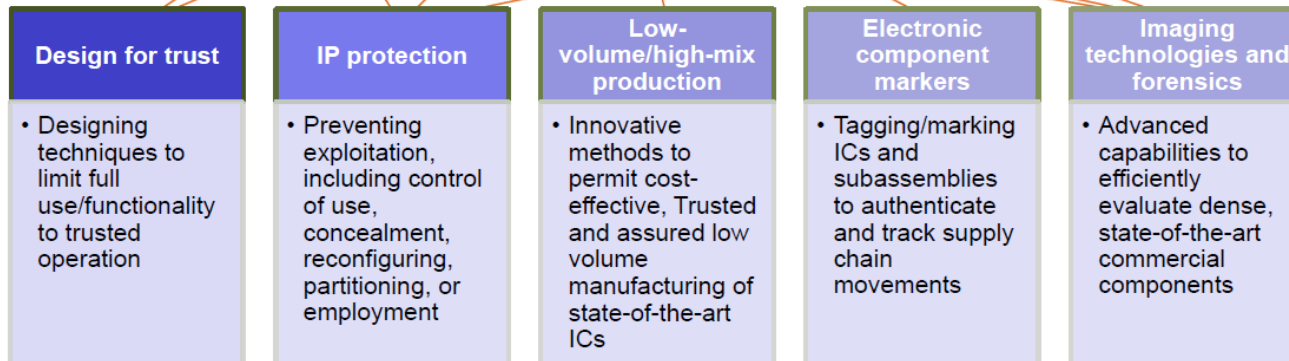
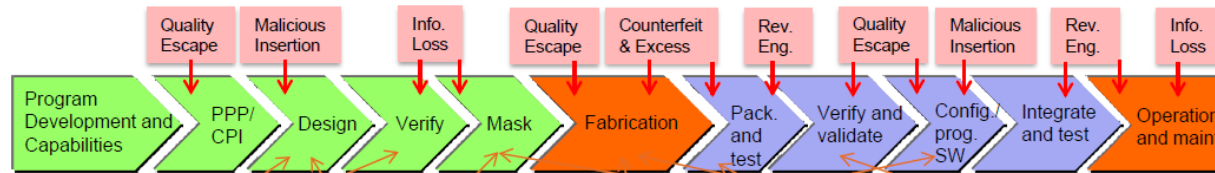
Communicates with reader via Internet connection; performs using Amazon and Microsoft web services

Maintains a record for each IC

- Manufacture date
- Part/package information
- Interrogation history

Microelectronics Innovation for National Security and Economic Competitiveness (MINSEC): Packaging is critical part of security

T&AM New Trust and Assurance Approaches



Implement and demonstrate assurance capability with transition partners

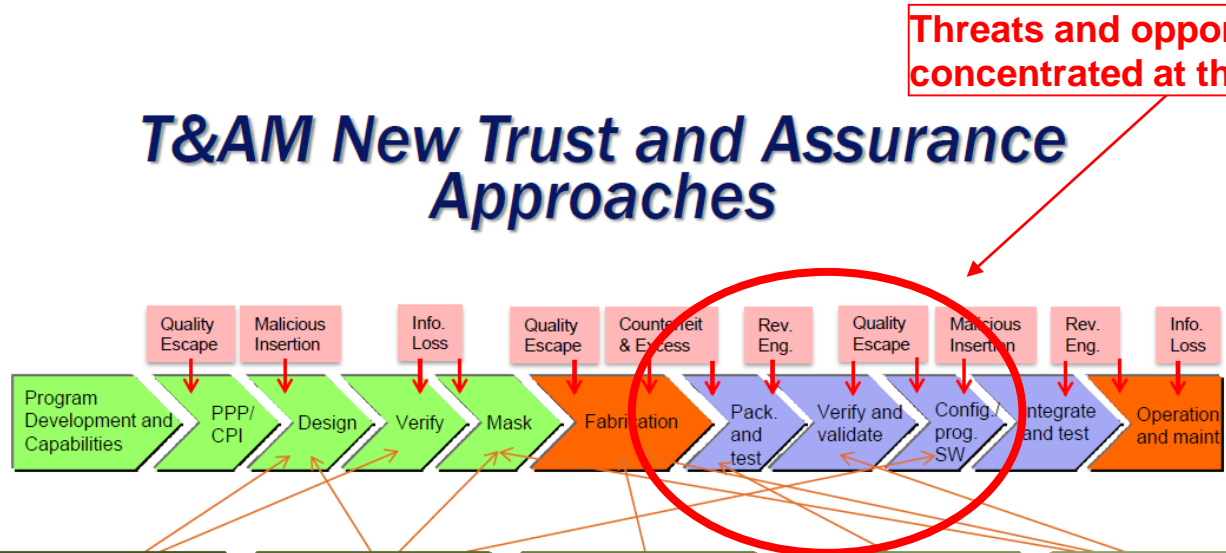


Domestic Foundry & Packaging

- Multiple competitive State-of-the-Art Foundries on shore
- Leadership in R&D and production
- Strong commercial business models
- Government business model for innovation & assurance

Microelectronics Innovation for National Security and Economic Competitiveness (MINSEC): Packaging is critical part of security

T&AM New Trust and Assurance Approaches



Threats and opportunities concentrated at the back end



Solutions needed where all pieces come together

- Design for trust**
 - Designing techniques to limit full use/functionality to trusted operation
- IP protection**
 - Preventing exploitation, including control of use, concealment, reconfiguring, partitioning, or employment
- Low-volume/high-mix production**
 - Innovative methods to permit cost-effective, Trusted and assured low volume manufacturing of state-of-the-art ICs
- Electronic component markers**
 - Tagging/marking ICs and subassemblies to authenticate and track supply chain movements
- Imaging technologies and forensics**
 - Advanced capabilities to efficiently evaluate dense, state-of-the-art commercial components

- ### Domestic Foundry & Packaging
- Multiple competitive State-of-the-Art Foundries on shore
 - Leadership in R&D and production
 - Strong commercial business models
 - Government business model for innovation & assurance

Implement and demonstrate assurance capability with transition partners

Office of the Secretary of Defense, July 2019



Competitive Opportunities



Opportunity	Open Date	End Date	Reference
State of the Art (SOTA) Heterogeneous Integrated Packaging (SHIP) Prototype	3 Jul 2019	6 Aug 2019	https://s2marts.org/ Contact: S2MARTS@nstxl.org
Rapid Assured Microelectronics Prototypes using Commercial Design & Intellectual Property	4th Qtr FY19	-----	https://s2marts.org/ Contact: S2MARTS@nstxl.org
Microelectronics Innovation for Next- generation System Advancement and Validation (MINSAV) Advanced Research Announcement Advanced Technology Center (ATC) for Data Processing	4th Qtr FY19	-----	https://www.cto.mil/work-with-us/
Assured and Trusted Microelectronics Solutions (ATMS) Broad Agency Announcement (BAA)	Jan 2017	Nov 2022	FedBizOps Solicitation Number: FA8650-18-S-1201
Rapid Innovation Fund (RIF) Broad Agency Announcement (BAA)	4th Qtr FY19	-----	https://www.cto.mil/work-with-us/

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State of the art Heterogeneous Integrated Packaging (SHIP)

This Request for Solutions is anticipated to result in two awards, with each award respectively related to the focus areas below:

1) SHIP Digital: State of the Art Digital Design Center and Integrated Packaging and Assembly Test Center; and,

2) SHIP RF: State of the Art RF Design Center and Integrated Packaging and Assembly Test Center.

Item No.	Item/Deliverable	Quantity / Frequency	Deliverable Due Date
1	<p>Phase 1 SHIP Report</p> <p>Comprised of Technical & Business Plans discussing the phases below:</p> <ul style="list-style-type: none"> • <u>Phase 2</u>: <i>Advanced Prototype Capability Development and Initial Design Activities</i>; • <u>Phase 3</u>: <i>Install and Qualification of Processes</i>; • <u>Phase 4</u>: <i>Operate and Maintain Advanced Prototype Capability</i> 	1 / Once	<u>No Later Than six (6) months from project award.</u>

State of the art Heterogeneous Integrated Packaging (SHIP)

This Request for Solutions is anticipated to result in two awards, with each award respectively related to the focus areas below:

- 1) SHIP Digital: State of the Art Digital Design Center and Integrated Packaging and Assembly Test Center; and,
- 2) SHIP RF: State of the Art RF Design Center and Integrated Packaging and Assembly Test Center.

\$25M for a six-month paper study!

Item No.	Item/Deliverable	Quantity / Frequency	Deliverable Due Date
1	Phase 1 SHIP Report	1 / Once	No Later Than six

Current Project Budget: \$25,000,000 is budgeted and available for the Phase 1 awards, while subsequent Phases will be funded upon successful completion of the previous Phase.

	<ul style="list-style-type: none"> • <u>Phase 2</u>: <i>Advanced Prototype Capability Development and Initial Design Activities;</i> • <u>Phase 3</u>: <i>Install and Qualification of Processes;</i> • <u>Phase 4</u>: <i>Operate and Maintain Advanced Prototype Capability</i> 		
--	--	--	--

SHIP Advanced Prototype Capability Concept

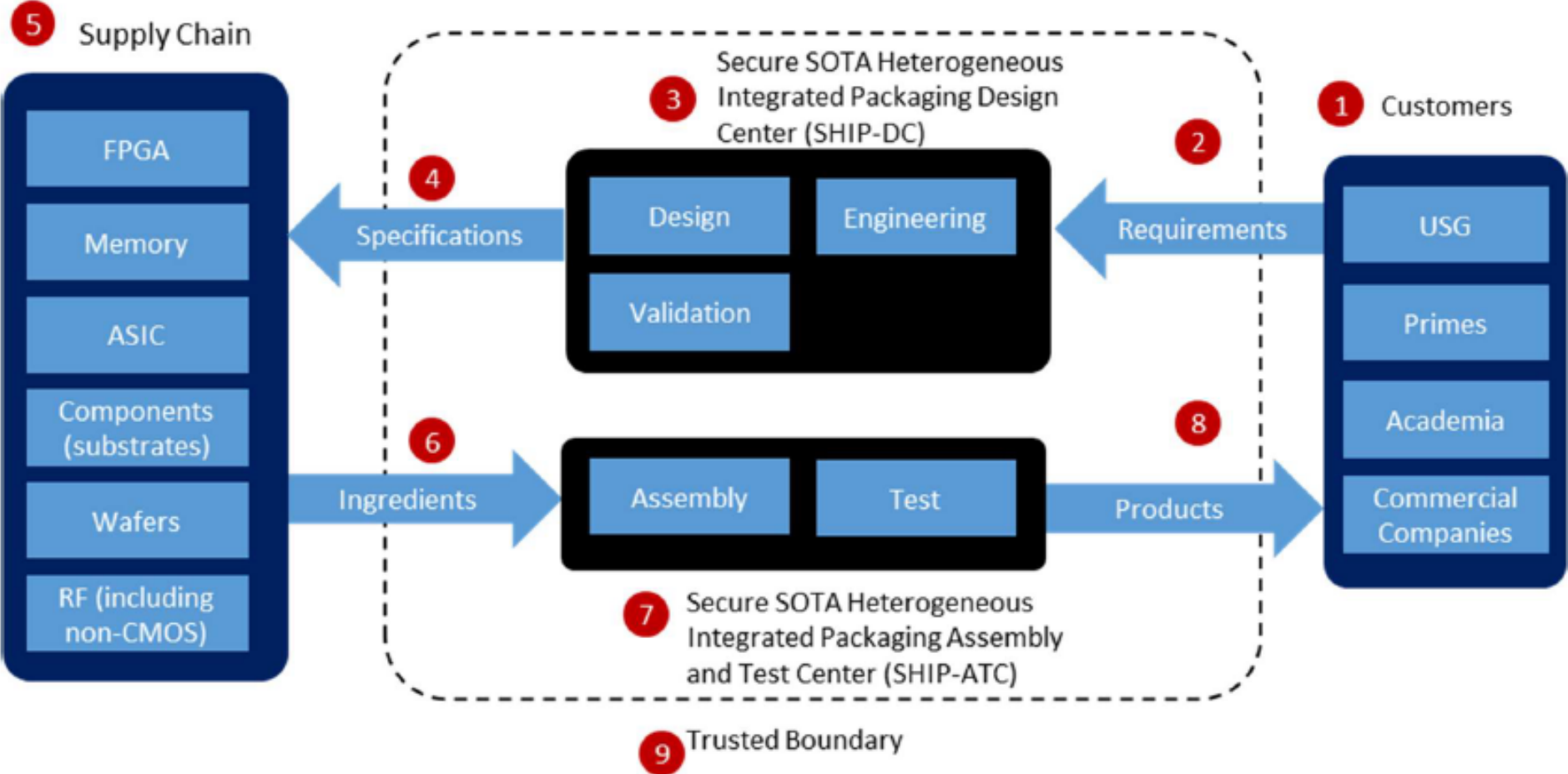


Figure 1 Notional design and prototype manufacturing flow

SHIP Capabilities

Table 3 General Capacity and Capability for the SHIP-ATC

Category	IOC	FOC	Scale
Capacity: Volume	1k+	10k+	100k/mo+
Silicon interposer	Required	Required	Required
Organic interposer	Preferred	Required	Required
Utilize SOTA COTS FPGA ¹ and programmable devices	Required	Required	Required
Structured ASIC	Preferred	Preferred	Required
Security	Trust	ITAR	Classified
Number of Chips/Package ²	4	8	12+
Supply Chain target	>50% US	>75% US	>90% US
Can process singulated die	Required	Required	Required
Can process up to 300mm wafers	Preferred	Required	Required
Can process 200mm die	Preferred	Preferred	Required

¹ Must include ability to integrate and test SOTA FPGA (<14nm), not required for RF centric applications

² Could include, but not limited to, memory, ADC/DAC, transceivers, optical couplers, ASIC, structured ASICs, etc.

SHIP Interposer Specs

Table 4 Silicon Interposer Foundry Specifications

		IOC	Final State
Size	Interposer Area	26x33mm	(26x33mm) X 2 with stitching (1)
Front-side	Wiring Density	1000-1600 IO/mm	1600 IO/mm (2)
	Metal Layers	(0.4/1.08/4.0) μm (1.08/1.08/4.0) μm	(0.4/1.08/4.0) μm (1.08/1.08/1.08/4.0) μm
	Bump Pitch	50μm	36μm
Middle	TSV Pitch	55μm Min	45μm Min
Back-side	Bump Pitch	55μm Min	45μm Min

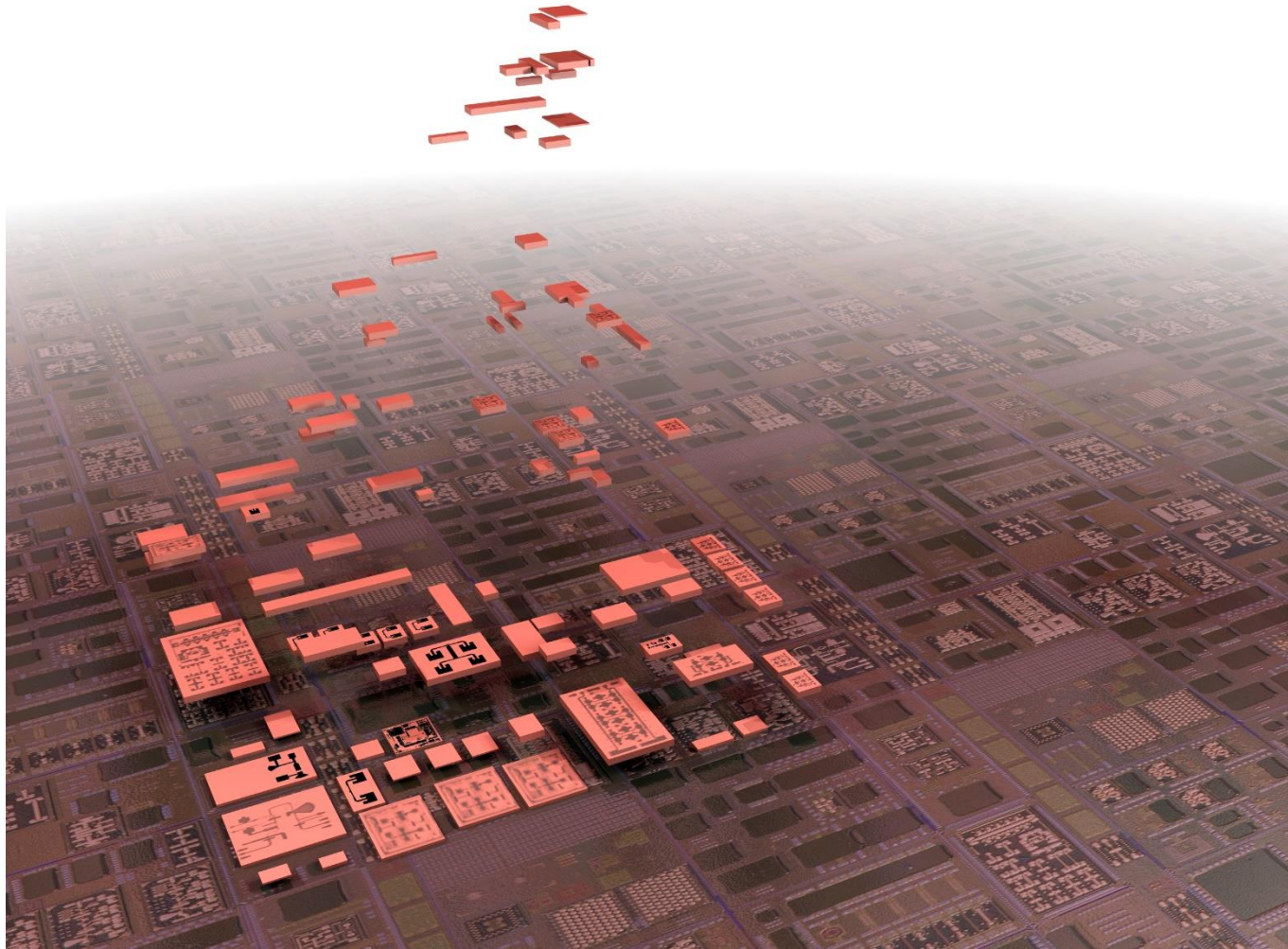
SHIP Assembly Specs (sample)

Table 6 Advanced Microelectronics Assembly Specifications

		IOC	Final State
		IOC	FOC
Chip on Chip	Silicon Interposer Sizes	(22 x 33) mm	(22 x 33) mm
	Top Chip Process	All leading processes from 180nm to 7nm	
	Chip Size Range	(2 x 2) mm to (21 x 32) mm	(1 x 1) mm to (21 x 32) mm
	Chips Placed Per Interposer	20	
	Chip Spacing	100 μm	100 μm
	Chip Bump Pitch	50 μm	36 μm
	Total Connections		
	Number of chips in 3D stack	21 (estimate only)	> 21 (estimate only)
Chip on Substrate	Max Organic Substrate Sizes	(76 x 74) mm	(100 x 100) mm
	Substrate C4 Bump Pitch	55 μm	45 μm
	Chips Placed Per Substrate	7	12
	Chip Spacing	100 μm	100 μm
Packaging	Features	<ul style="list-style-type: none"> • High performance polymer and solder thermal interface materials integrated with Cu heat spreaders for improved thermal performance • Package substrates that are optimized for low loss high speed signaling 	



Future of heterogeneous integration



Requires a lot of pieces coming together!