Government Investment in Heterogeneous Integration

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Innovate Forward
Booz | Allen | Hamilton
100 YEARS

Image courtesy of Athena Group

Government Investment in Heterogeneous Integration

- Past
  - Background and history
  - DAHI (Diverse Accessible Heterogeneous Integration)
- Present
  - CHIPS (Common Heterogeneous Integration and IP Reuse Strategies)
  - ERI (Electronics Resurgence Initiative)
- Future
  - Security and Trust Issues
  - MINSEC (Microelectronics Innovation for National Security and Economic Competitiveness)
  - SHIP (State of the art Heterogeneous Integrated Packaging)

Past

No "Perfect" Material

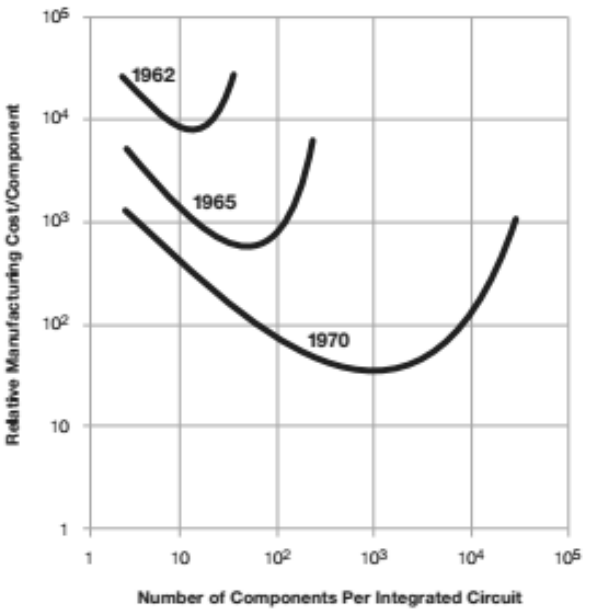
			← device materials →					integration
Parameter	**Why?**	**Unit**	**Si**	**GaAs**	**InP[1]**	**GaN[2]**		**COSMOS / DAHI**
Electron Mobility	**Carrier velocity**	**10^3 cm²/V·s**	**1.4**	**8.5**	**12**	**<1**		**InP**
V_{peak}	**Transit time**	**10^7 cm/s**	**1**	**2**	**2.5**	**2.5**		**InP / GaN**
E_{BK}	**Voltage swing**	**10^5 V/cm**	**5.7**	**6.4**	**4**	**40**		**GaN**
E_g	**Charge density**	**eV**	**1.12**	**1.42**	**0.74**	**3.4**		**GaN**
κ	**Heat removal**	**W/cm·K**	**1.3**	**0.5**	**0.05**	**2.9**		**GaN / Si**
Maturity	**Circuit complexity**		**Excellent**	**Good**	**OK**	**Limited**		**Si + GaN + InP (heterogeneous)**
DARPA Investment			**~$100M**	**~$600M**	**~$200M**	**~$300M**		**~$180M**
Programs			**Portions of GRATE, ADRT, LPE, and TEAM**	**MIMIC**	**SWIFT, TFAST, THz Electronics, SMART**	**GaN Title III, WBGS-RF, NEXT, MPC, NJTT**		**COSMOS, DAHI**

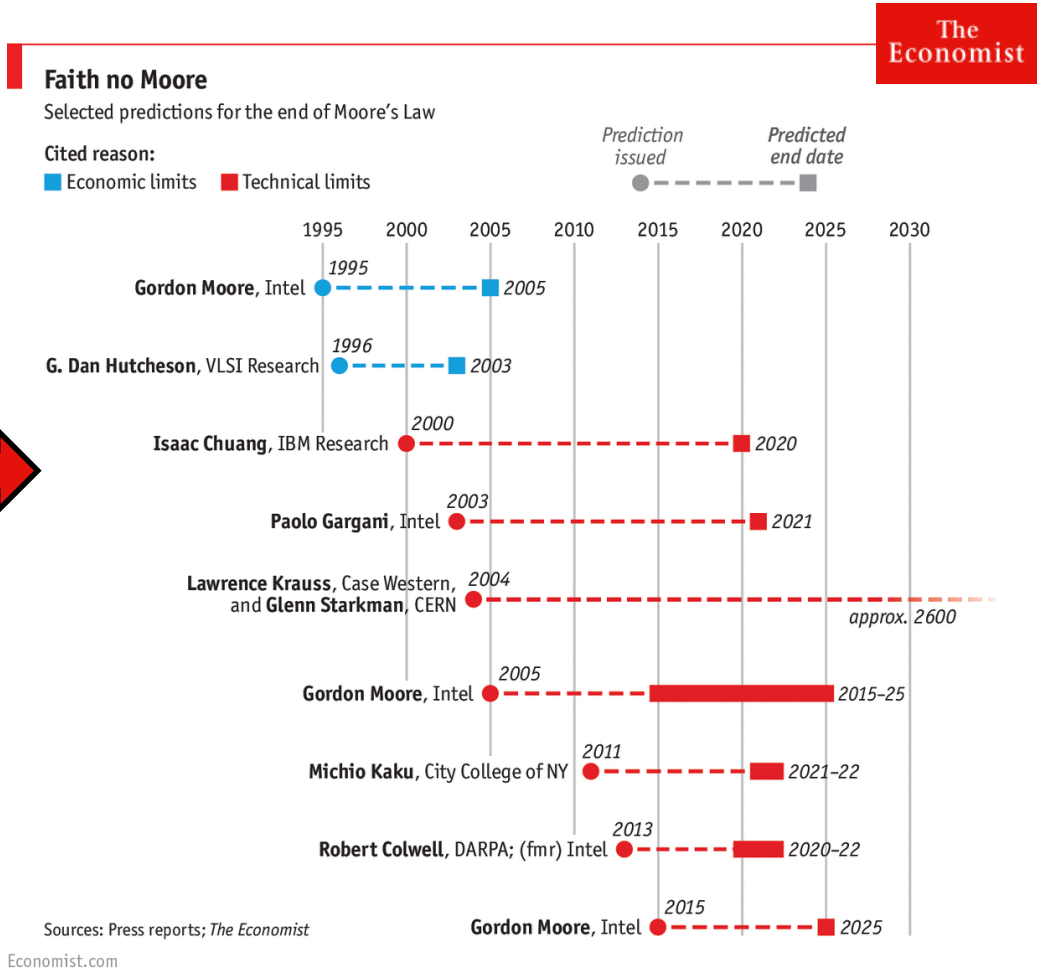
Materials and device parameters favor a diversity of semiconductors

1. InGaAs channel
2. SiC substrate

End of Moore's Law?

Moore's Law





Changes in silicon industry will be felt by compound semiconductors

Source: Electronics Magazine, Economist.com

Moore's paper INCLUDES Heterogeneous Integration

It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected. The availability of large functions, combined with functional design and construction, should allow the manufacturer of large systems to design and construct a considerable variety of equipment both rapidly and economically.

The experts look ahead

Cramming more components onto integrated circuits

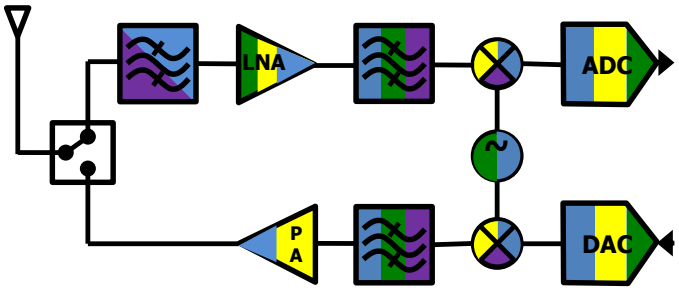
With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

By Gordon E. Moore

Director, Research and Development Laboratories, Fairchild Semiconductor division of Fairchild Camera and Instrument Corp.

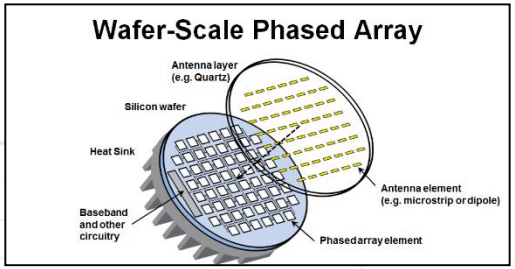
G. E. Moore is one of the new breed of electronic engineers, schooled in the physical sciences rather than in electronics. He earned a B.S. degree in chemistry from the University of California and a Ph.D. degree in physical chemistry from the California Institute of Technology. He was one of the founders of Fairchild Semiconductor and has been Director of the research and development laboratories since 1959.

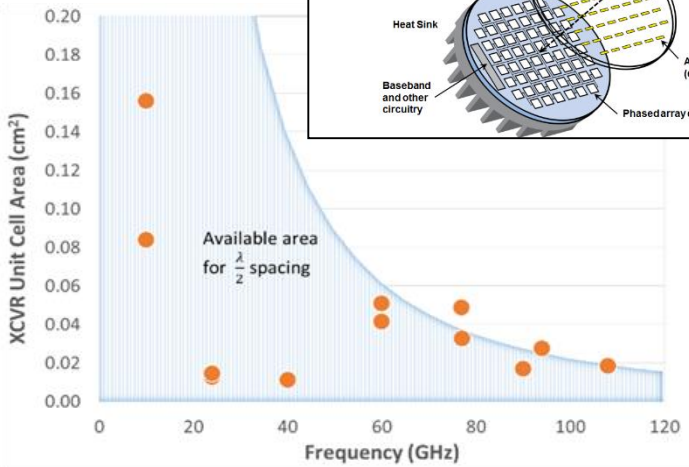
Why Heterogeneous Integration?



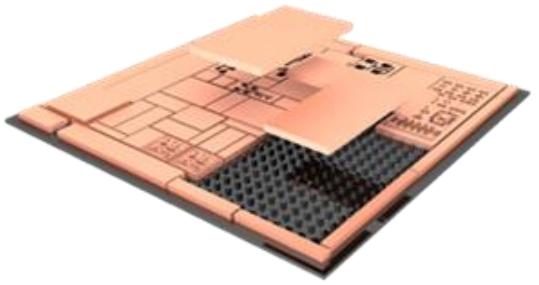
Si CMOS/SiGe BiCMOS
InP HBTs/HEMTs
GaN HEMTs
RF MEMS/High-Q passives

Best of breed technology





Density of integration



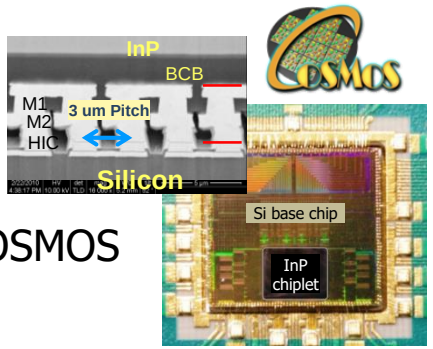
Modular design

Sources: DARPA, UCSD

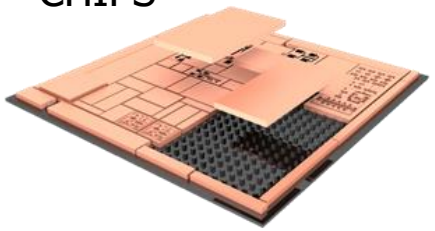
DARPA's long history of innovation in integration

ASEM

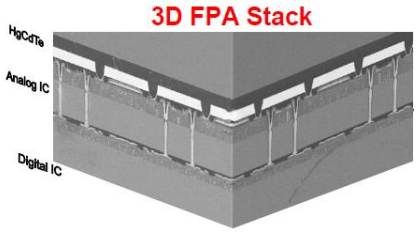
COSMOS



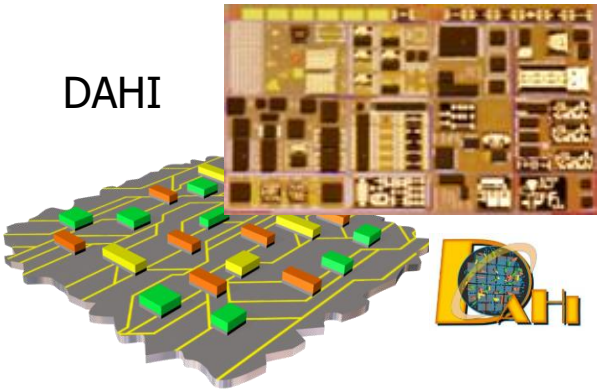
CHIPS



VISA

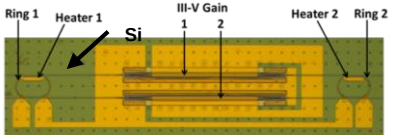


DAHI

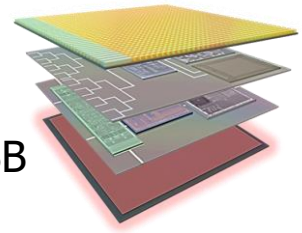


3D-IC

E-PHI



MOABB

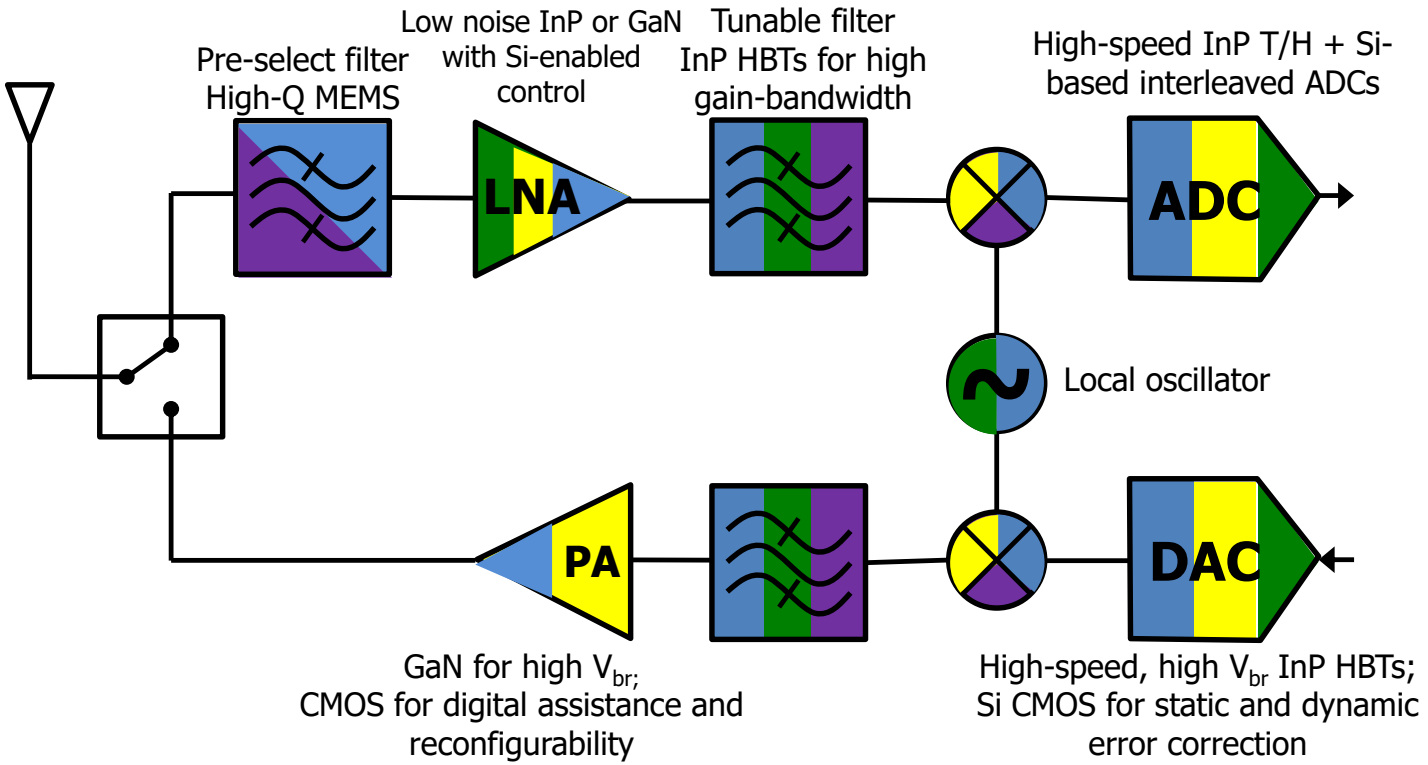


ASEM: Application Specific Electronic Modules
E-PHI: Electronic-Photonic Heterogeneous Integration
VISA: Vertically Integrated Sensor Arrays
COSMOS: Compound Semiconductor Materials on Silicon
DAHI: Diverse Accessible Heterogeneous Integration
MOABB: Modular Optical Aperture Building Blocks
CHIPS: Common Heterogeneous Integration and IP Reuse Strategies

1990s 2000s 2010s 2020s

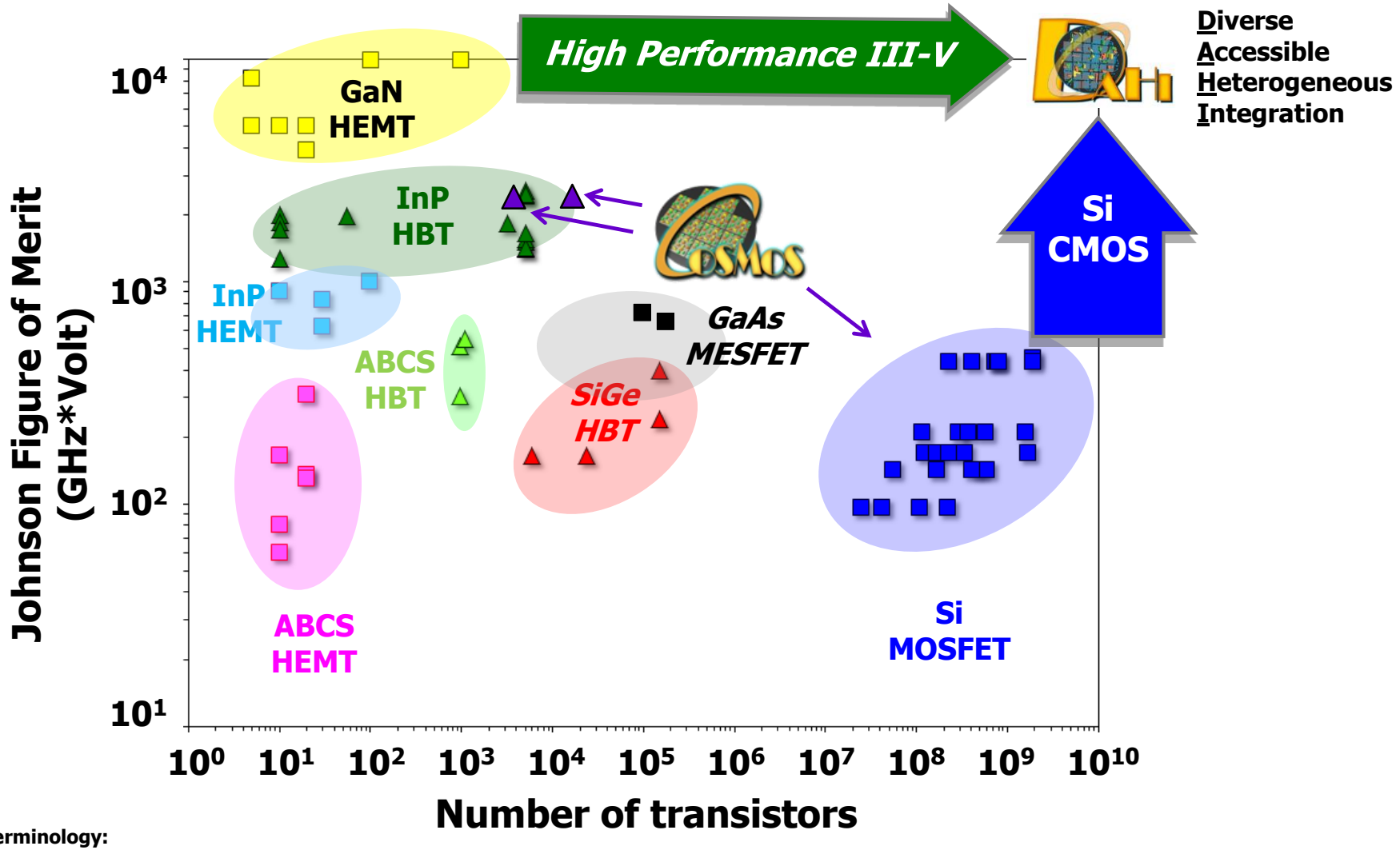
Sources: DARPA, Smithsonian Chips

Vision for Representative Transceiver: 4+ Device Technologies



Legend:
- Si CMOS/SiGe BiCMOS
- InP HBTs/HEMTs
- GaN HEMTs
- RF MEMS/High-Q passives

Heterogeneous Integration: DAHI Broadens the Device Material Options



Terminology:
InP = indium phosphide, GaN = gallium nitride, SiGe = silicon germanium, ABCS = antimonide-based compound semiconductor
HBT = heterojunction bipolar transistor, HEMT = high electron mobility transistor, CMOS = complementary metal oxide semiconductor
COSMOS = Compound Semiconductor Materials on Silicon

COSMOS Program Showed the Promise of Heterogeneous Integration

Transistor-scale Integration Technology

Yield Enhancement & Circuit Integration

Advanced Circuits

# of Heterogeneous Interconnects

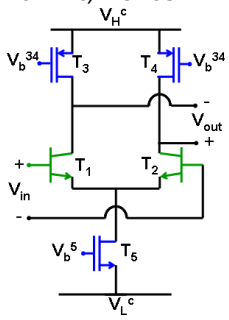
1000

100

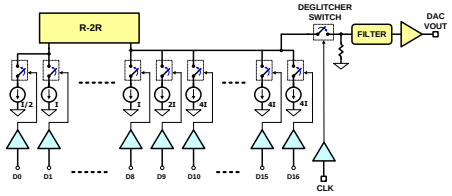
10

Differential amplifier ✓

- ***~10 heterogeneous interconnects (HICs)***
- *≤ 5μm HIC length and pitch*
- *~5 HBTs, 4 CMOS*

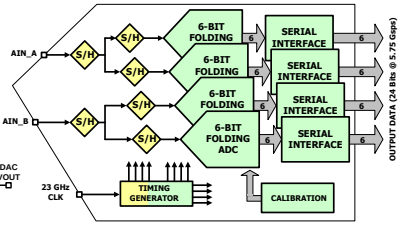


D/A converter ✓



- ***~500 HICs***
- *~400 HBTs, 3200 CMOS.*

A/D converter ✓



- ***~1800 HICS.***
- *~1000HBTs, 18000 CMOS*

integration	Phase I	Phase II/III
monolithic	✓	X (yield)
epi printing	✓	X (yield)
chiplet	✓	✓

FY07 FY08 FY09 FY10 FY11 FY12 FY13

✓ **COSMOS Phase I completed** → ✓ **COSMOS Phase II completed** → ✓ **COSMOS Phase III completed**

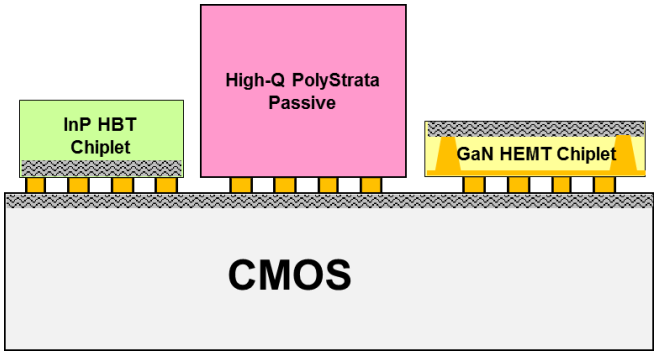
COSMOS[1]:

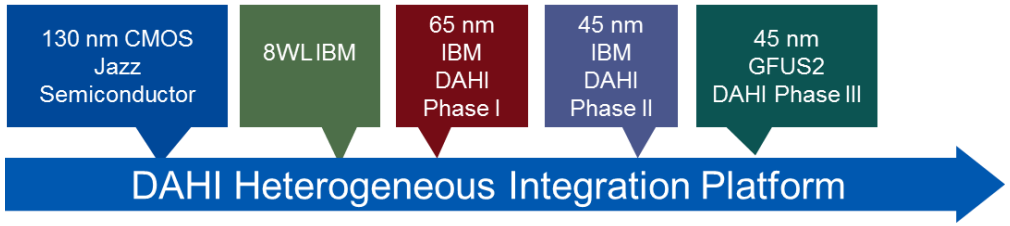
1. **Developed technology for intimate integration of III-Vs and Si.**
2. **Demonstrated world-record capabilities with heterogeneous circuits:**
   a. **Differential amplifier gain-bandwidth**
   b. **DAC SFDR**
3. **Clarified benefits of integration processes that:**
   a. **are scalable,**
   b. **use finished devices, and**
   c. **leverage industry efforts.**

[1]Compound Semiconductor Materials on Silicon

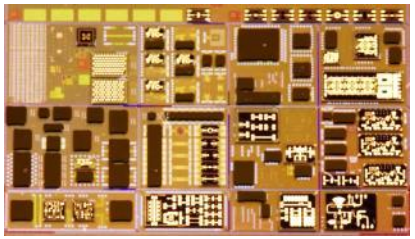
Phase II/III: Demonstrated benefits of integration of completed devices.

DARPA's DAHI program: Silicon CMOS as integration platform

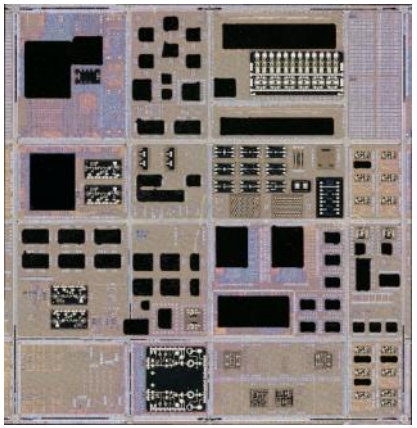




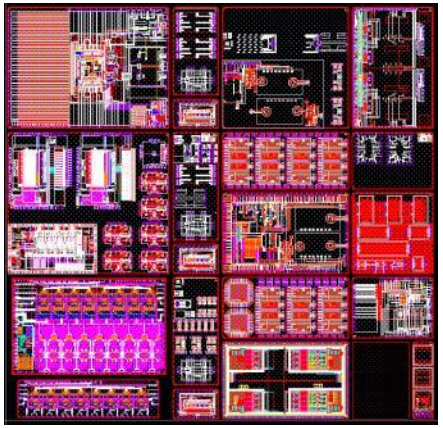
MPW0



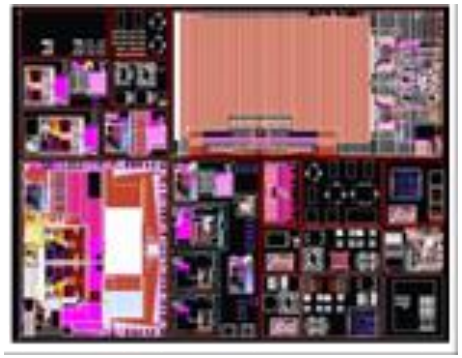
MPW1



MPW2

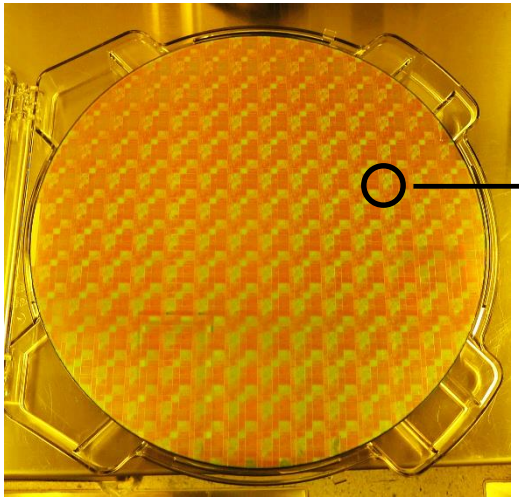


MPW3

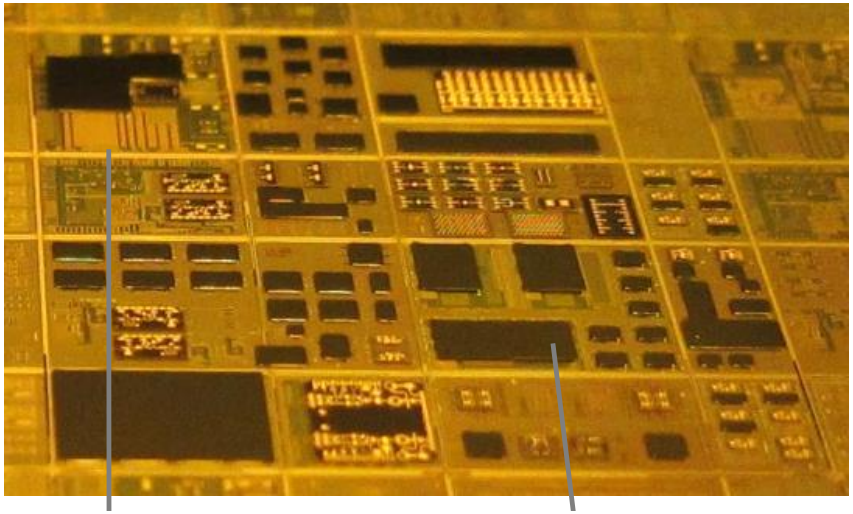


Sources: DARPA, Northrop Grumman

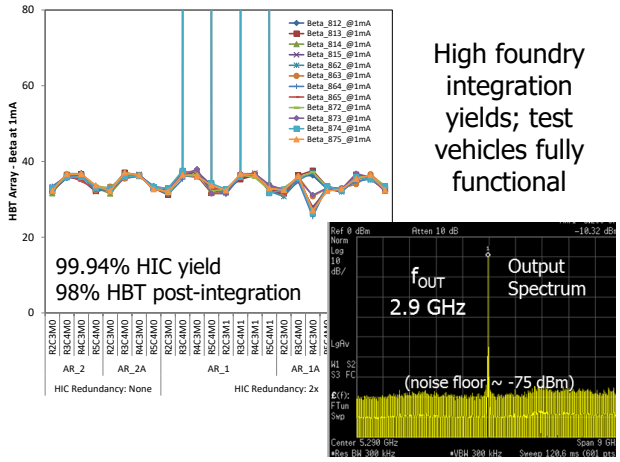
DAHI snapshot:
Excellent yield, demonstrated RF performance



300mm diameter Si CMOS wafer (45nm node)

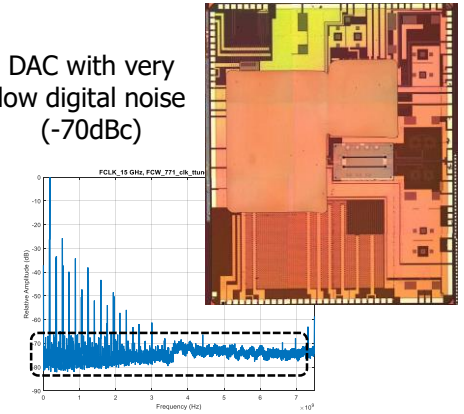


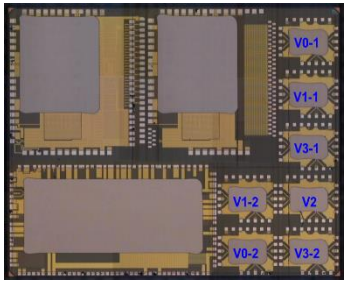
DAHI integration: Si (45nm), InP (TF5 HBT), GaN (GaN20 HEMT)



High foundry integration yields; test vehicles fully functional

DAC with very low digital noise (-70dBc)

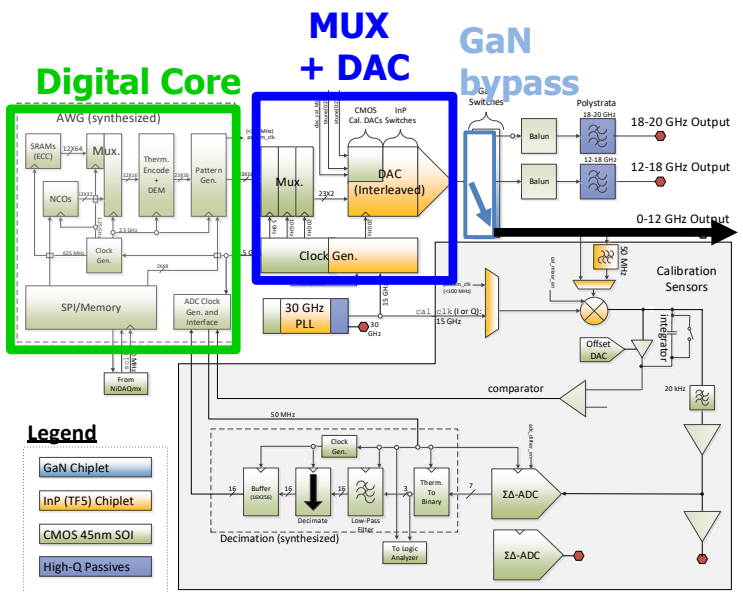


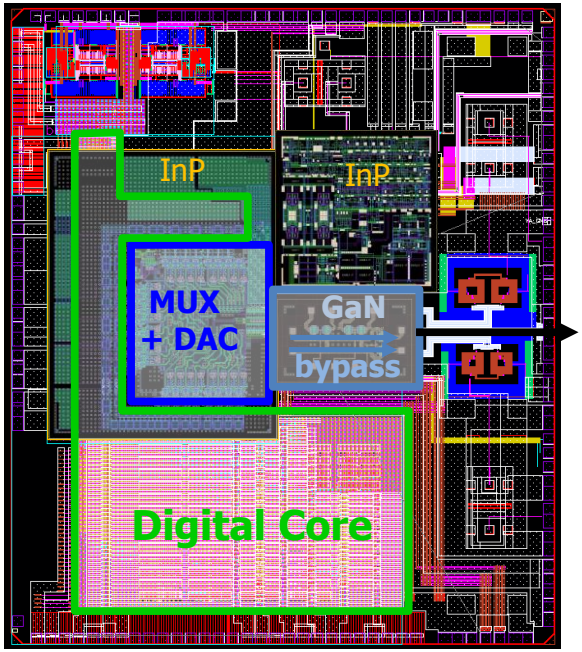


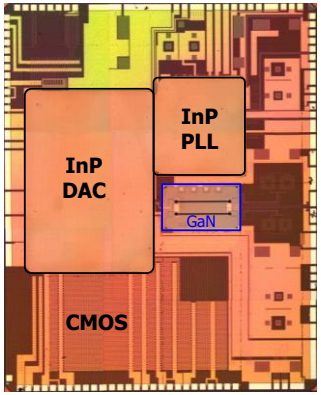
Successful testing identified optimal S/H circuit for ADC (>65dB SFDR @ 2GHz)

Sources: DARPA, Northrop Grumman

DAHI MPW1:
Arbitrary Waveform Generator Enabled by Heterogeneity

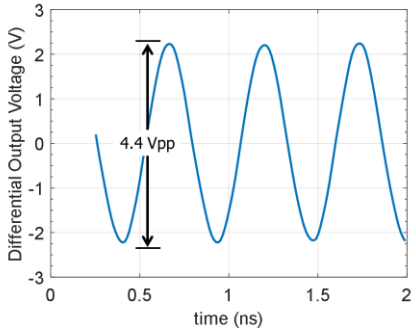


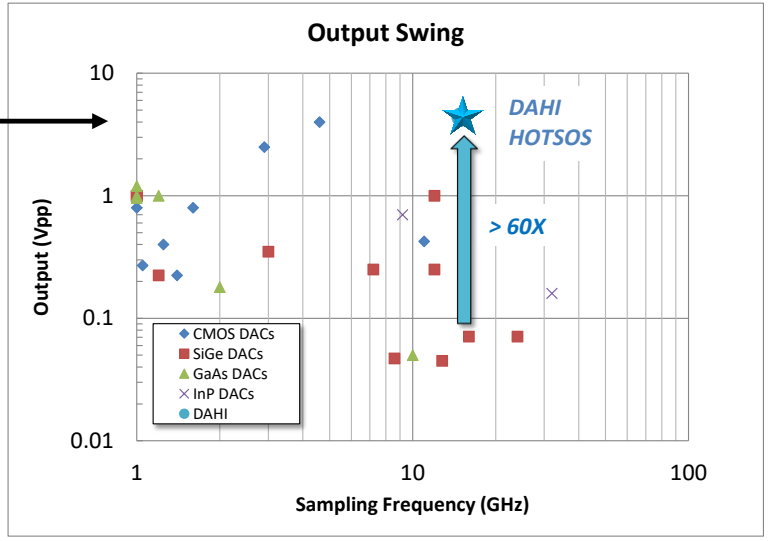




InP + GaN + Si CMOS

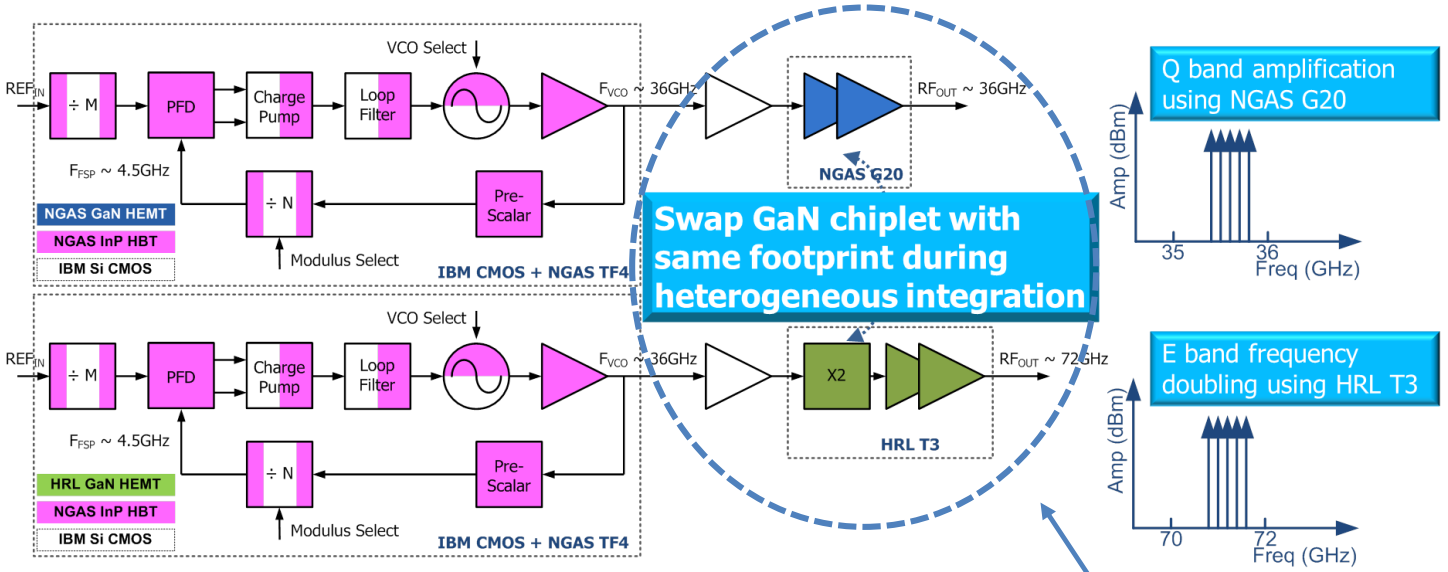
Heterogeneous integration enables unprecedented output swing





DAHI MPW1:
Dual-Band Frequency Synthesizer Demonstrates Modularity

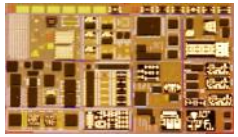
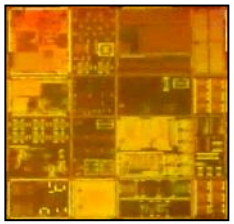
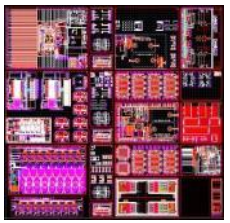
MPW1 Q/E Dual Band Frequency Synthesizer (36 and 72 GHz)

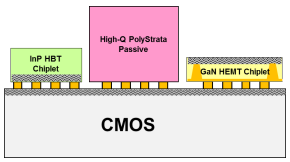


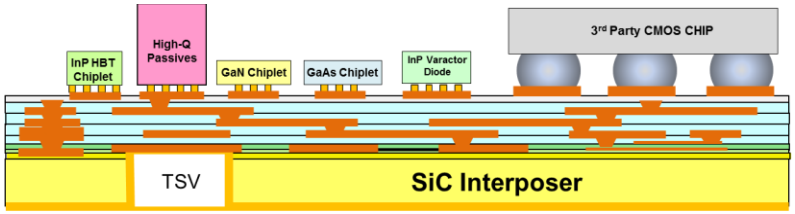
	Function	Freq (GHz)	Technology			
			CMOS 12SOI	InP TF4	GaN G20	GaN T3
A	Amplifier	36			✓	
	Frequency Doubler	72				✓
B	Buffer	36	✓			
C	Buffer + Amp	36	✓		✓	
	Buffer + FD	72				✓
D	VCO + Buffer + Amp	36	✓	✓	✓	
	VCO + Buffer + FD	72	✓	✓		✓
E	Frequency Synthesizer	36	✓	✓	✓	
	Frequency Synthesizer	72	✓	✓		✓

Integration of diverse device technologies enables modular functionality.

DAHI simplicity enables rapid evolution

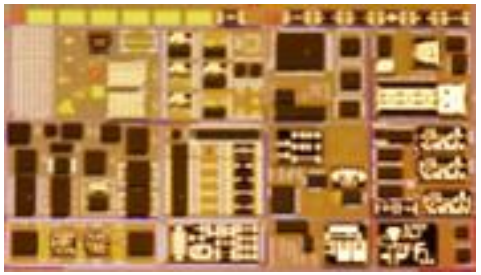
Technology	MPW0	MPW1	MPW2	MPW3	Future MPWs
CMOS	IBM 65nm	GF 45 nm	GF 45 nm	GF 45 nm	GF 45 nm
InP HBT	TF4 (2 metals)	TF4 (3 metals)	TF4 (4 metals)	TF4 (4 metals)	TF4 (4 metals)
		TF5 (3 metals)	TF5 (4 metals)	TF5 (4 metals)	TF5 (4 metals)
InP Varactor Diode					AD1
GaN HEMT	GaN20	GaN20	GaN20	GaN20	GaN20
	T3 (HRL)	T3 (HRL)	T3 (HRL)	T3 (HRL)	T3 (HRL)
GaAs HEMT				P3K6	P3K6
Passive Components		PolyStrata (Nuvotronics)	PolyStrata (Nuvotronics)	PolyStrata (Nuvotronics)	PolyStrata (Nuvotronics)
Base Substrate	CMOS	CMOS	CMOS	CMOS	CMOS
				SiC (IWP5)	SiC (IWP5)
					(in design)



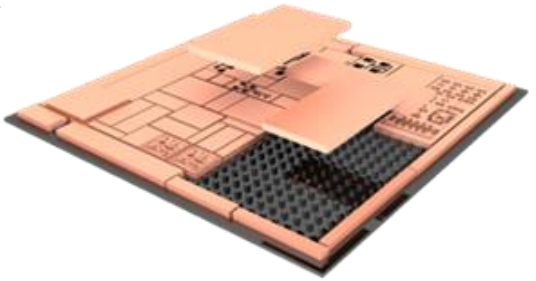


Sources: DARPA, Northrop Grumman

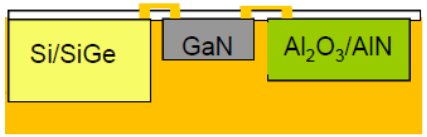
Flavors of heterogeneous integration



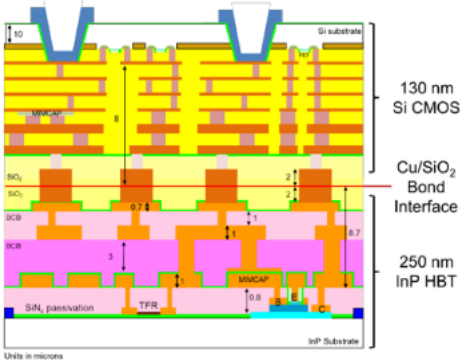
CHIPS: modular design



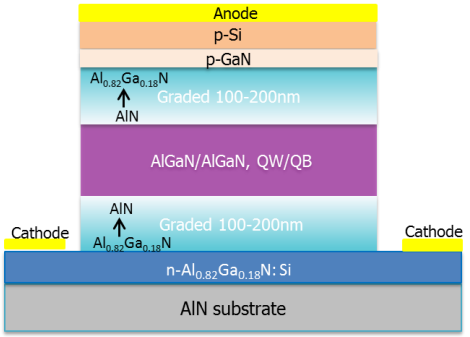
DAHI: RF power



DAHI: wafer scale



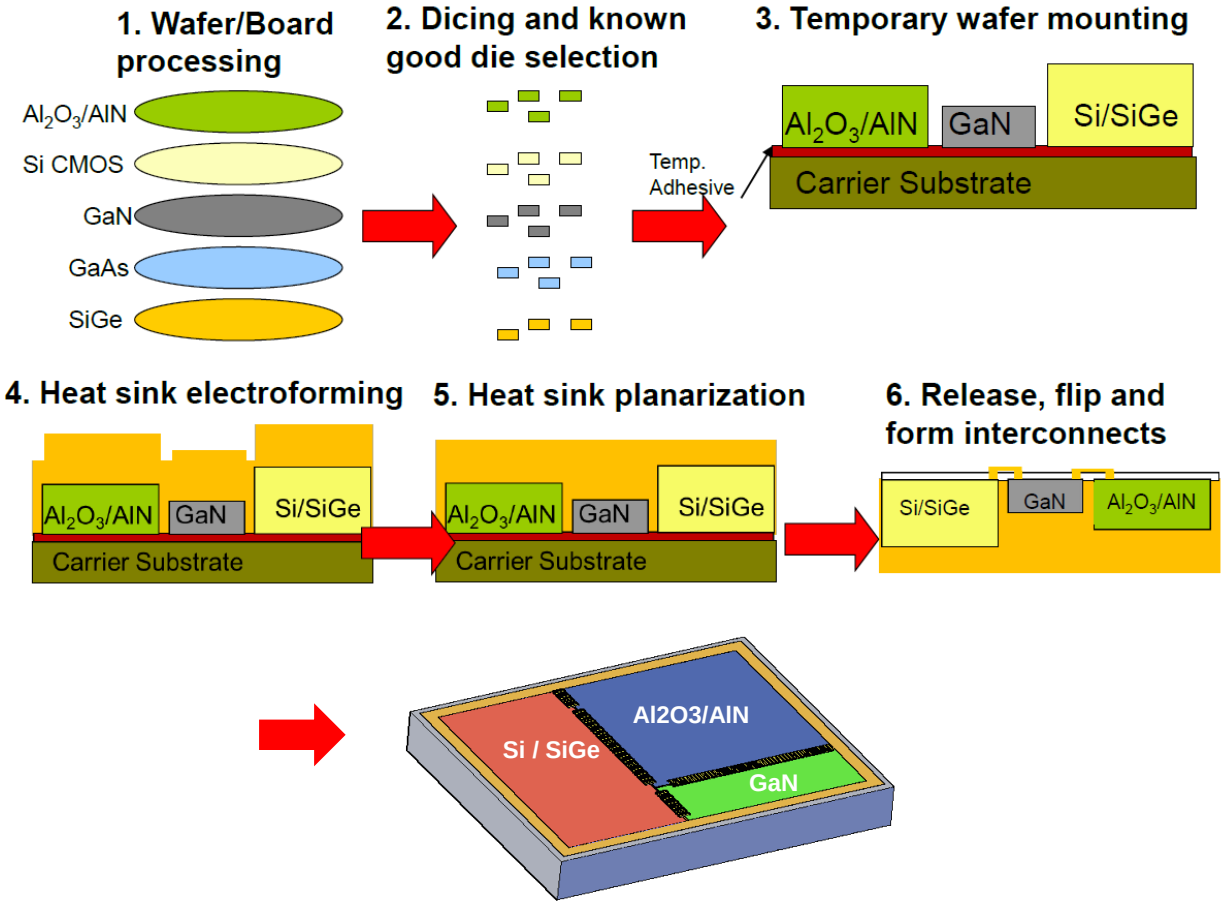
Heterogeneous devices



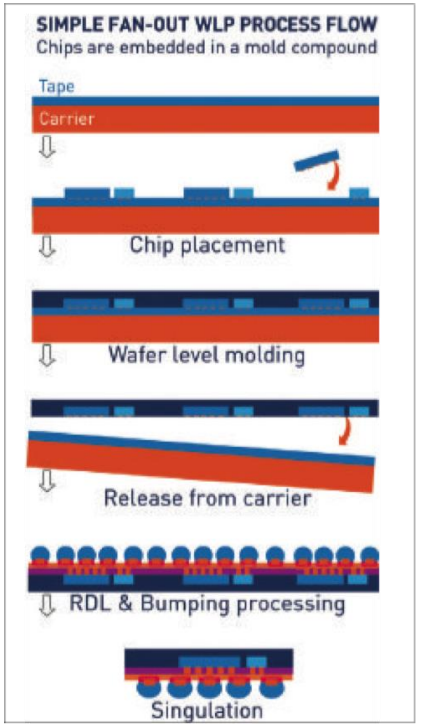
Source: DARPA

Metal Embedded Chip Assembly (MECA)

MECA enables heterogeneous integration with a metal interconnect platform for high-power requirements.



MECA-integrated heterogeneous module



MECA is analogous to wafer-level fan-out packaging technology.

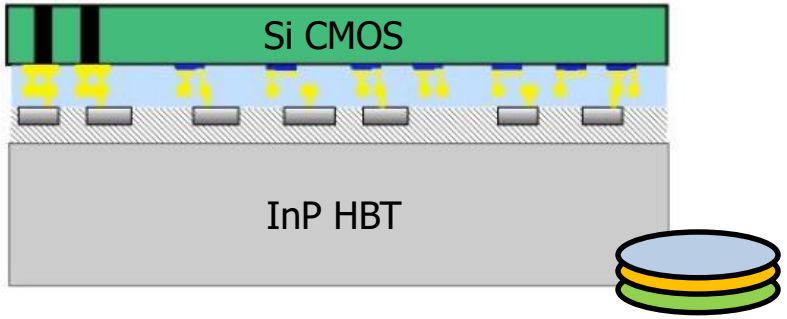
Sources: HRL, Solid State Technology

DAHI chip-scale phased arrays

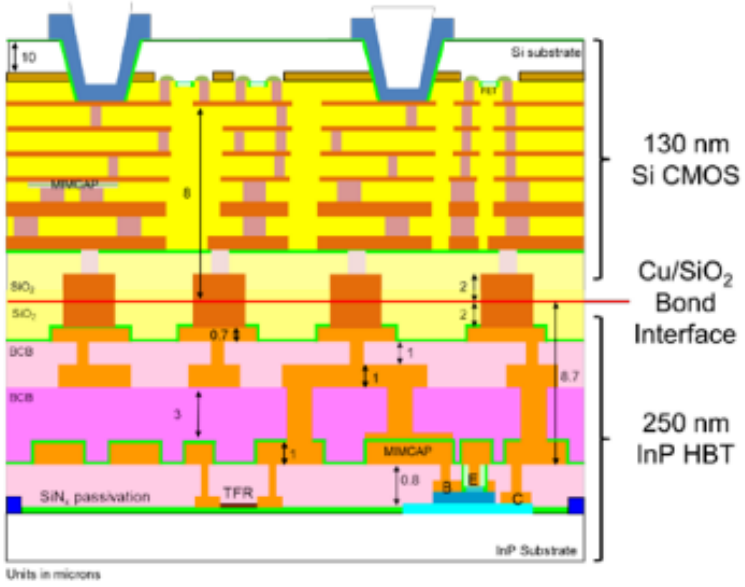
Heterogeneous integration for mm-wave:
Phased array beamformers

- Can maintain λ/2 channel spacing as frequencies increase
- CMOS control circuitry closely integrated with RF chain
- Improved channel performance and efficiency with addition of III-V devices
- Fully integrated beamformer channels demonstrated with integrated InP devices and Si control electronics
- >100mW Pout Tx channel, 4.5 dB NF Rx

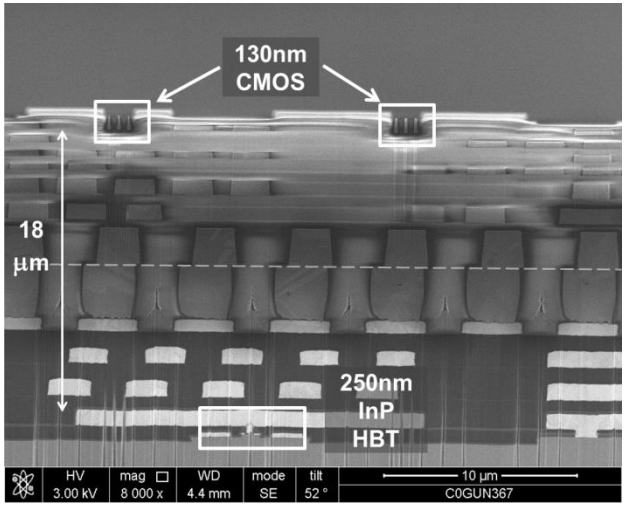
Wafer-level heterogeneous integration



Integration schematic



InP/CMOS with DBI Process

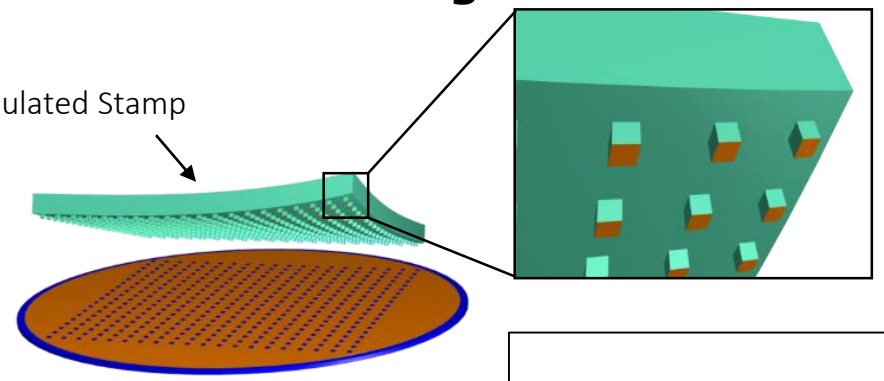


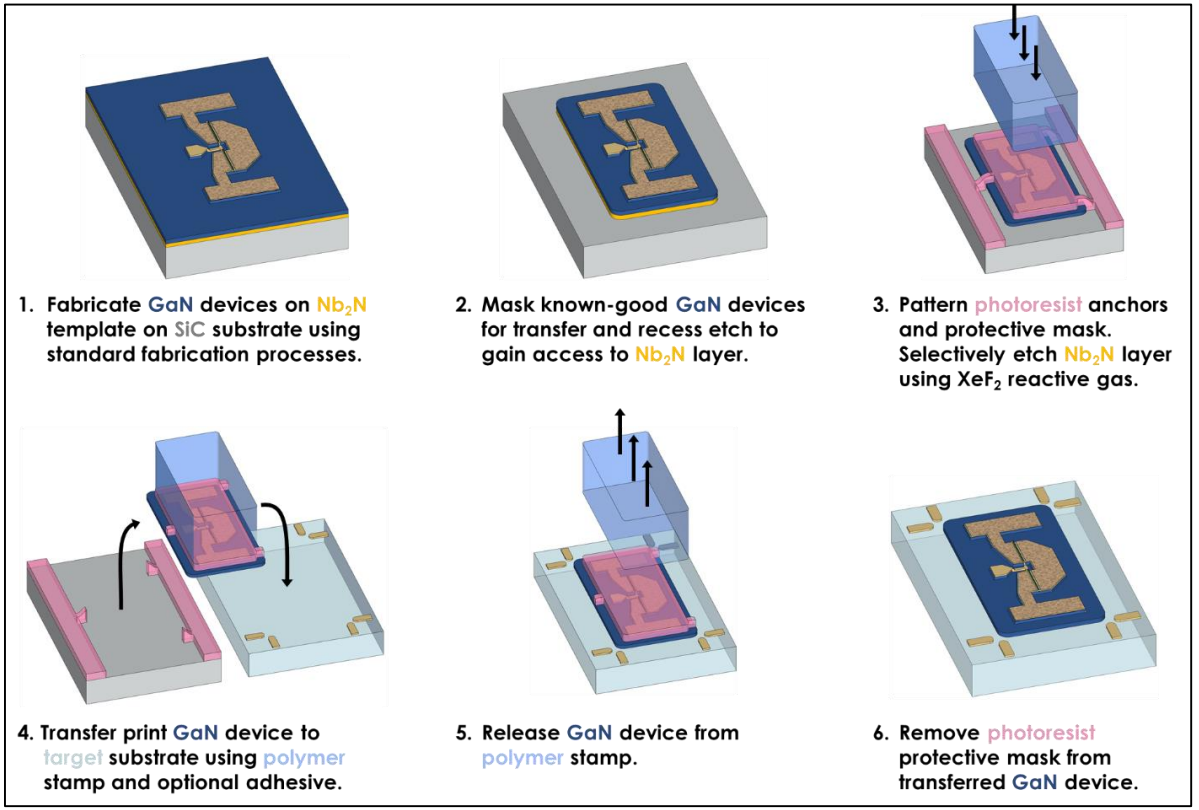
DBI = Direct Bond Interconnect

Source: Teledyne

Advancing integration to the device level

Microtransfer Printing

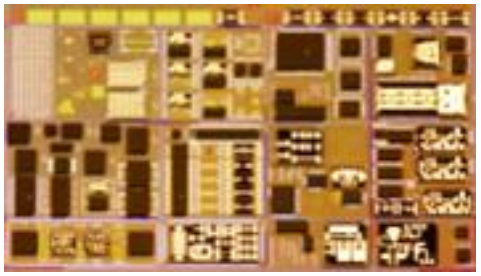




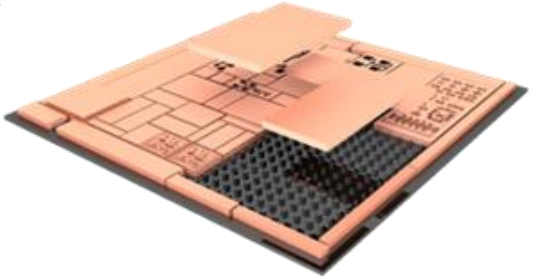
Source: Naval Research Laboratory

Present

Common Heterogeneous Integration and IP Reuse Strategies: CHIPS as the next step in heterogeneous integration

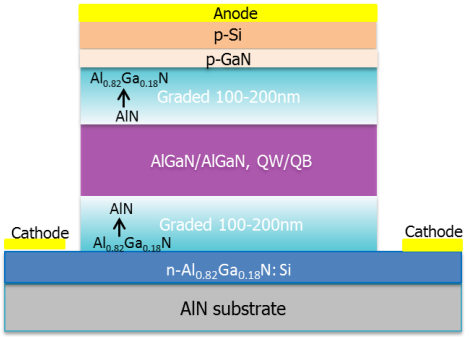


CHIPS: modular design

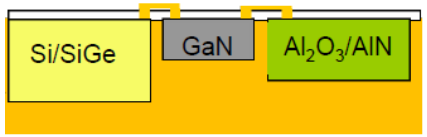


Integration technologies

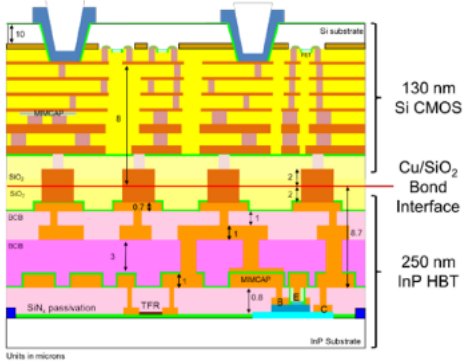
Heterogeneous devices



DAHI: RF power



DAHI: wafer scale



Source: DARPA

Integration impact driven by **Standards** and **Modularity**

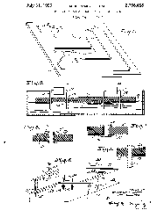
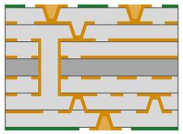
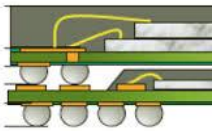


Image: Intel





"Printed circuit board" invented by Paul Eisler.

Early PCB demo in a radio.

First HVM PCBs enable proximity fuze during WWII.

Patent to US Army for PCB assembly.

IPC (Institute for Printed Circuits) founded; standards follow.

Multi-layer PCB invented.

Surface Mount Technology on PCBs revolutionizes manufacturing.

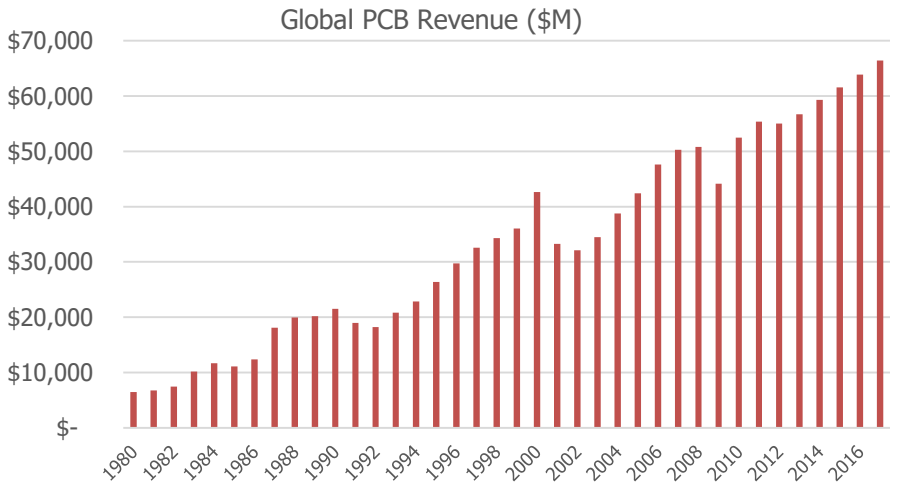
HDI / Microvia technology enables further integration.

First package-on-package standard from JEDEC

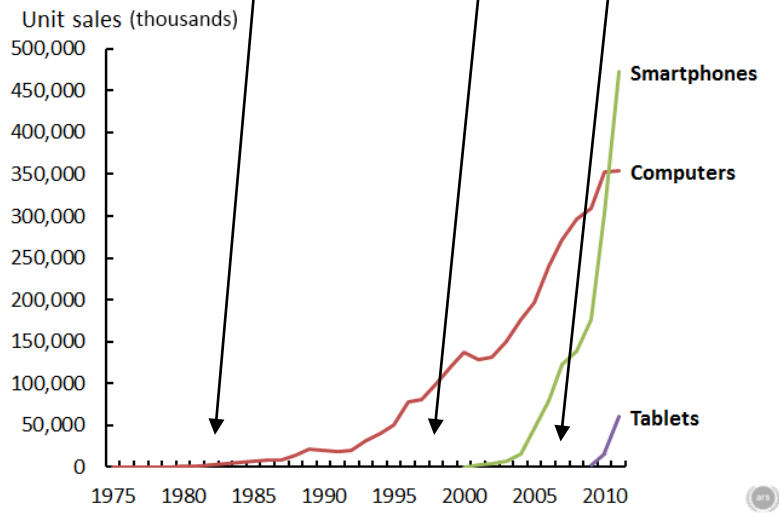
DoD jump-start

1936 1941 1943 1956 1957 1960 1980s 1995 2006

PCB industry sees steady expansion with DoD origins, standardization, and technology development.



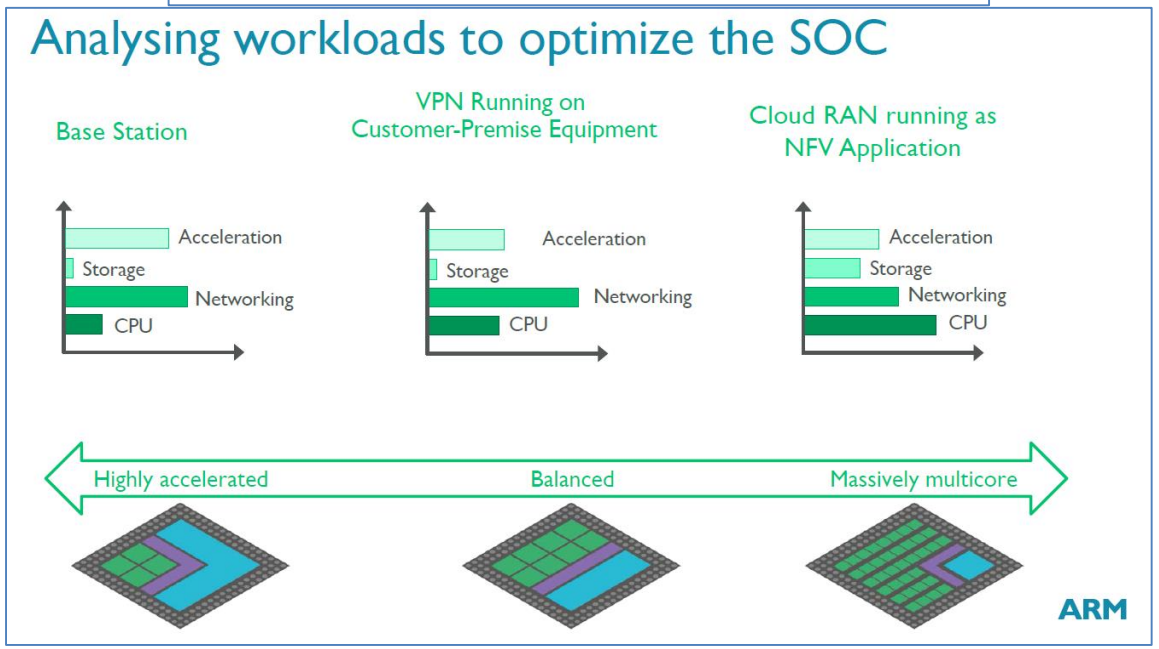
Computers, smartphones, and tablet sales: 1975-2011



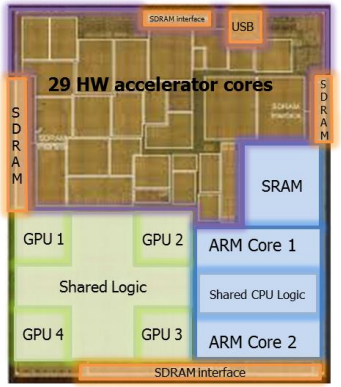
Sources: Prismark, Arstechnica, USPTO, Wikipedia, IPC, SMTA

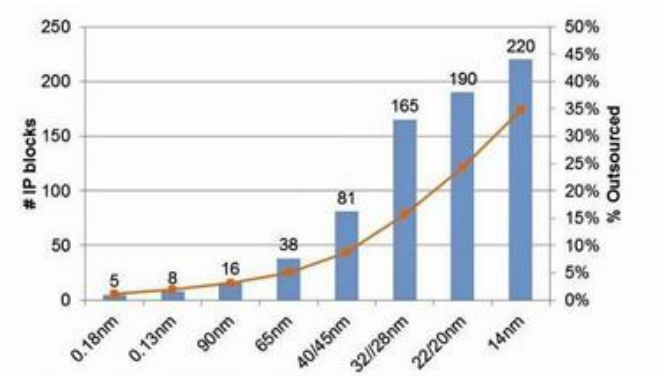
Modularity Already in Place at Monolithic Level

IP business model is based on chip modularity

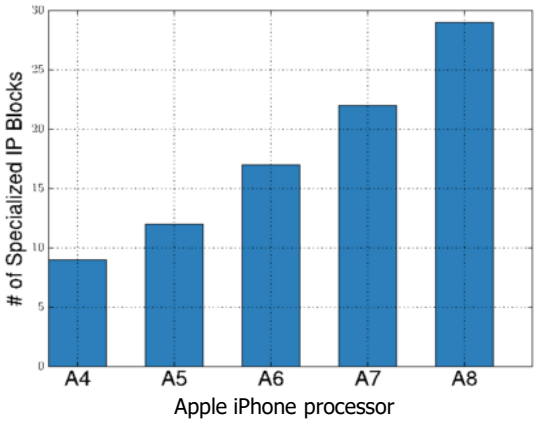


Apple A8





IP usage grows with node progress and design updates.

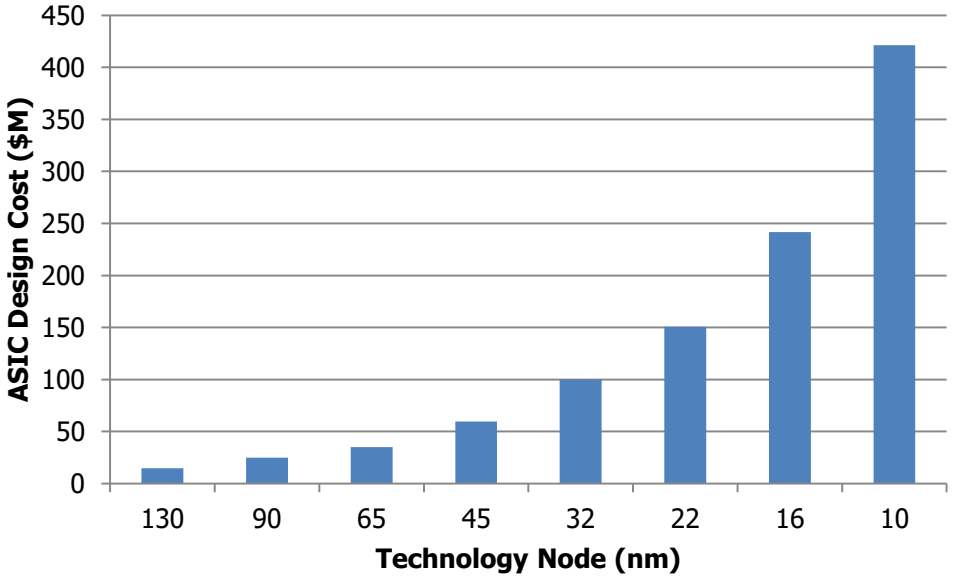


Modular semiconductor IP reduces chip design effort (time AND cost)

Sources: Cadence; ARM, Chipworks, Harvard

But Advanced Si is Still Expensive to Design and Fab

Expensive to design at advanced nodes …



… which some commercial products can support …

© apple.com

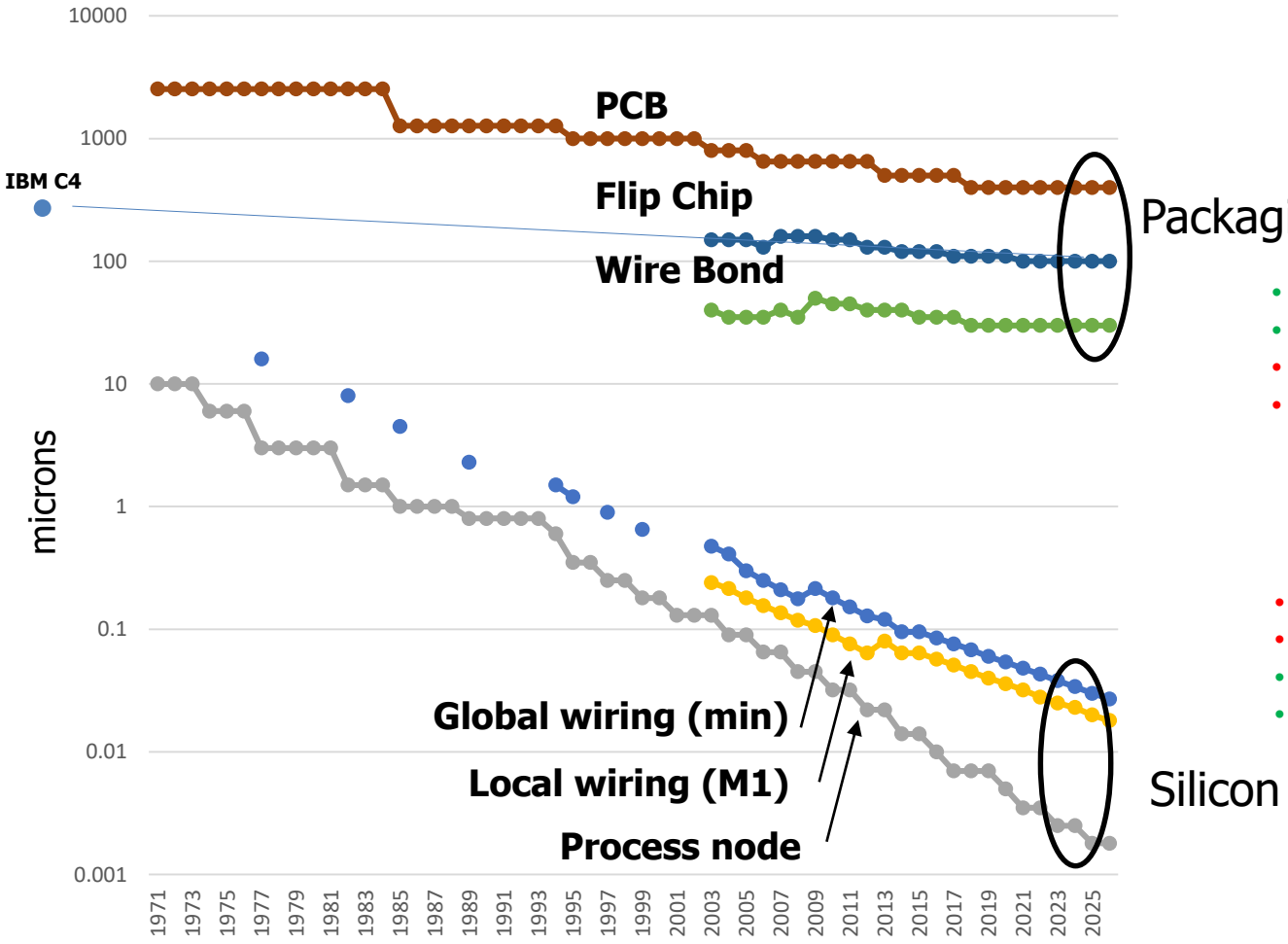
Fab cost for commercial electronics amortized over **one day's** worth of iPhones

… but DoD cannot.

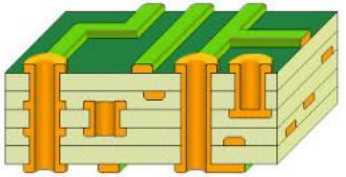
Fab cost for a DoD IC amortized over **entire 29 year** acquisition of JSF

Source: "Cashing in with Chips" AlixPartners Semiconductor R&D outlook report, 2014.

Conventional Assembly Has Attractive Features Too … But Isn't Keeping Up on Pitch and Performance



Packaging



- Flexible heterogeneous integration
- Quick design / manufacturing turns
- Coarse pitch
- Lower performance

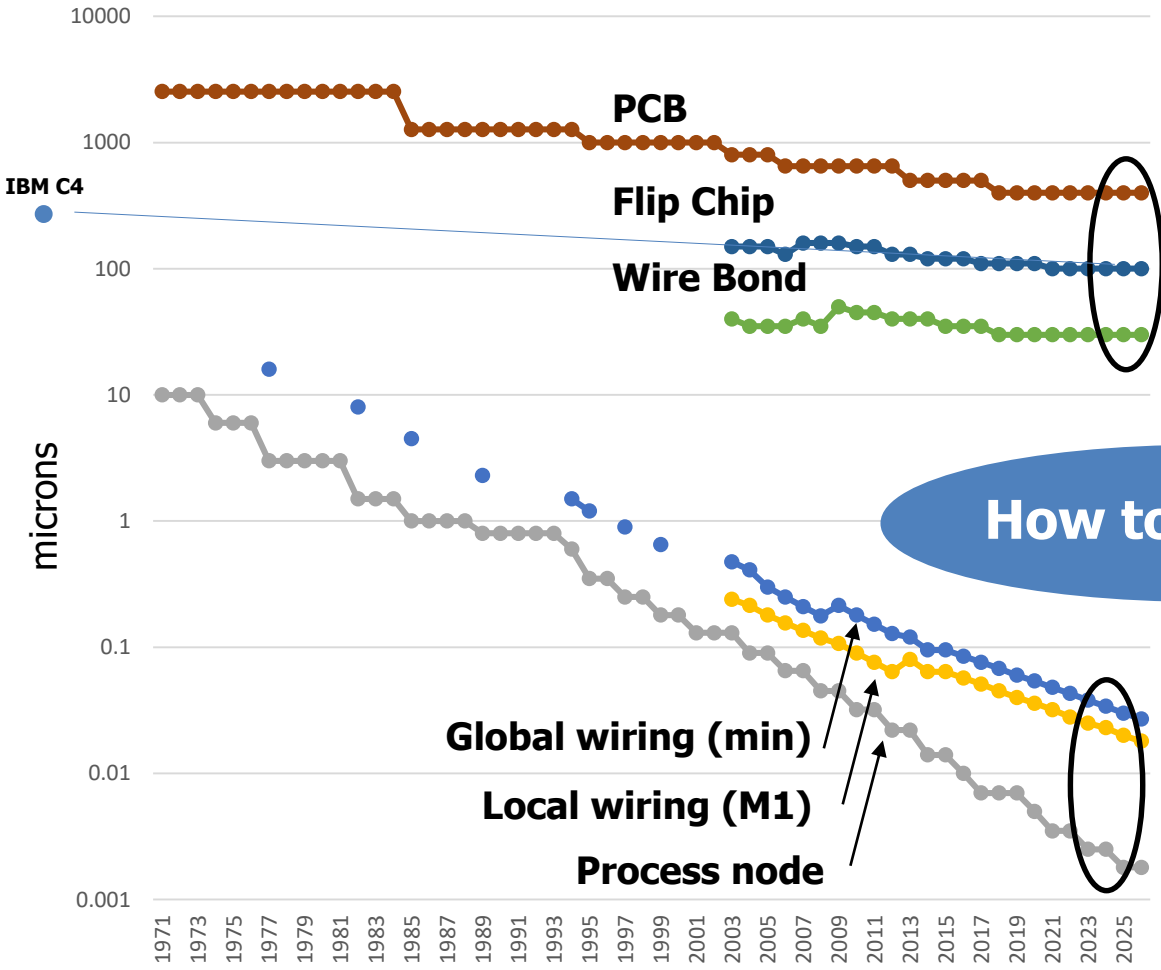
- Monolithic process
- Long design / manufacturing turns
- Fine pitch
- Higher performance

Silicon

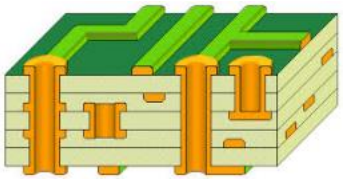
Need to combine speed and flexibility of packaging with pitch and performance of advanced heterogeneous device technology.

Source: 2003-13 ITRS, Wikipedia

Conventional Assembly Has Attractive Features Too … But Isn't Keeping Up on Pitch and Performance



Packaging



- Flexible heterogeneous integration
- Quick design / manufacturing turns
- Coarse pitch
- Lower performance

How to get both?

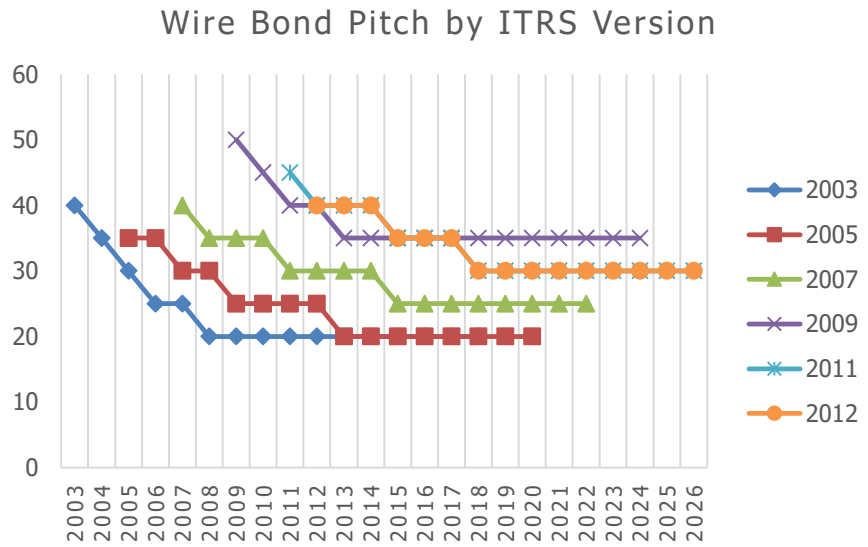
- Monolithic process
- Long design / manufacturing turns
- Fine pitch
- Higher performance

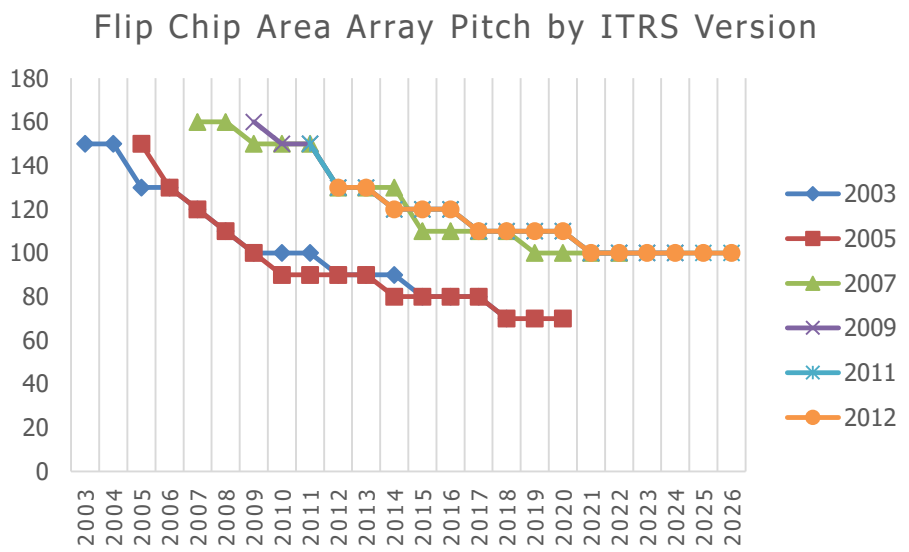
Silicon

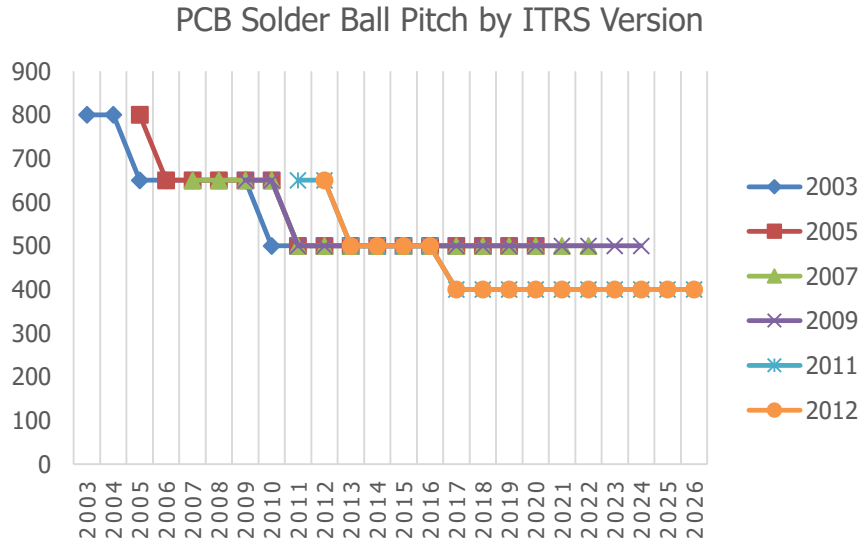
Need to combine speed and flexibility of packaging with pitch and performance of advanced heterogeneous device technology.

Source: 2003-13 ITRS, Wikipedia

Interconnect Pitch Progress Has Lagged Projections







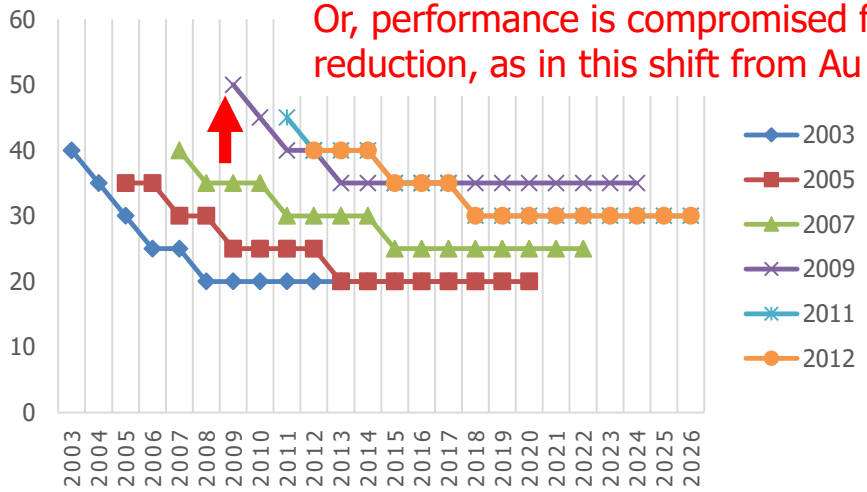
Notes:
1. Dimensions in microns.
2. Wire bonding:
   a. Discontinuity in 2009 due to shift to Cu as mainstream wire material.
   b. Data is for "single in-line." Multi-tier first appeared in 2005 roadmap.
3. Flip chip:
   a. Discontinuities due to shifting ITRS product/application categories.
   b. Data is for "GPU/CPU/Chipset" in 2007, "high-performance" in 2009, and "cost-performance" in 2011-12.
4. PCB:
   a. Data is for "cost-performance" category.
   b. Data is for "conventional system board" application starting in 2007.

Can address the growing interconnect gap with standardized, fine pitch interconnects.

Source: 2003-13 ITRS

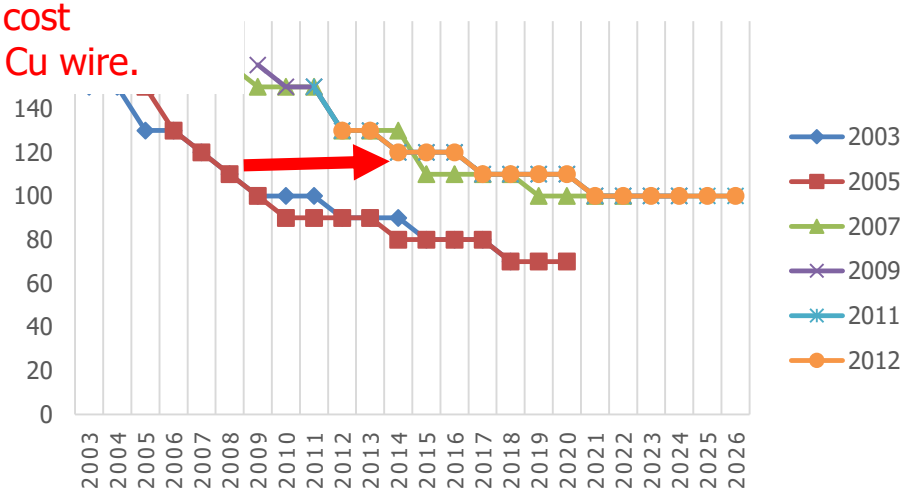
Interconnect Pitch Progress Has Lagged Projections

Wire Bond Pitch by ITRS Version

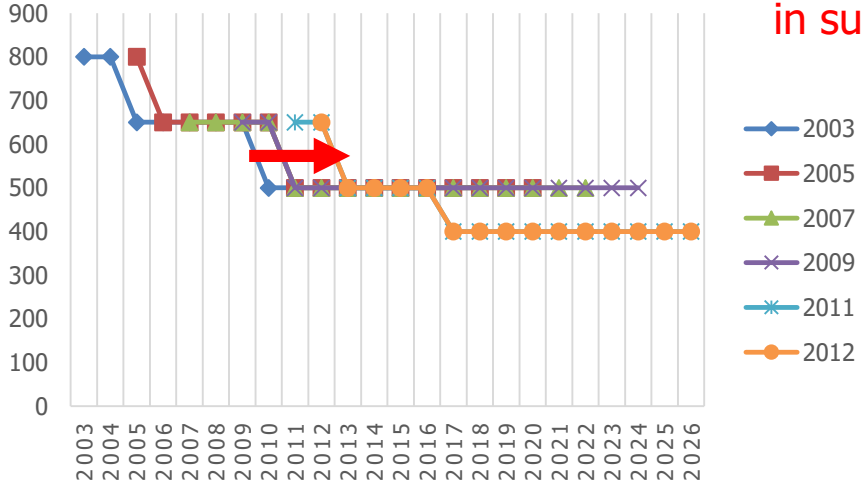


Or, performance is compromised for cost reduction, as in this shift from Au to Cu wire.

Flip Chip Area Array Pitch by ITRS Version



PCB Solder Ball Pitch by ITRS Version



Progress is typically pushed out in subsequent roadmap updates.

Notes:
1. Dimensions in microns.
2. Wire bonding:
   a. Discontinuity in 2009 due to shift to Cu as mainstream wire material.
   b. Data is for "single in-line." Multi-tier first appeared in 2005 roadmap.
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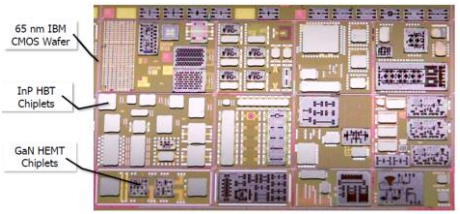
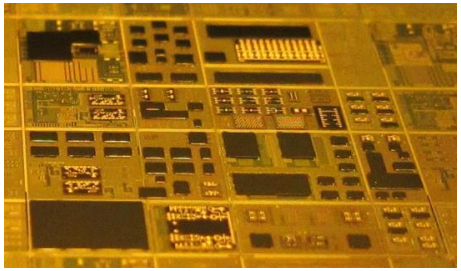
Can address the growing interconnect gap with standardized, fine pitch interconnects.

Source: 2003-13 ITRS

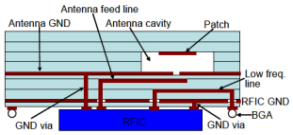
Heterogeneous Integration: Bridging the Gap



DAHI MPW0

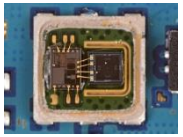


DAHI MPW1

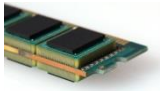


Advanced PCB

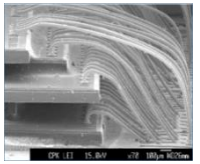
Package-based: Mature and flexible, but not scalable



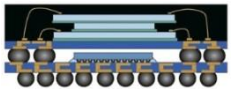
MEMS + ASIC



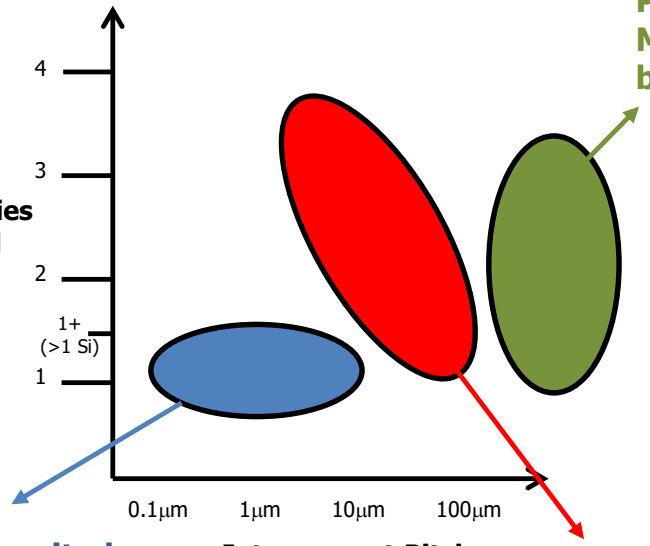
PoP memory

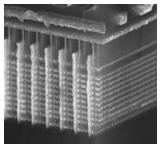


Stacked die (WB)

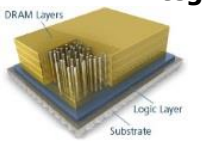


Processor + memory PoP

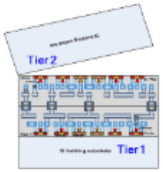




Monolithic 3D NAND

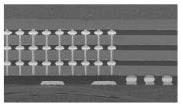


Processor + memory TSV



F2F wafer-bond

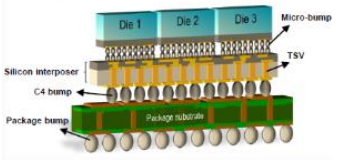
TSV / Wafer-scale: Immature or not well-suited for Heterogeneous Integration



NAND/DRAM TSV

Image sensor TSV

Interposer-based: Scalable and flexible

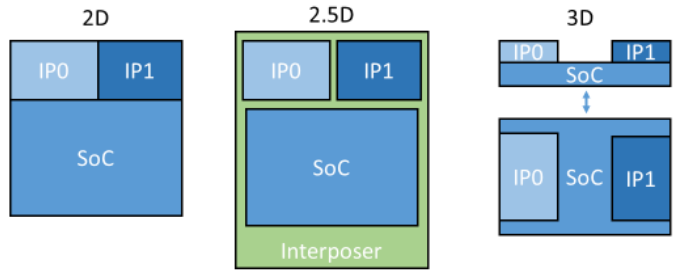


2.5D Si interposer

DAHI creates integration capabilities beyond current advanced interconnect technologies.

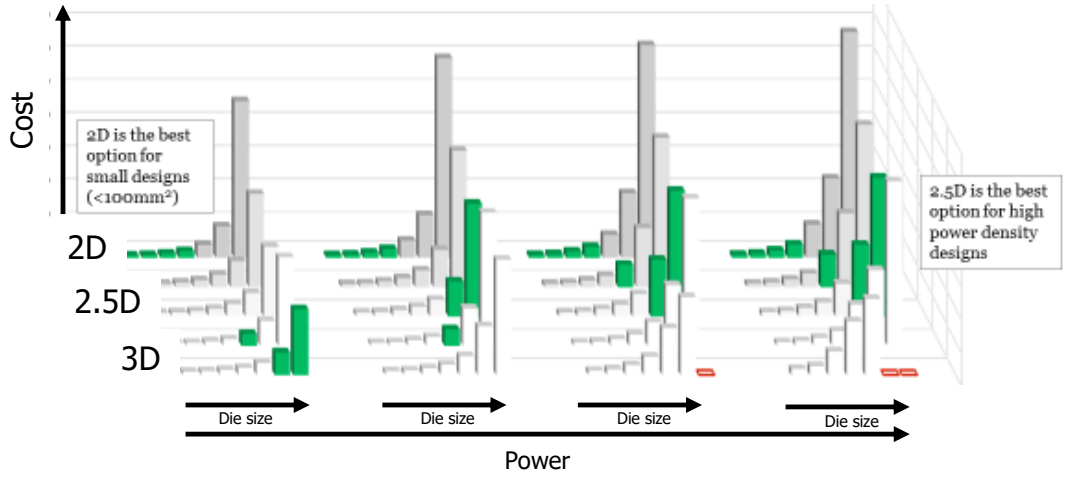
Complicated Trade Space in Choosing Integration Approach

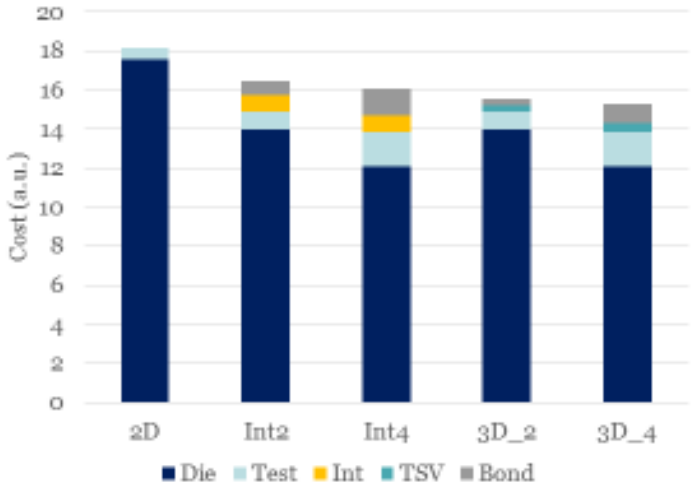
Case Study Scenario



Many factors affect optimal integration approach:

- size of IP blocks
- % IP reuse
- licensing cost
- die size
- process yield / maturity
- relative cost of nodes
- power / cooling options
- gate count





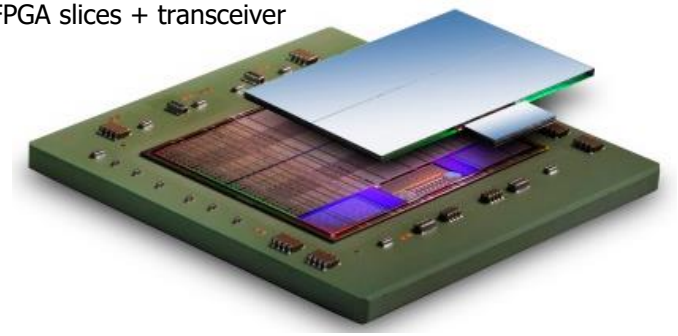
The die cost dominates, independent of integration approach, so chip cost reduction via IP reuse is beneficial in all scenarios.

2.5D is typically the best option for high power, high complexity designs.

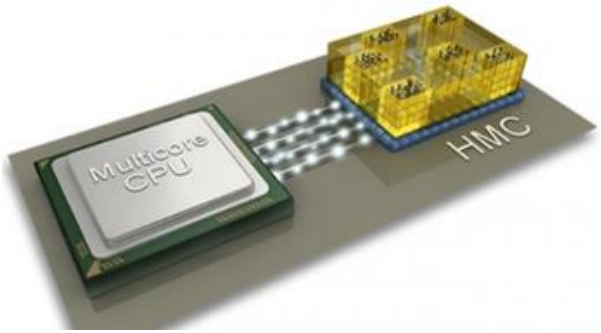
Source: UCSB

Modularity Addresses Digital Challenges at Leading Edge

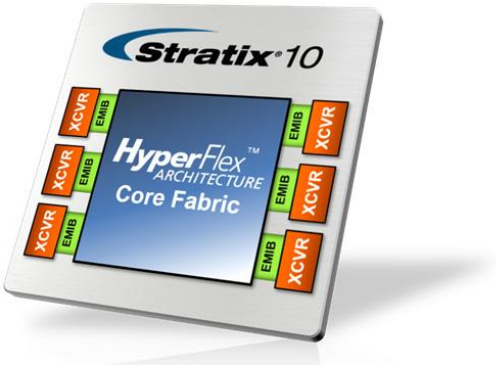
Xilinx Virtex-7 H580T
2 FPGA slices + transceiver



Increases Yield



Links High Bandwidth Memory to Processor



Enables IP Reuse

But everything is a point solution!

Sources: EETimes / Xilinx, Extremetech / HMC, Altera/Intel

What is CHIPS?

CHIPS will develop design tools, integration standards, and IP blocks required to demonstrate modular electronic systems that can leverage the best of DoD and commercial designs and technology.

Today – Monolithic

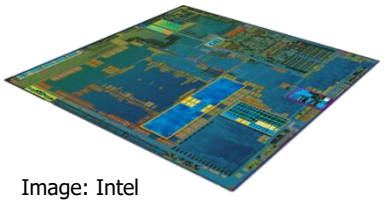
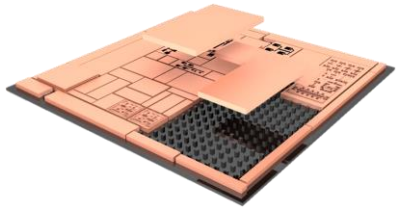
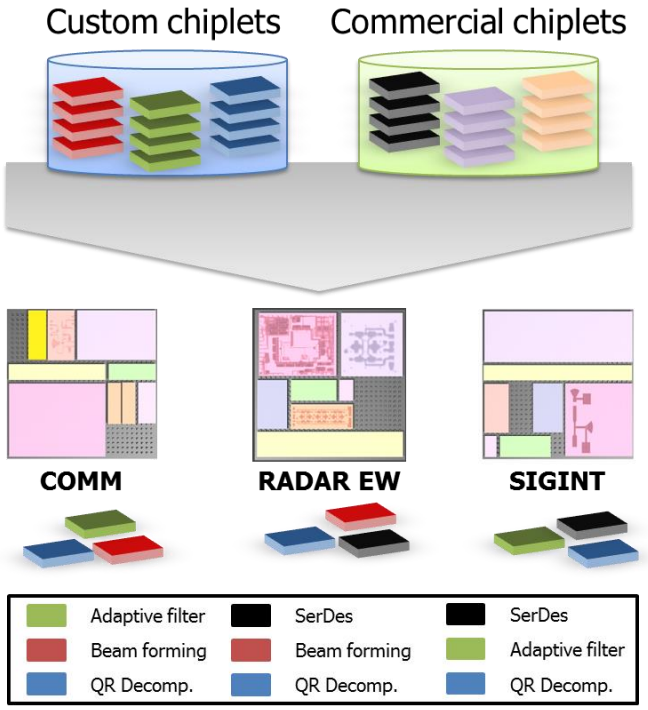


Image: Intel

Tomorrow – Modular

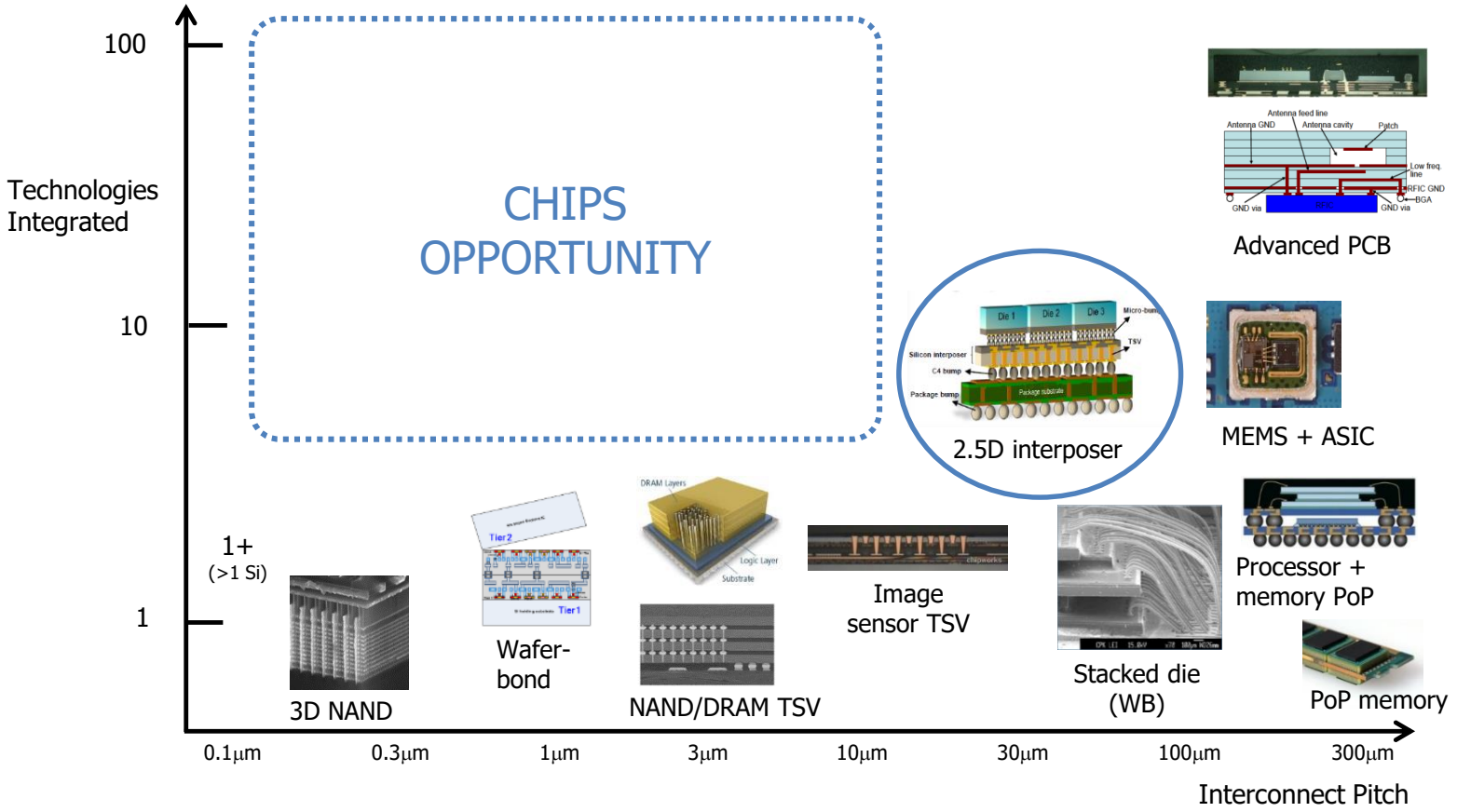


CHIPS enables rapid integration of functional blocks at the chiplet level



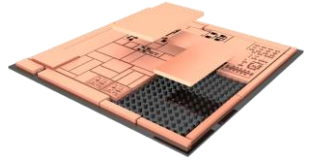
Source: DARPA

Integration diversity vs. density

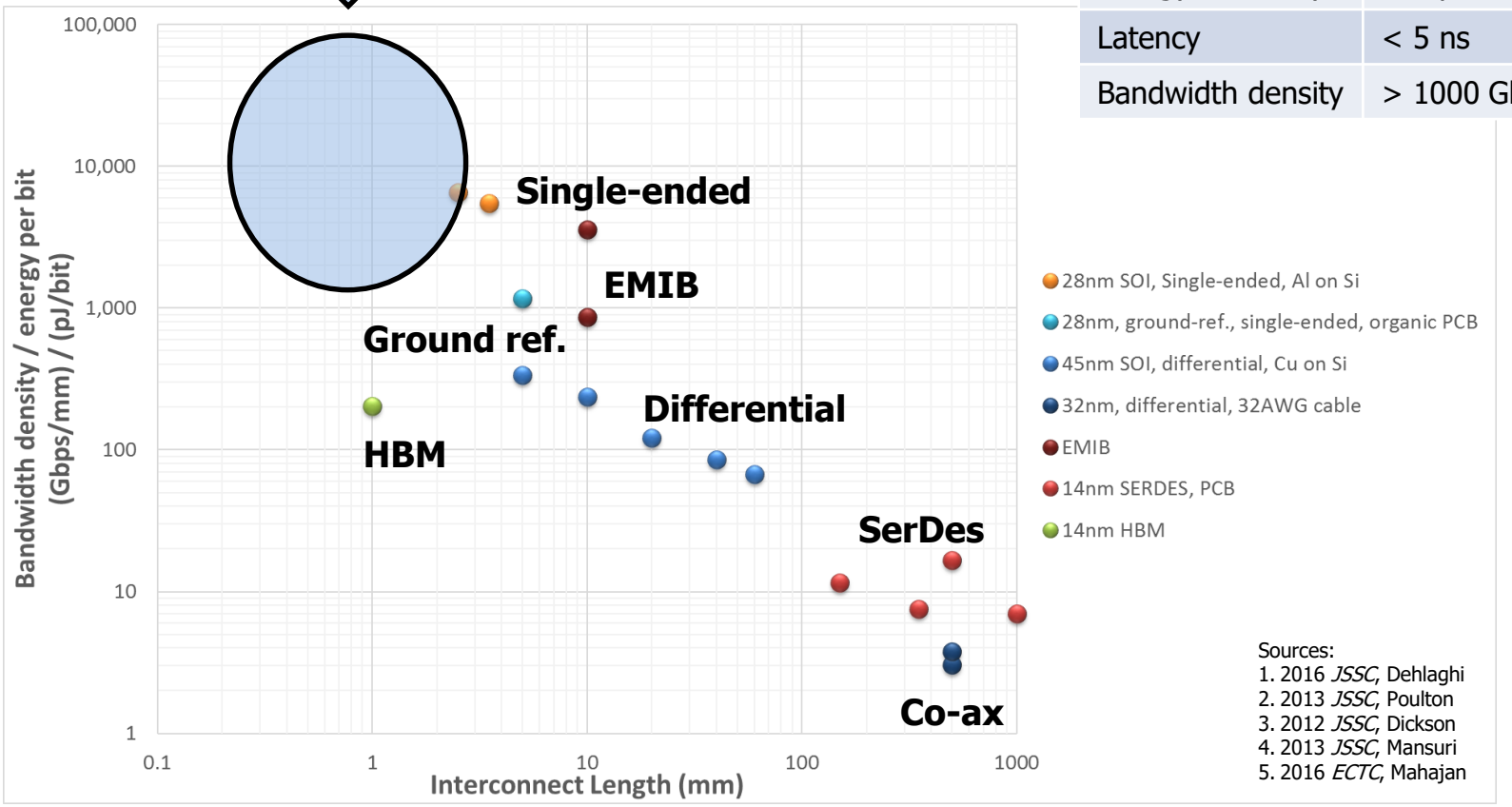


Sources: Samsung, Tezzaron, Micron, Hynix, Sony, TSMC, Prismark, STATS ChipPAC, Georgia Tech, IEEE, STMicro, Finetech

CHIPS developing interface standard



CHIPS Target

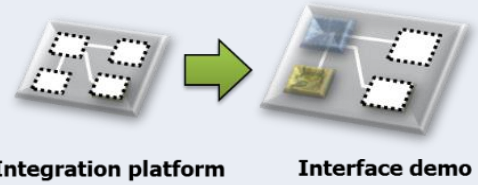
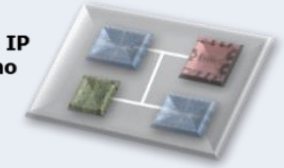
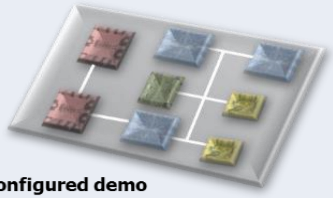


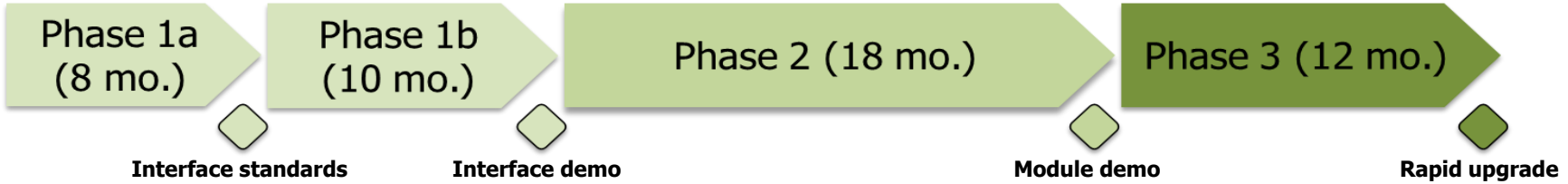
CHIPS Program Interface Standard Metrics	
Data rate	10 Gpbs
Energy efficiency	< 1 pJ/bit
Latency	< 5 ns
Bandwidth density	> 1000 Gbps/mm

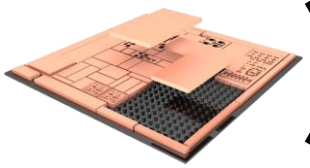
Sources:
1. 2016 *JSSC*, Dehlaghi
2. 2013 *JSSC*, Poulton
3. 2012 *JSSC*, Dickson
4. 2013 *JSSC*, Mansuri
5. 2016 *ECTC*, Mahajan

CHIPS interface is one of many possible routes for efficient interdie communications

CHIPS program: structure and timing

PHASE 1	PHASE 2	PHASE 3
Interface and IP Block Demo	**Module Demo with IP Blocks**	**Rapid Module Upgrade**
 Integration platform Interface demo	Full system IP reuse demo 	 Reconfigured demo



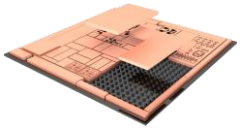


TA1	Modular Digital Systems
TA3	Supporting Technologies
TA2	Modular Analog Systems

Seeking CHIPS collaboration to help drive a common interface

Source: DARPA

CHIPS: August 2017 Kickoff



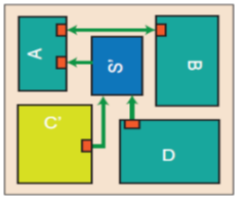
CHIPS Team

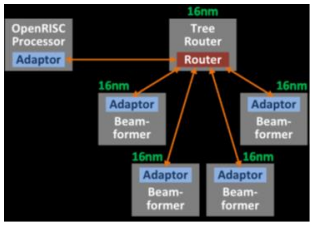
Designs
- Boeing
- Intel
- Lockheed Martin
- Northrop Grumman
- Univ. of Michigan

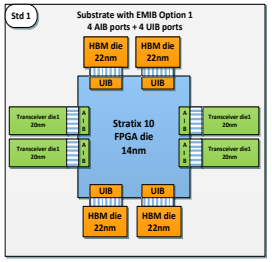
Chiplets
- Intrinsix
- Jariet
- Micron
- North Carolina State
- Synopsys

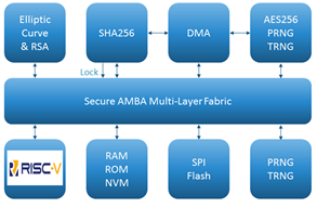
Tools
- Cadence
- Georgia Tech

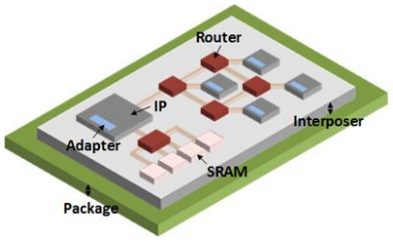
CHIPS Approach
Modularity
Standards











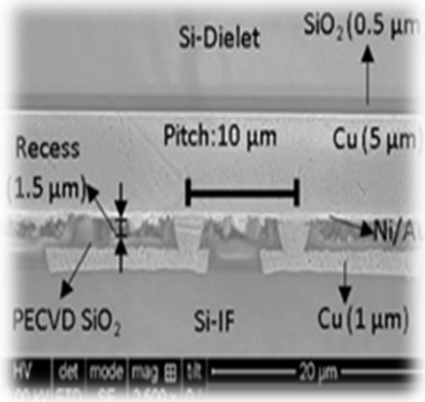
CHIPS Results
Fast
Cost-Effective
Best-in-Class

5G

Images sources:
Lockheed Martin, Boeing, Intel, Intrinsix, Univ. of Michigan, 3GPP.org

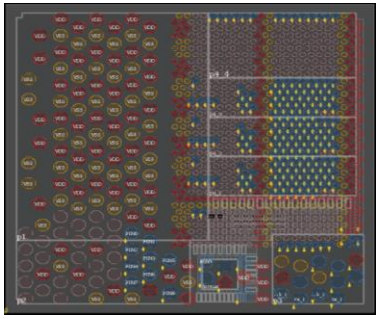
CHIPS Performer Summary

Manufacturing



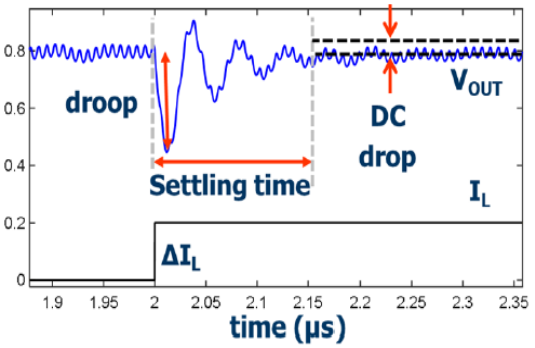
Intel
Northrop Grumman
Micross
UCLA

Chiplets



Jariet
Synopsys
Micron
Intrinsix
Lockheed Martin
Michigan
NCSU
Ferric

Tools

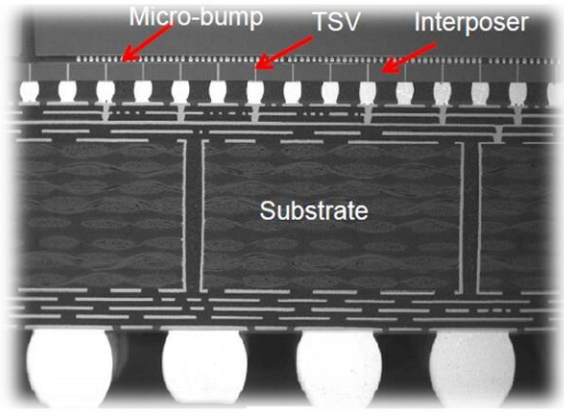


Cadence
Georgia Tech

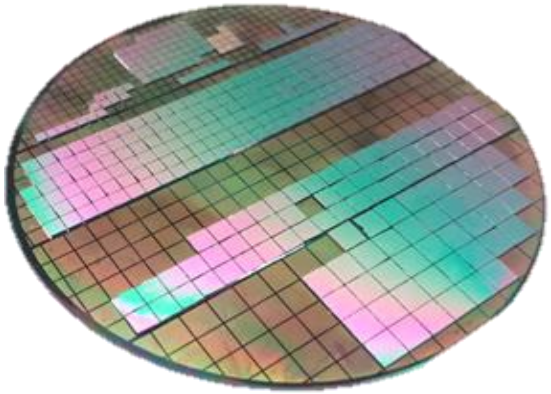
Sources: UCLA, Michigan, Georgia Tech

Current Focus of CHIPS:
Interface Standard and Manufacturing

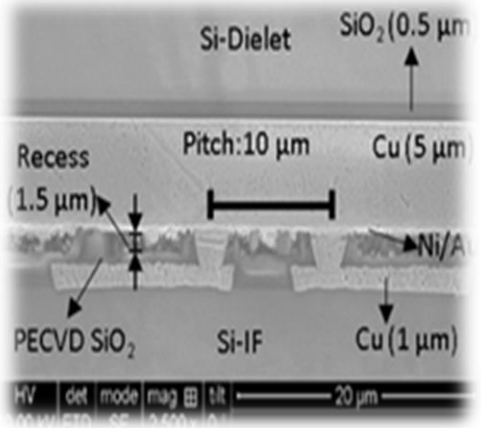
CHIPS Manufacturing Research Vectors



Low Cost
Interposers



Micron Scale
Chiplet Placement



10-55um
Bump & Bond

CHIPS is targeting solutions suitable for low volume (<100K units) trusted manufacturing needed for national security requirements.

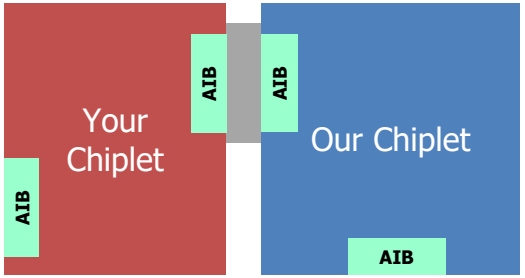
Sources: Xilinx, UCLA

CHIPS Interface Standard Based on Intel's AIB

- **AIB (Advanced Interface Bus)** is a PHY-level interface standard for **high bandwidth, low power** die-to-die communication
  - AIB is a clock-forwarded parallel data transfer like DDR DRAM
  - High density with 2.5D interposer (e.g., CoWoS, EMIB) for multi-chip packaging
  - AIB is PHY level (OSI Layer 1)
  - Can build protocols like AXI-4 or PCI Express on top of AIB

- **AIB Promoters** agreed to promote AIB as a die-to-die interface standard

- Public information available from Intel at: https://intel.ly/2LISZcr



ADC/DAC
Machine Learning
Memory
Processors
Adjacent IP
Etc. …

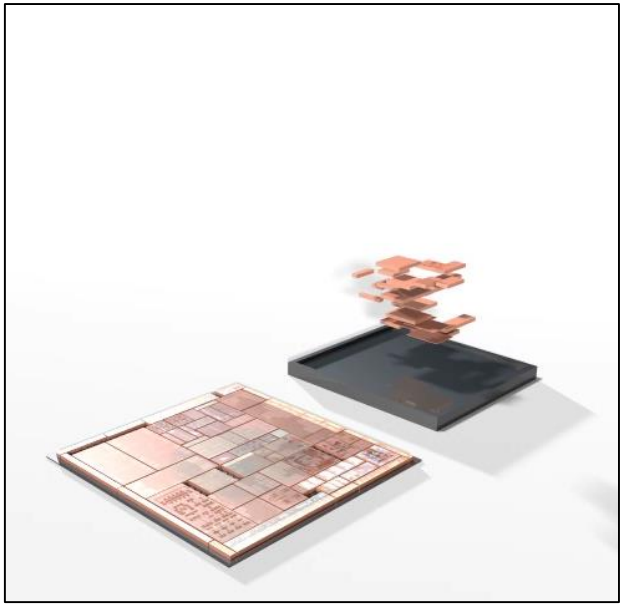
AIB Promoters:

-Boeing
-Intrinsix
-Synopsys
-Intel
-Lockheed Martin
-Sandia
-Jariet
-NCSU
-U. of Michigan

Source: Intel

The CHIPS Vision: Ethernet for Chips

- **Modularity**: A ubiquitous chiplet interface standard "Ethernet for chiplets"
- **Speed**: Board manufacturing time scales (days) possible with a library of hundreds of COTS chiplets
- **Performance**: 1pJ/bit and 1Tbit/mm WILL disrupt the computing landscape
- **Security**: CHIPS disaggregation offers a pathway to high assurance electronics



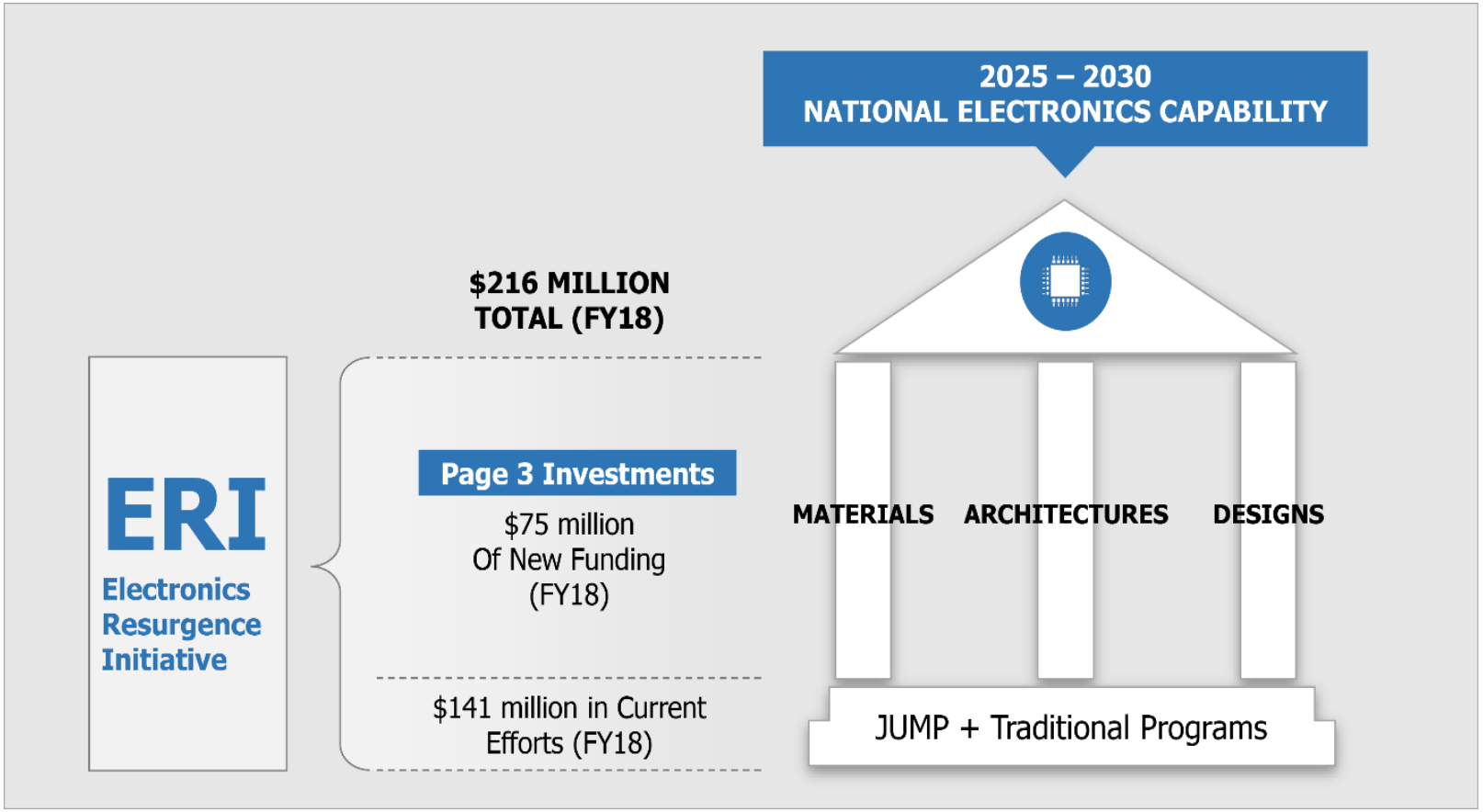
DARPA MTO Electronics Resurgence Initiative

Most presentations from the July 2018 and July 2019 ERI Summits are available as links from the agenda pages:

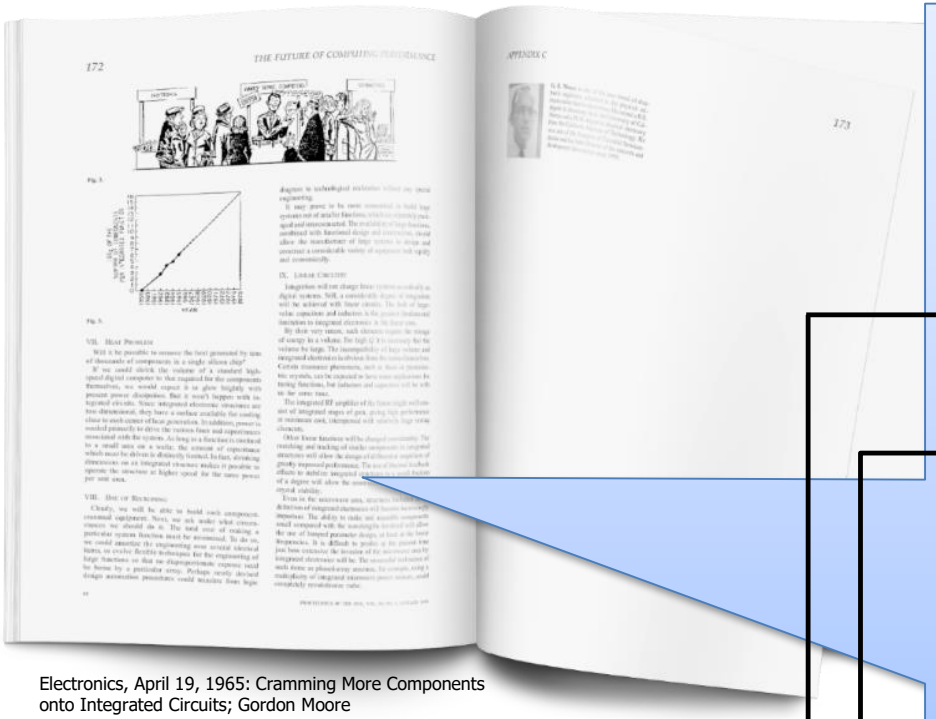
http://www.eri-summit.com

Electronics Resurgence Initiative

- ERI—creating an electronics capability that will provide a foundational contribution to national security
- Three thrust areas: Materials and Integration, Architectures, Designs



New investment based on "Page 3"



Electronics, April 19, 1965: Cramming More Components onto Integrated Circuits; Gordon Moore

P.3

VIII. DAY OF RECKONING

Clearly, we will be able to build such component-crammed equipment. Next, we ask under what circumstances we should do it. **The total cost of making a particular system function must be minimized.** To do so, we could amortize the engineering over several identical items, or **evolve flexible te** **functions** so that no disproportionate expense need be borne by a particular array. Perhaps newly devised design automation proced y special engineering.

It may prove to be more economical to build large systems out of smaller functions, which are separately packaged, combined with functional design and construction, should allow the manufacturer of large systems to design and construct a considerable variety of equipment both rapidly and economically.

evolve flexible techniques for the engineering of large functions

newly devised design automation procedures could translate from logic diagram to technological realization

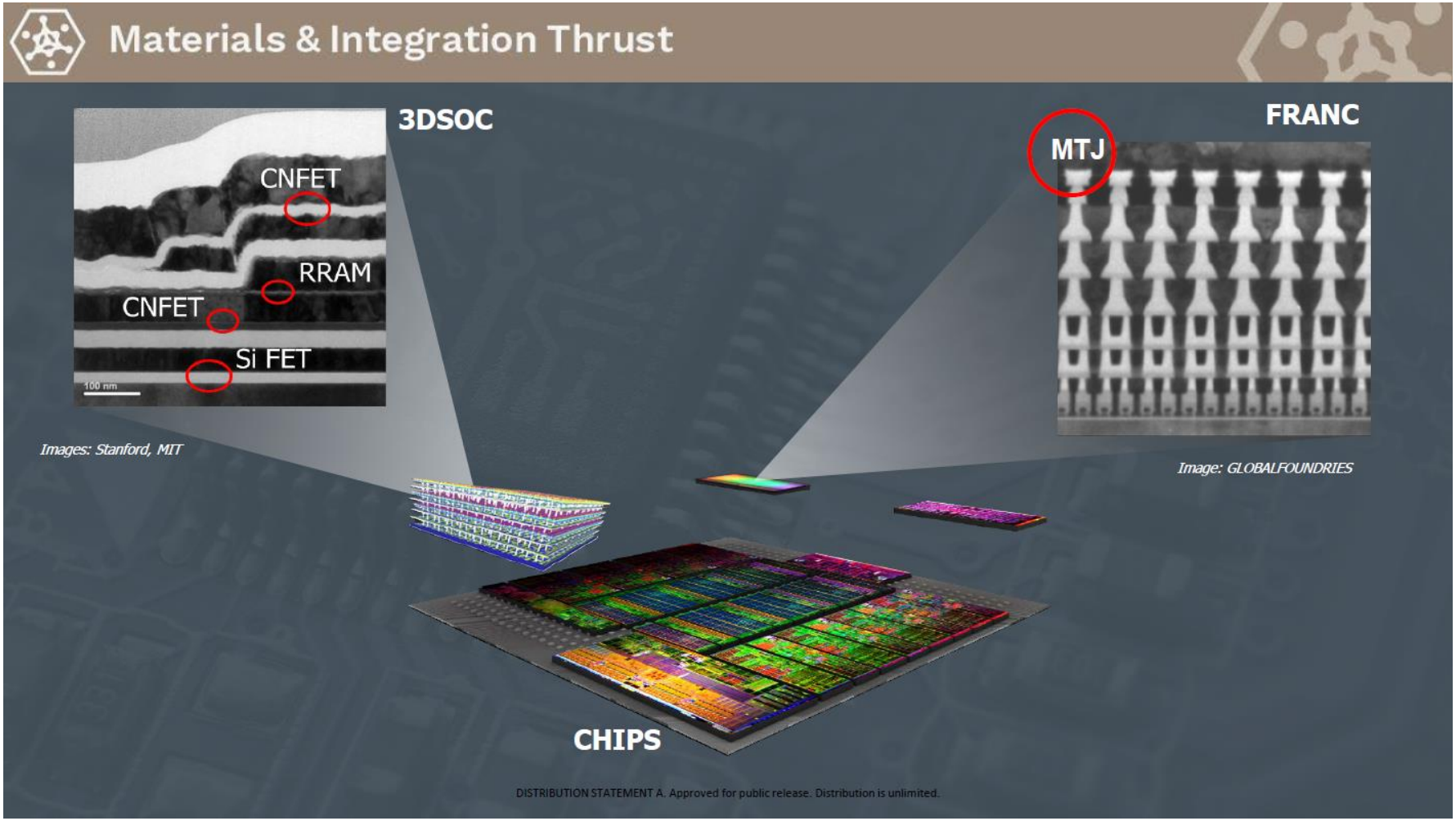
more economical to build large systems out of smaller functions, which are separately packaged

Architecture
Maximizing specialized functions

Design
Quickly enabling specialization

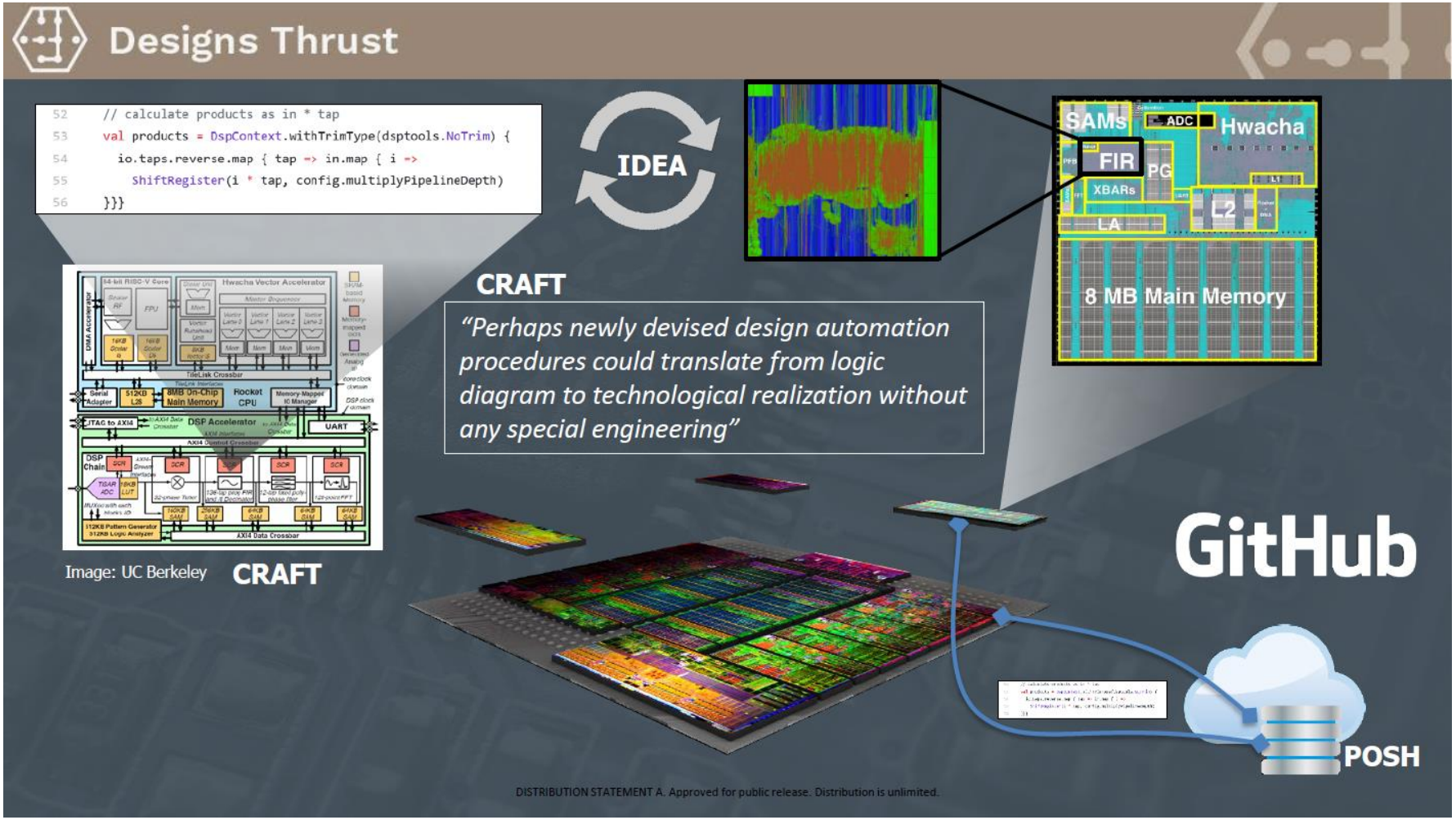
Materials & Integration
Adding separately packaged novel materials and using integration to provide specialized computing

ERI Materials and Integration



Bill Chappell, DARPA ERI Summit, July 2018

ERI Designs



Bill Chappell, DARPA ERI Summit, July 2018

ERI Architectures

Architectures Thrust

HIVE

DSSoC

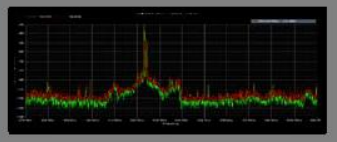
SDH

Image: Drexel Univ.

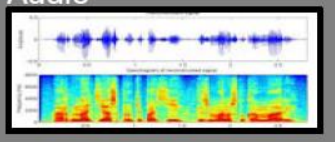
Array of sensors

LiDAR

RF

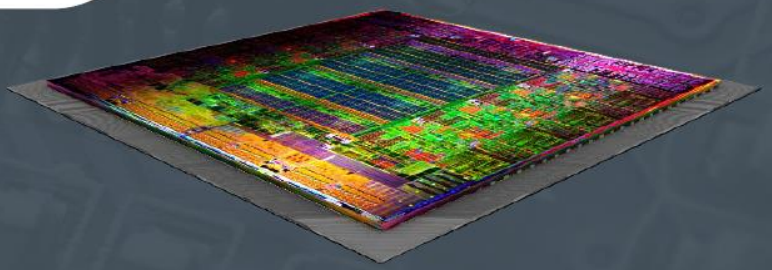


Audio



HIVE

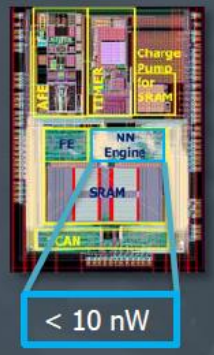
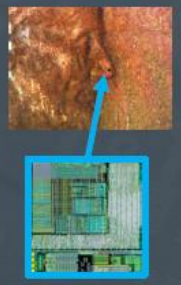
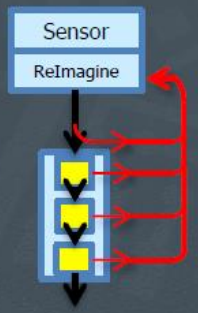
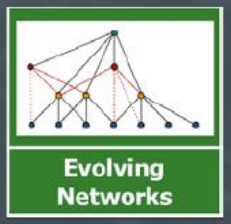
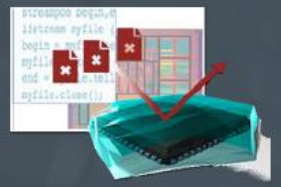
"...amortize the engineering over several identical items, or evolve flexible techniques for the engineering of large functions..."

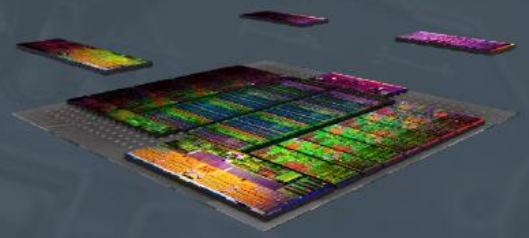


Bill Chappell, DARPA ERI Summit, July 2018

ERI Applications

Driving Applications

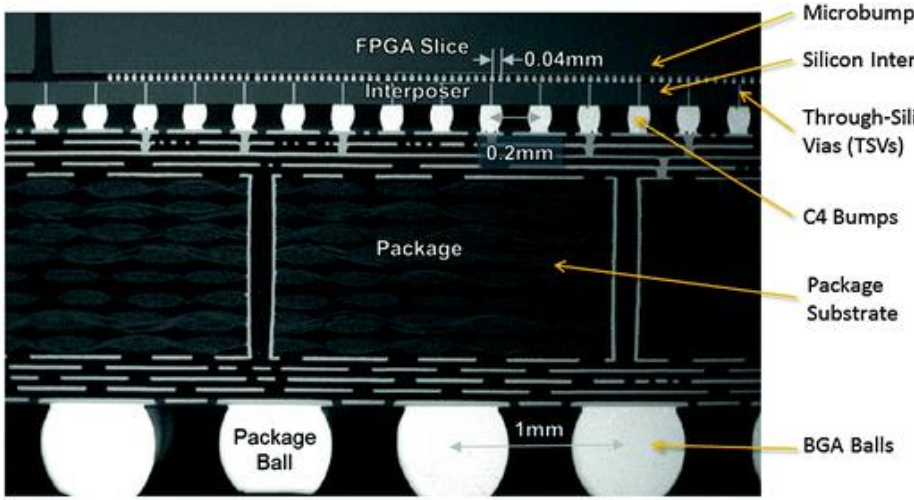
N-ZERO	SHIELD	ReImagine	L2M	SC2	SSITH
					
< 10 nW	< 100 um²				
No Power Operation	Art of the Small	Saliency	In Field Learning	Learning Cooperation through Edge Intelligence	Hardware as the Foundation of Security



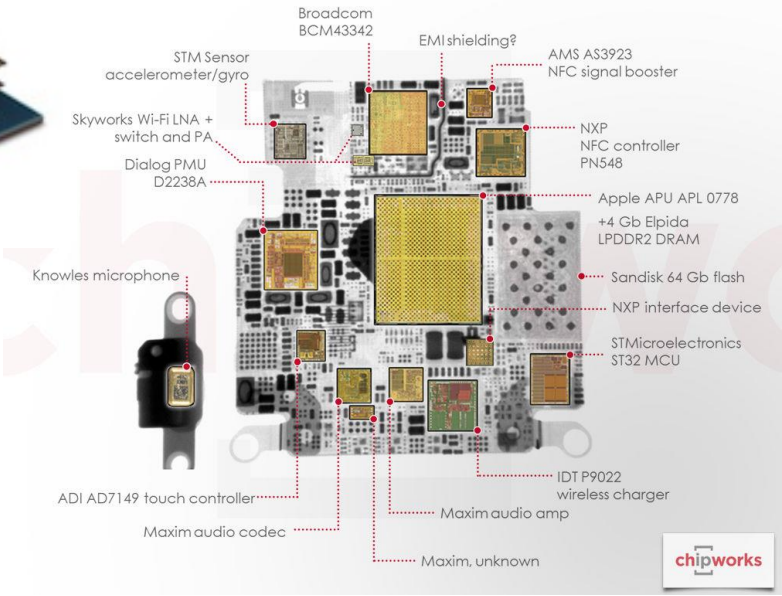
Bill Chappell, DARPA ERI Summit, July 2018

Future

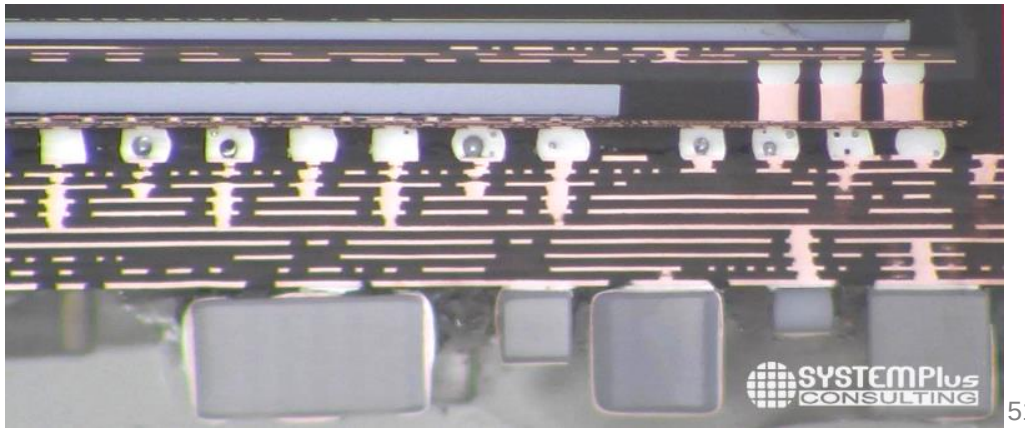
Semiconductor Packaging Landscape:
Examples of leading edge capabilities available at commercial scales



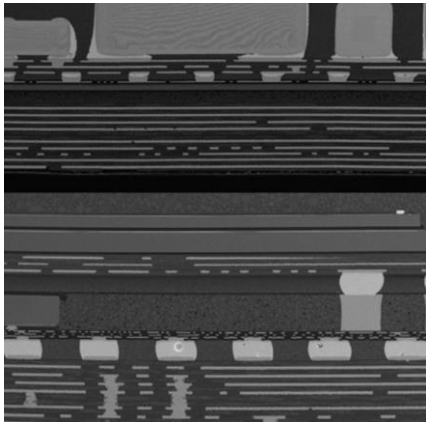
Amkor / Ibiden / TSMC Silicon interposers and through silicon vias (TSVs) for Xilinx FPGA



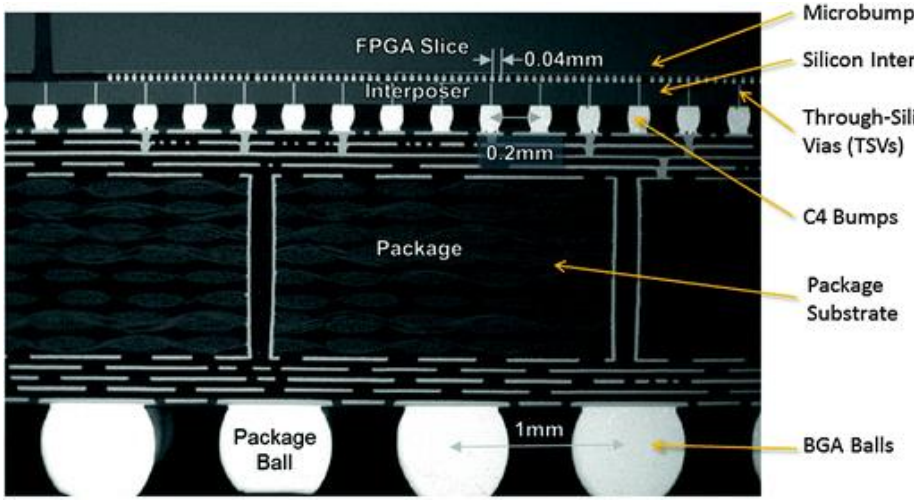
TSMC Integrated fan-out (InFO) packaging of A10 processor in iPhone7



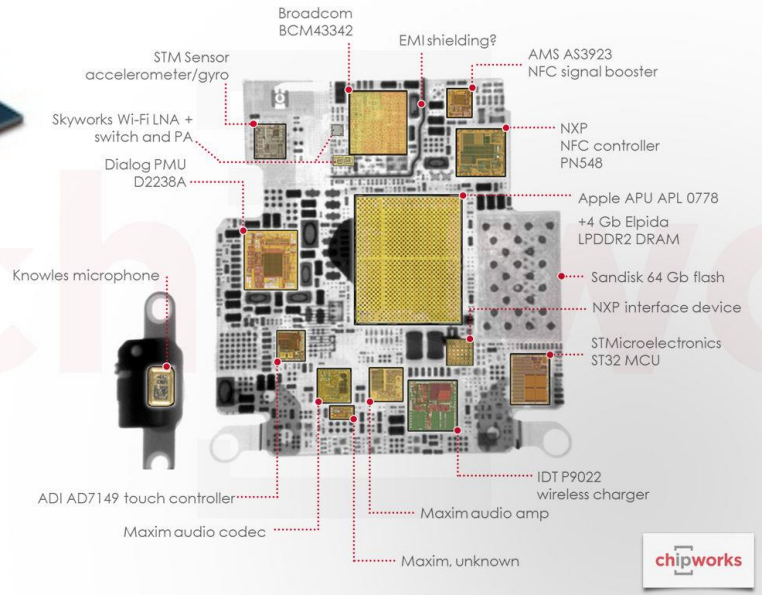
ASE System-in-Package in Apple Watch



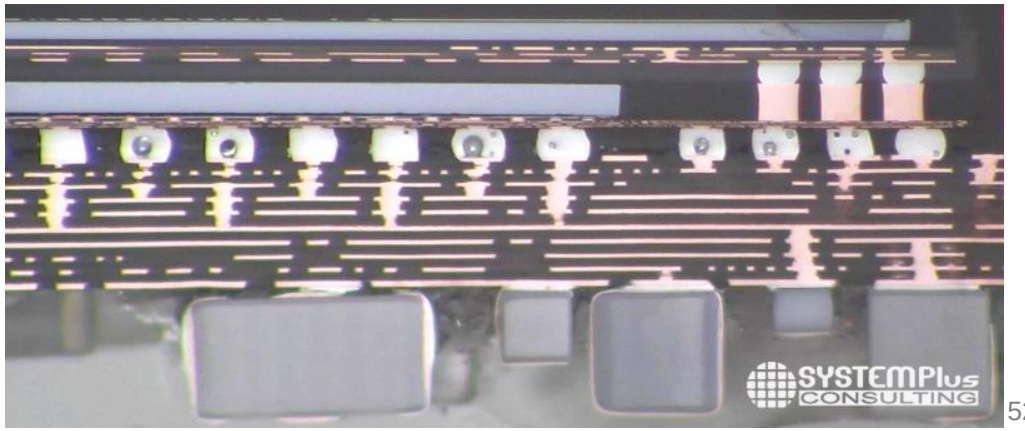
Semiconductor Packaging Landscape:
Examples of leading edge capabilities not available to the DoD



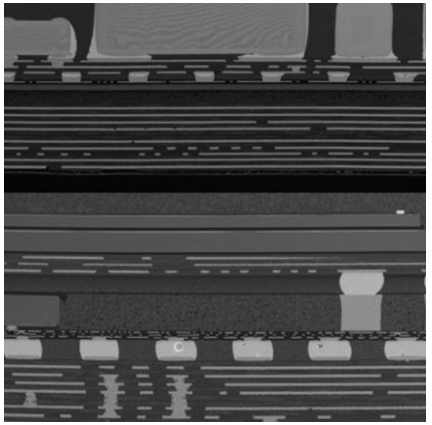
Amkor / Ibiden / TSMC Silicon interposers and through silicon vias (TSVs) for Xilinx FPGA



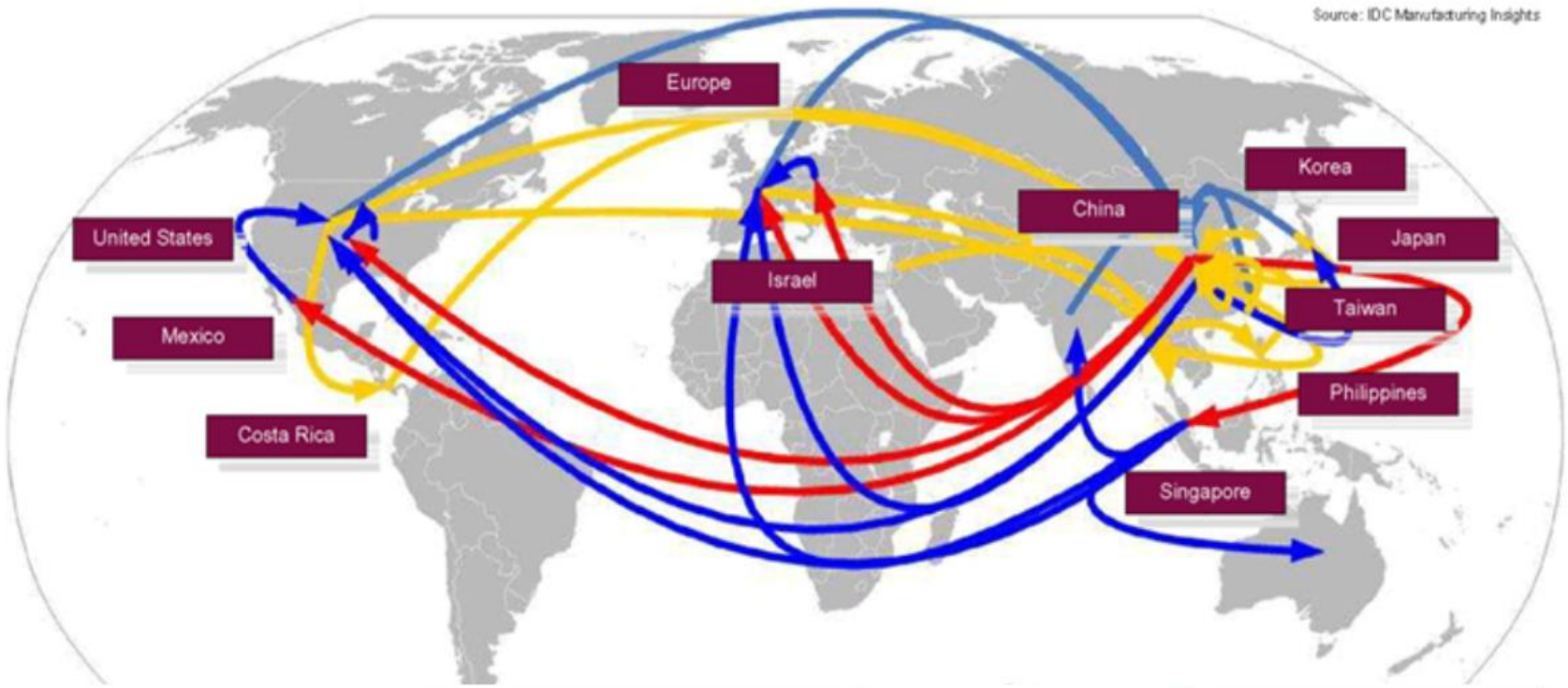
TSMC Integrated fan-out (InFO) packaging of A10 processor in iPhone7



ASE System-in-Package in Apple Watch



Electronic Manufacturing Supply Chain: Unavoidably international, even for DoD



Source: IDC Manufacturing Insights & Booz Allen analysis

Lifecycle for a single Joint Strike Fighter component, which changes hands 15 times before final installation

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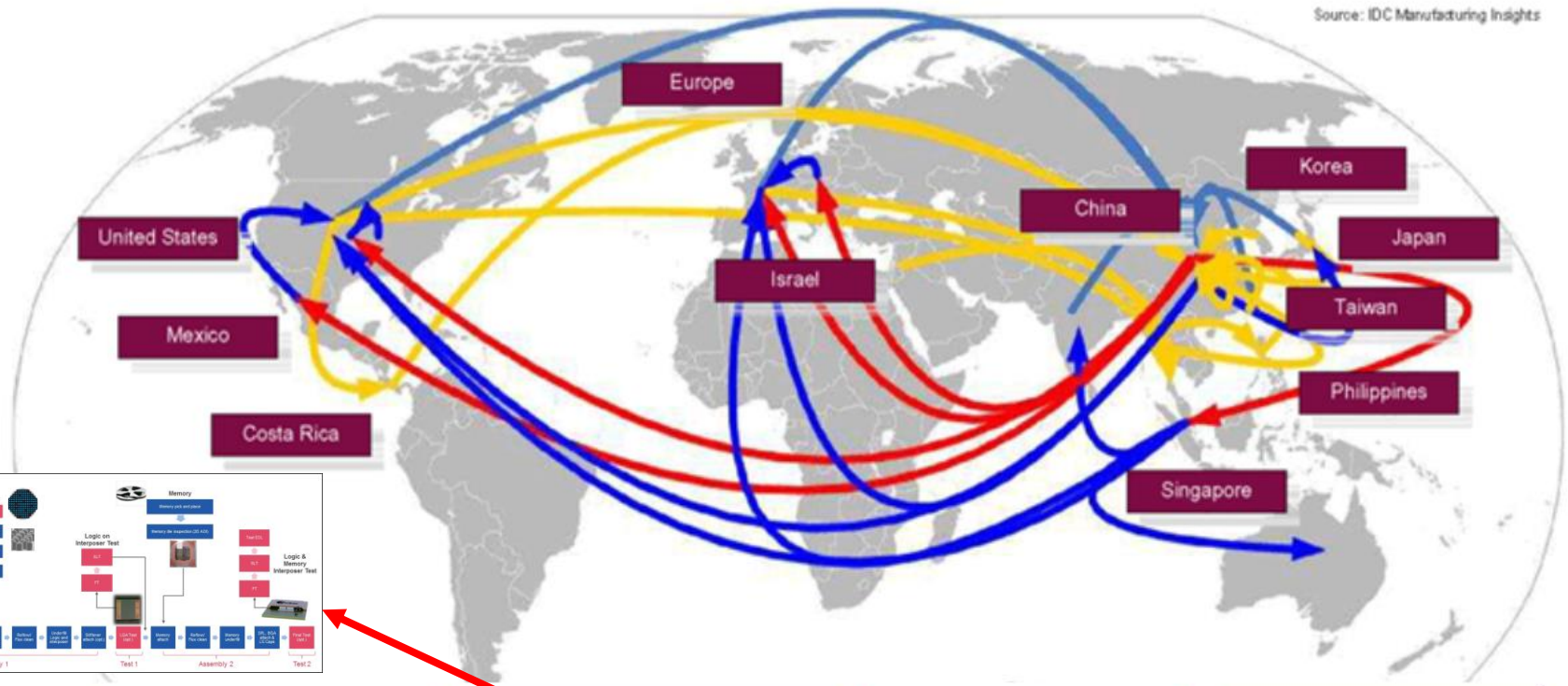
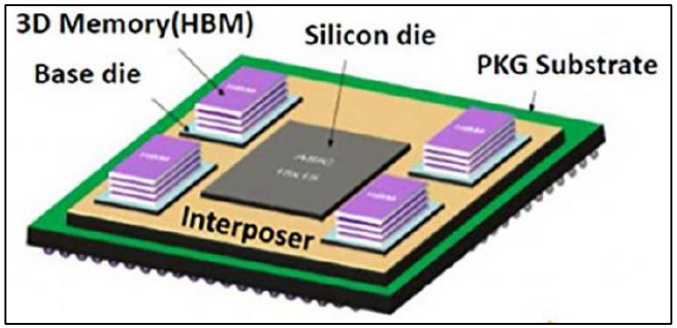


Semiconductor Design | Semiconductor Manufacturing & Packaging | Printed Circuit Board Production | Printed Circuit Board Distribution

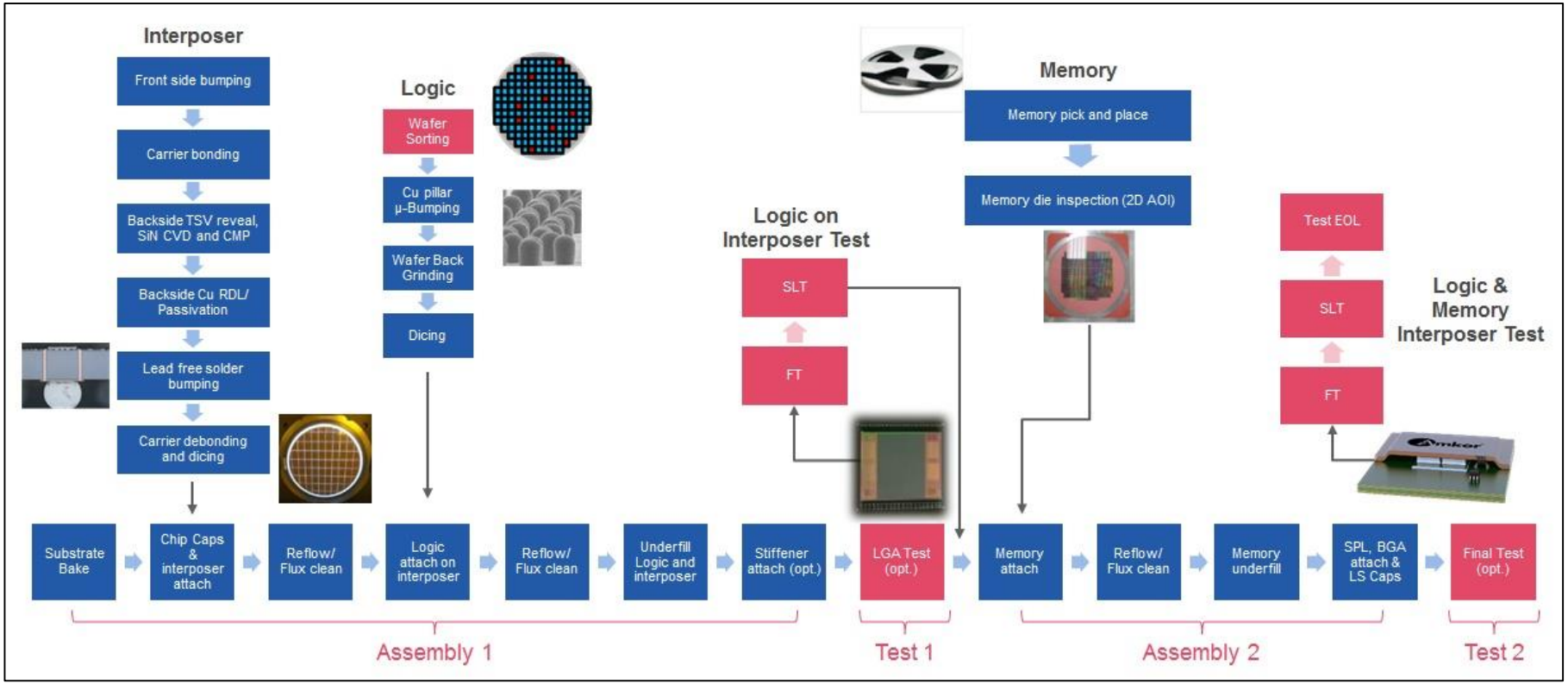
Source: IDC Manufacturing Insights & Booz Allen analysis

Lifecycle for a single Joint Strike Fighter component, which changes hands 15 times before final installation

Semiconductor Assembly Example (2.5D HBM)



How many people have access throughout the supply chain?



Source: "Start Your HBM/2.5D Design Today," SK Hynix, Amkor, eSilicon, Northwest Logic, Avery Design, 2016.

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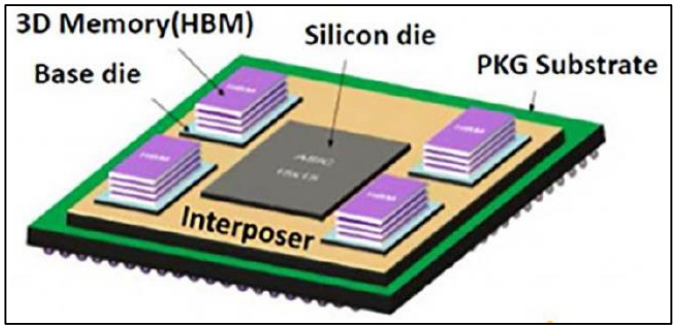
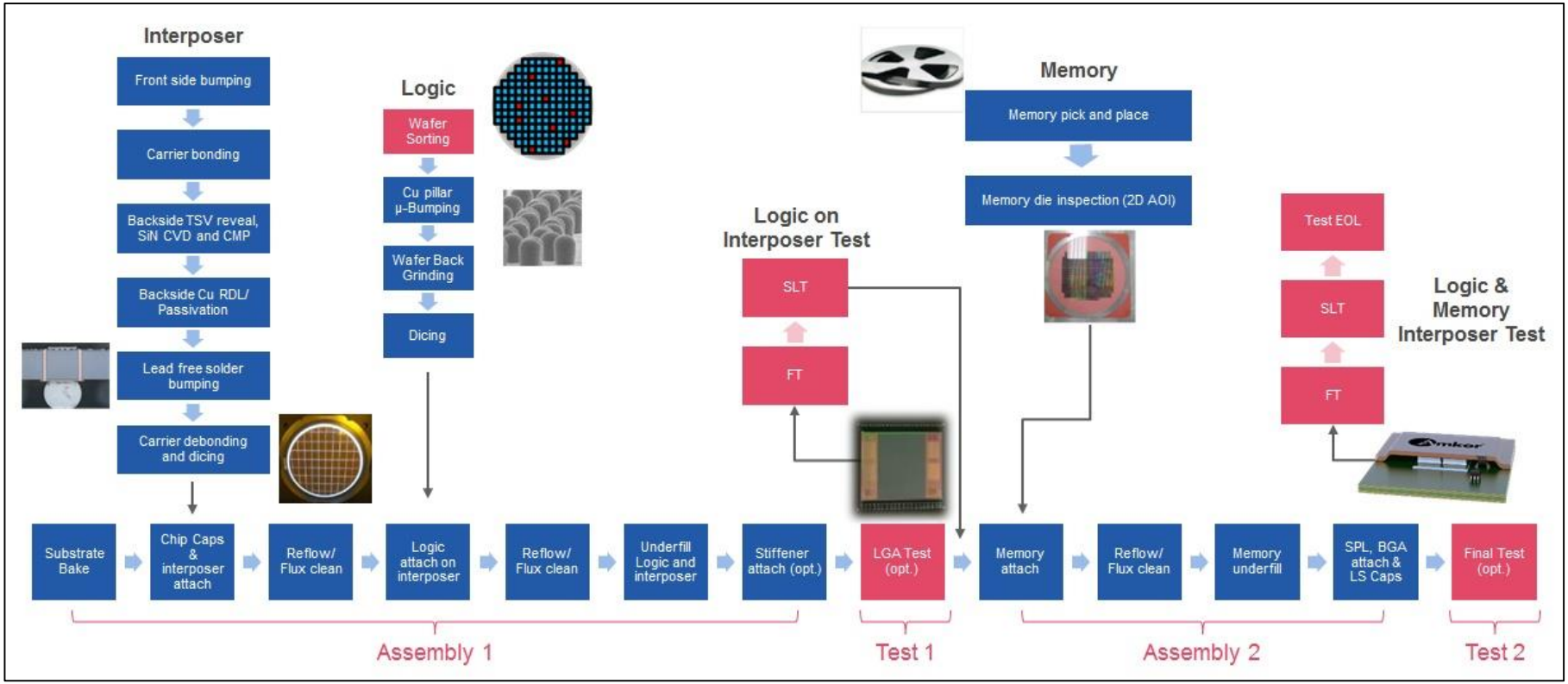


Can't control every step
=> Need combination of trusted resources and in-line checks

Optimal solution varies by assembly flow
=>Need semiconductor packaging process knowledge



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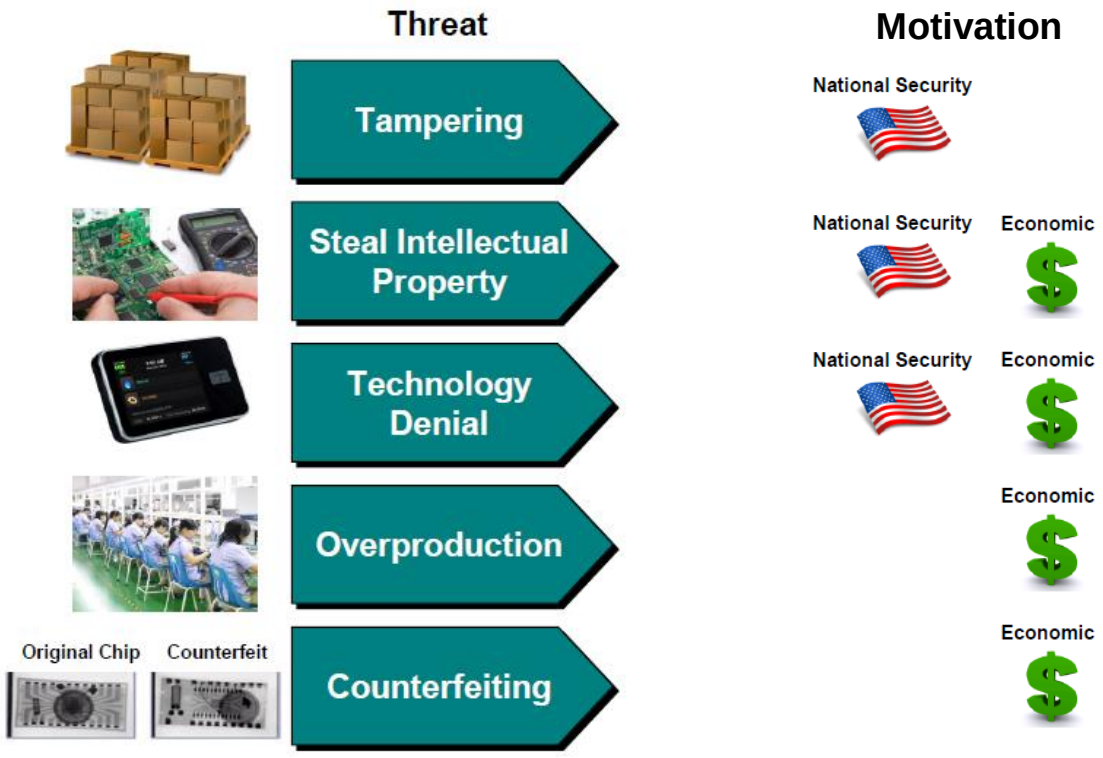
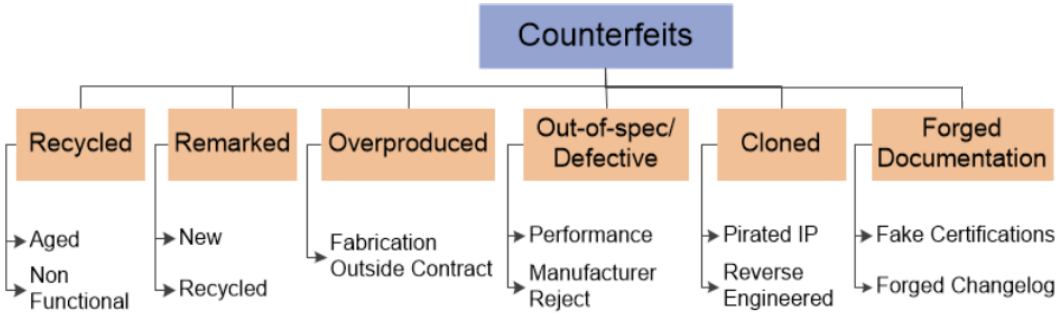
Semiconductor Security Vulnerabilities:
Many types of threats, motivated by financial and malicious interests



Many ways to profit via counterfeiting



Source: Mark Tehranipoor, "Counterfeit Detection and Avoidance," April 2018.
Source: "Supply Chain Hardware Integrity for Electronics Defense (SHIELD)," Serge Leef, Software and Supply Chain Assurance Winter Forum, Dec. 2018

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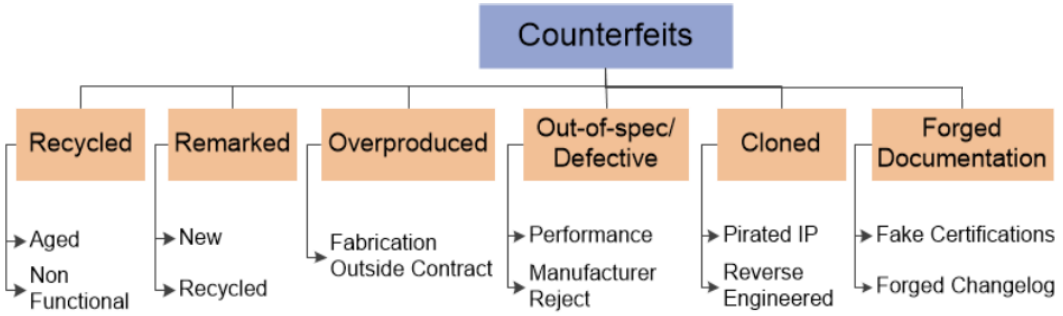
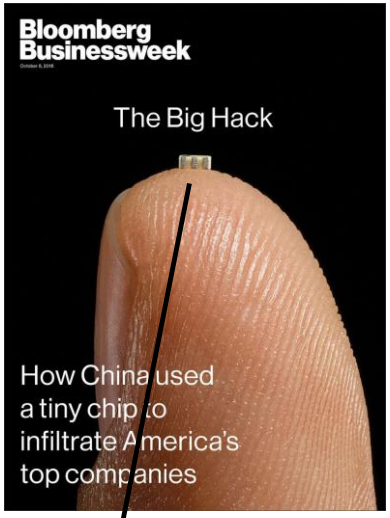
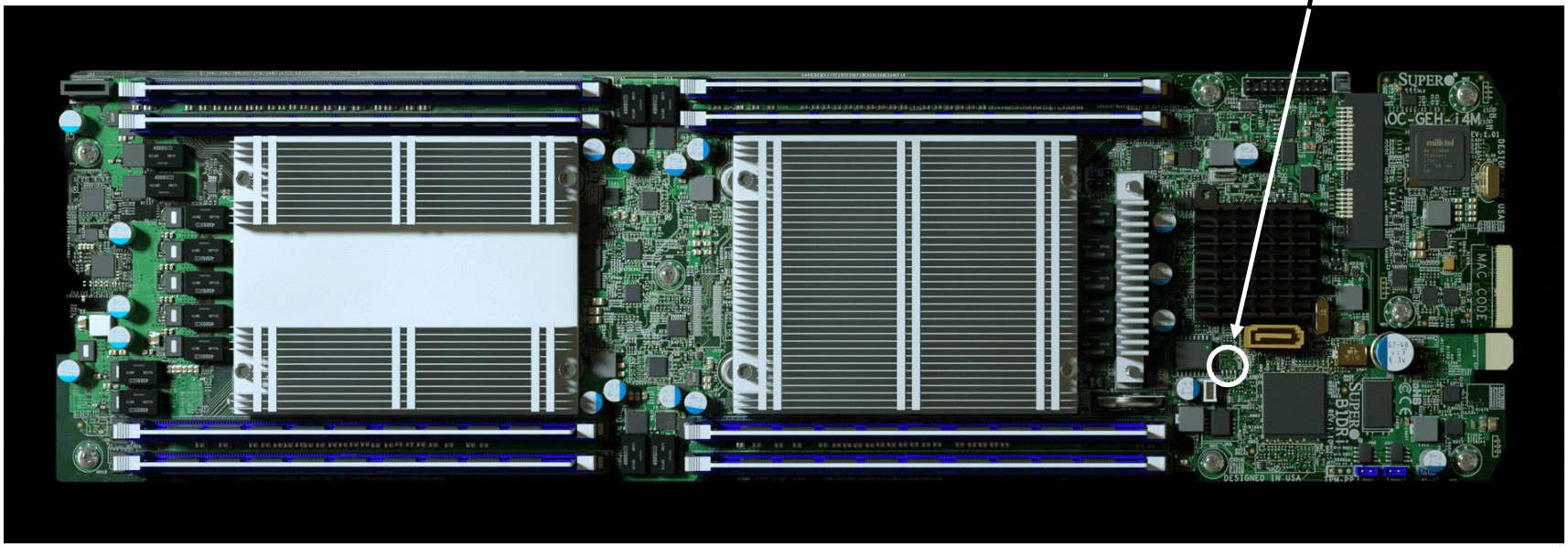


Source: Mark Tehranipoor, "Counterfeit Detection and Avoidance," April 2018.
Source: "Supply Chain Hardware Integrity for Electronics Defense (SHIELD)," Serge Leef, Software and Supply Chain Assurance Winter Forum, Dec. 2018

Supply Chain Vulnerability:
Headline-worthy hacking – full story still TBD, but illustrates the risk

- Recent reports of malicious interdiction in Supermicro server boards assembled in China
- Very broadly used in commercial and government systems (Amazon, Apple, CIA, etc.)
- High functionality components miniaturized, hidden, and disguised as other components
- Enable third party to control hardware, apparently done in parallel with SW/FW attacks





Source: Bloomber BusinessWeek, Aug. 2018

Government Focus on Semiconductor Packaging Security

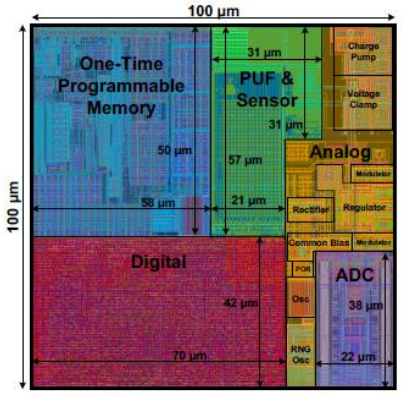
DARPA Microsystems Technology Office (MTO) PMs: Areas of interest => significant interest in security / packaging

		Areas of Interest (https://www.darpa.mil/about-us/people)																					
		Adaptibility	Automation	Communications	Cyber	Decentralization	Electronics	EW	Imagery	Integration	ISR	Leadership	Manufacturing	Materials	Microstructure	Microsystems	Photonics	PNT	Processing	Quantum	Security	Sensors	Spectrum	
MTO PM	Joined	2	2	2	2	1	8	3	2	3	1	1	3	5	1	5	3	2	1	1	2	5	7	Packaging Interests
Griffin, Ben	Oct-18						1							1								1	1	extreme environments
Rebello, Keith	Oct-18				1		1							1		1								
Burke, John	Aug-18							1		1							1	1		1		1		
Leef, Serge	Aug-18						1						1			1					1			Supply Chain, Security
Trimberger, Steve	Aug-18		1				1									1					1			Security
Mason, Whitney	Nov-17								1													1	1	
Chen, YK	Sep-17													1		1	1					1		Heterogeneous integration, materials
Keeler, Gordon	Aug-17						1			1						1	1							Photonics
Polcawich, Ron	Aug-17			1										1	1			1						MEMS
Olofsson, Andreas	Jan-17		1				1						1						1					HI, standards, automation, manufacturing
Hancock, Tim	Sep-16					1	1	1															1	Heterogeneous integration
Rondeau, Tom	May-16	1		1																			1	
Plaks, Ken	Jan-15				1			1						1										Security
Tilghman, Paul	Dec-14										1												1	
Lewis, Jay (DD)	Nov-14								1													1	1	
Salmon, Linton	Sep-14						1						1											Manufacturing, foundries
Chappell, Bill (OD)	Jun-14	1								1		1											1	

Source: https://www.darpa.mil/about-us/people

Another Approach to Trust:
SHIELD uses advanced assembly technology to verify a full assembly

Challenge and response to verify presence of trusted SHIELD dielet within

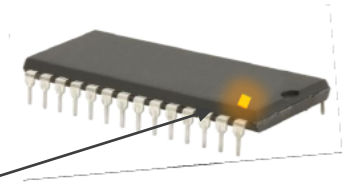


Dielet floorplan (Northrop Grumman)
14nm CMOS

Key SHIELD Specifications
- Unique Key Storage
- Full 256-bit AES encryption engine
- Unpowered, passive intrusion sensors
- RF power and communication
- Transfer fragility
- 100µm x 100µm
- 50 µW Total Power
- Operating temp < 120°C
- Cost < $0.01 per dielet

SHIELD Key Components

Dielet



Programmed on-reticle after manufacture

Installed on or within host IC package
- Embedded within package
- Custom package
- Epoxy to surface

No impact to host IC performance or reliability

Reader

Transmits at 5.8GHz to power dielet; 3.6GHz for data transfer

USB connection to smartphone, tablet or computer

Can be configured for high-volume interrogation (transaction time < 1 sec)

Remote Server

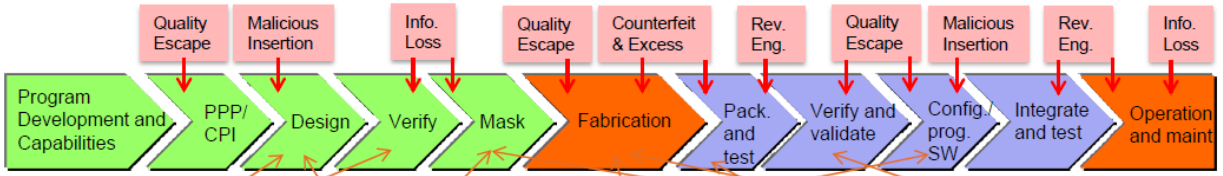
Communicates with reader via Internet connection; performers using Amazon and Microsoft web services

Maintains a record for each IC
- Manufacture date
- Part/package information
- Interrogation history

Source: "Supply Chain Hardware Integrity for Electronics Defense (SHIELD)," Serge Leef, Software and Supply Chain Assurance Winter Forum, Dec. 2018

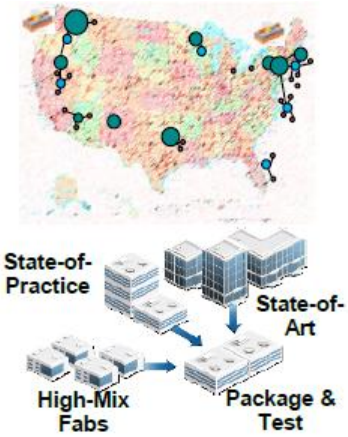
Microelectronics Innovation for National Security and Economic Competitiveness (MINSEC): Packaging is critical part of security

T&AM New Trust and Assurance Approaches



Design for trust	IP protection	Low-volume/high-mix production	Electronic component markers	Imaging technologies and forensics
• Designing techniques to limit full use/functionality to trusted operation	• Preventing exploitation, including control of use, concealment, reconfiguring, partitioning, or employment	• Innovative methods to permit cost-effective, Trusted and assured low volume manufacturing of state-of-the-art ICs	• Tagging/marking ICs and subassemblies to authenticate and track supply chain movements	• Advanced capabilities to efficiently evaluate dense, state-of-the-art commercial components

Implement and demonstrate assurance capability with transition partners



Domestic Foundry & Packaging

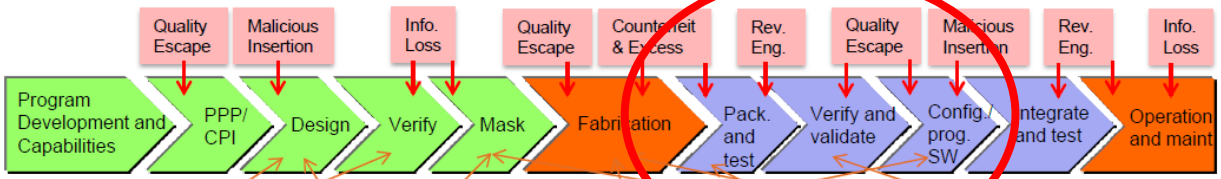
- Multiple competitive State-of-the-Art Foundries on shore
- Leadership in R&D and production
- Strong commercial business models
- Government business model for innovation & assurance

Source: "Long-Term Strategy for DoD Assured Microelectronics Needs and Innovation for National Economic Competitiveness," K. Baldwin, NDIA, Oct. 2018

Microelectronics Innovation for National Security and Economic Competitiveness (MINSEC): Packaging is critical part of security

Threats and opportunities concentrated at the back end

T&AM New Trust and Assurance Approaches



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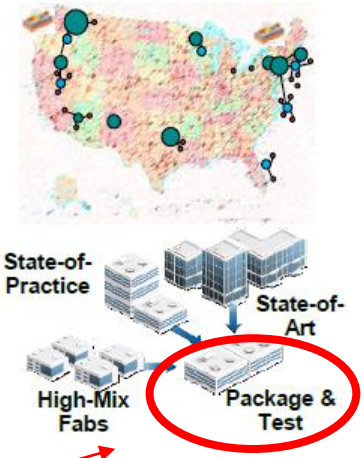

Solutions needed where all pieces come together

Domestic Foundry & Packaging

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- Leadership in R&D and production
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Source: "Long-Term Strategy for DoD Assured Microelectronics Needs and Innovation for National Economic Competitiveness," K. Baldwin, NDIA, Oct. 2018

Office of the Secretary of Defense, July 2019

Competitive Opportunities

Opportunity	Open Date	End Date	Reference
State of the Art (SOTA) Heterogeneous Integrated Packaging (SHIP) Prototype	3 Jul 2019	6 Aug 2019	https://s2marts.org/ Contact: S2MARTS@nstxl.org
Rapid Assured Microelectronics Prototypes using Commercial Design & Intellectual Property	4th Qtr FY19	------	https://s2marts.org/ Contact: S2MARTS@nstxl.org
Microelectronics Innovation for Next-generation System Advancement and Validation (MINSAV) Advanced Research Announcement Advanced Technology Center (ATC) for Data Processing	4th Qtr FY19	------	https://www.cto.mil/work-with-us/
Assured and Trusted Microelectronics Solutions (ATMS) Broad Agency Announcement (BAA)	Jan 2017	Nov 2022	FedBizOps Solicitation Number: FA8650-18-S-1201
Rapid Innovation Fund (RIF) Broad Agency Announcement (BAA)	4th Qtr FY19	------	https://www.cto.mil/work-with-us/

Source: Lisa Porter, OSD, DARPA MTO ERI Summit, July 2019

State of the art Heterogeneous Integrated Packaging (SHIP)

This Request for Solutions is anticipated to result in two awards, with each award respectively related to the focus areas below:

1) SHIP Digital: State of the Art Digital Design Center and Integrated Packaging and Assembly Test Center; and,

2) SHIP RF: State of the Art RF Design Center and Integrated Packaging and Assembly Test Center.

Item No.	Item/Deliverable	Quantity / Frequency	Deliverable Due Date
1	Phase 1 SHIP Report Comprised of Technical & Business Plans discussing the phases below: • Phase 2: *Advanced Prototype Capability Development and Initial Design Activities*; • Phase 3: *Install and Qualification of Processes*; • Phase 4: *Operate and Maintain Advanced Prototype Capability*	1 / Once	No Later Than six (6) months from project award.

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$25M for a six-month paper study!

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	• Phase 2: *Advanced Prototype Capability Development and Initial Design Activities*; • Phase 3: *Install and Qualification of Processes*; • Phase 4: *Operate and Maintain Advanced Prototype Capability*		

Current Project Budget: $25,000,000 is budgeted and available for the Phase 1 awards, while subsequent Phases will be funded upon successful completion of the previous Phase.

SHIP Advanced Prototype Capability Concept

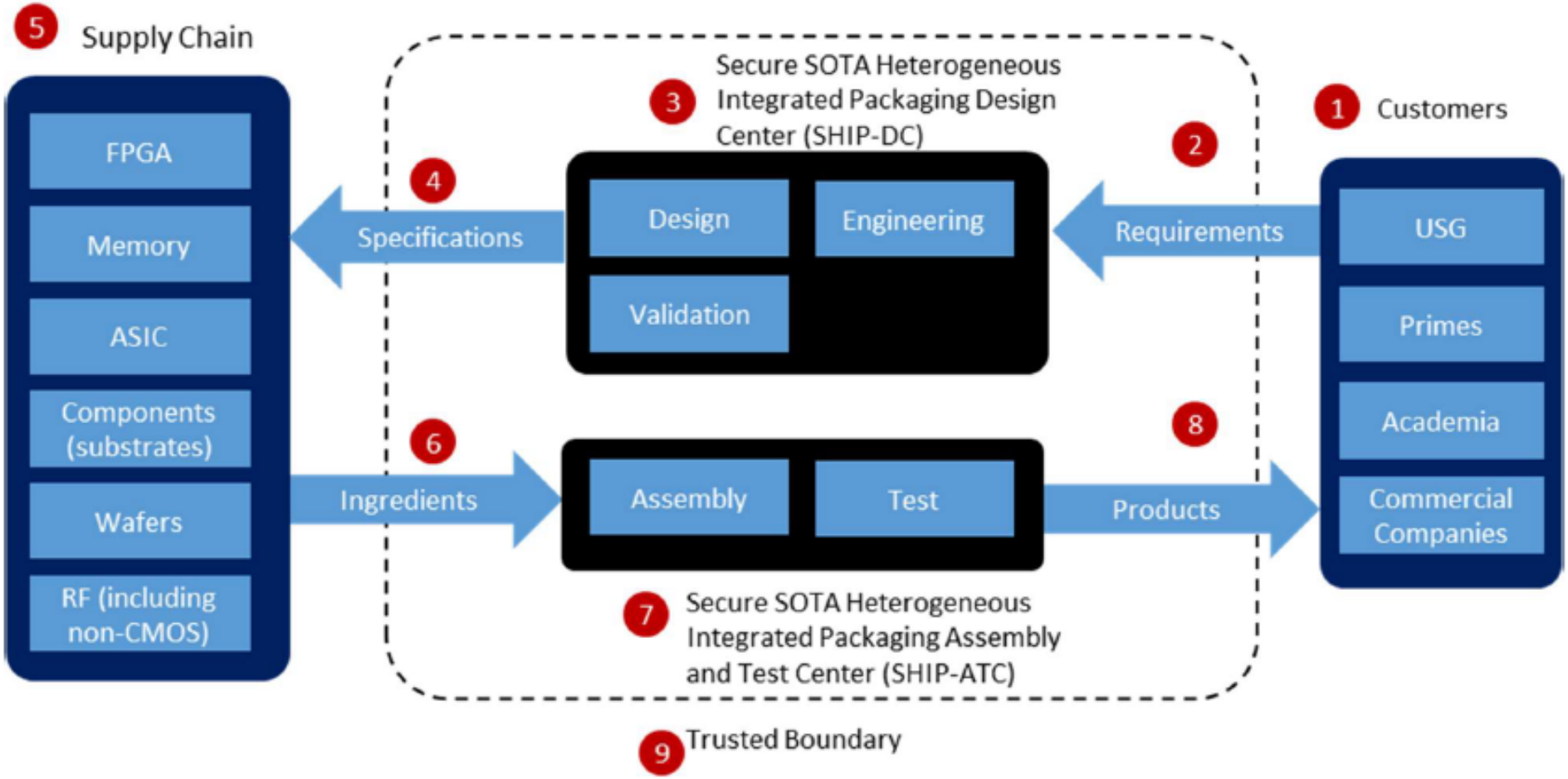


Figure 1 Notional design and prototype manufacturing flow

SHIP Capabilities

Table 3 General Capacity and Capability for the SHIP-ATC

Category	IOC	FOC	Scale
Capacity: Volume	**1k+**	**10k+**	**100k/mo+**
Silicon interposer	**Required**	**Required**	**Required**
Organic interposer	Preferred	**Required**	**Required**
Utilize SOTA COTS FPGA[1] and programmable devices	**Required**	**Required**	**Required**
Structured ASIC	Preferred	Preferred	**Required**
Security	Trust	ITAR	Classified
Number of Chips/Package[2]	4	8	12+
Supply Chain target	>50% US	>75% US	>90% US
Can process singulated die	**Required**	**Required**	**Required**
Can process up to 300mm wafers	Preferred	**Required**	**Required**
Can process 200mm die	Preferred	Preferred	**Required**

[1] Must include ability to integrate and test SOTA FPGA (<14nm), not required for RF centric applications

[2] Could include, but not limited to, memory, ADC/DAC, transceivers, optical couplers, ASIC, structured ASICs, etc.

SHIP Interposer Specs

Table 4 Silicon Interposer Foundry Specifications

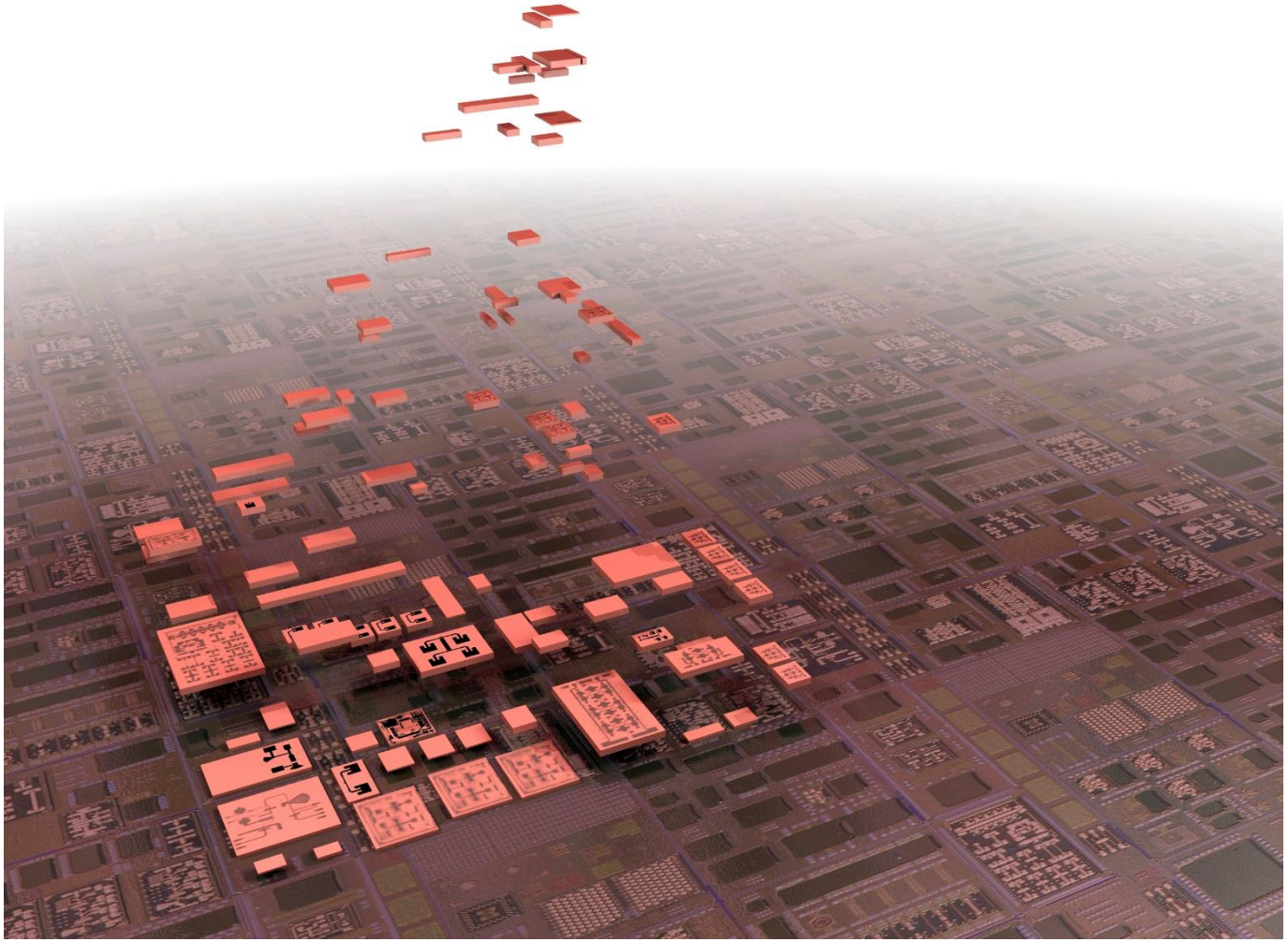
		IOC	Final State
Size	Interposer Area	26x33mm	(26x33mm) X 2 with stitching (1)
Front-side	Wiring Density	1000-1600 IO/mm	1600 IO/mm (2)
	Metal Layers	(0.4/1.08/4.0) µm (1.08/1.08/4.0) µm	(0.4/1.08/4.0) µm (1.08/1.08/1.08/4.0) µm
	Bump Pitch	50µm	36µm
Middle	TSV Pitch	55µm Min	45µm Min
Back-side	Bump Pitch	55µm Min	45µm Min

SHIP Assembly Specs (sample)

Table 6 Advanced Microelectronics Assembly Specifications

		IOC	Final State
		IOC	**FOC**
Chip on Chip	Silicon Interposer Sizes	(22 x 33) mm	(22 x 33) mm
	Top Chip Process	All leading processes from 180nm to 7nm	
	Chip Size Range	(2 x 2) mm to (21 x 32) mm	(1 x 1) mm to (21 x 32) mm
	Chips Placed Per Interposer	20	
	Chip Spacing	100 µm	100 µm
	Chip Bump Pitch	50 µm	36 µm
	Total Connections		
	Number of chips in 3D stack	21 (estimate only)	> 21 (estimate only)
Chip on Substrate	Max Organic Substrate Sizes	(76 x 74) mm	(100 x 100) mm
	Substrate C4 Bump Pitch	55 µm	45 µm
	Chips Placed Per Substrate	7	12
	Chip Spacing	100 µm	100 µm
Packaging	Features	• High performance polymer and solder thermal interface materials integrated with Cu heat spreaders for improved thermal performance • Package substrates that are optimized for low loss high speed signaling	

Future of heterogeneous integration



Requires a lot of pieces coming together!

Source: DARPA