Thin Is In: The Challenge and Solution of Picking Thinner Die

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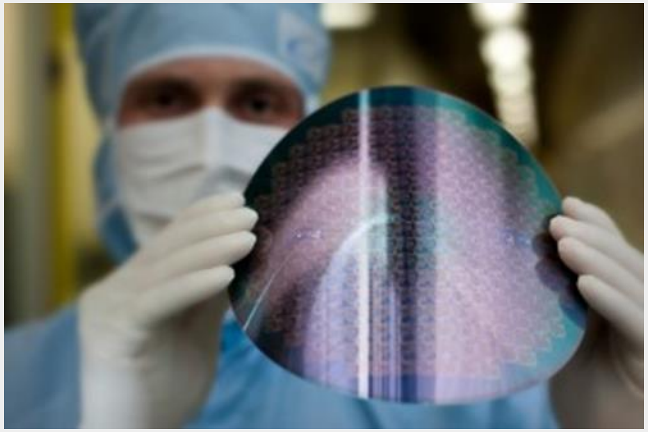
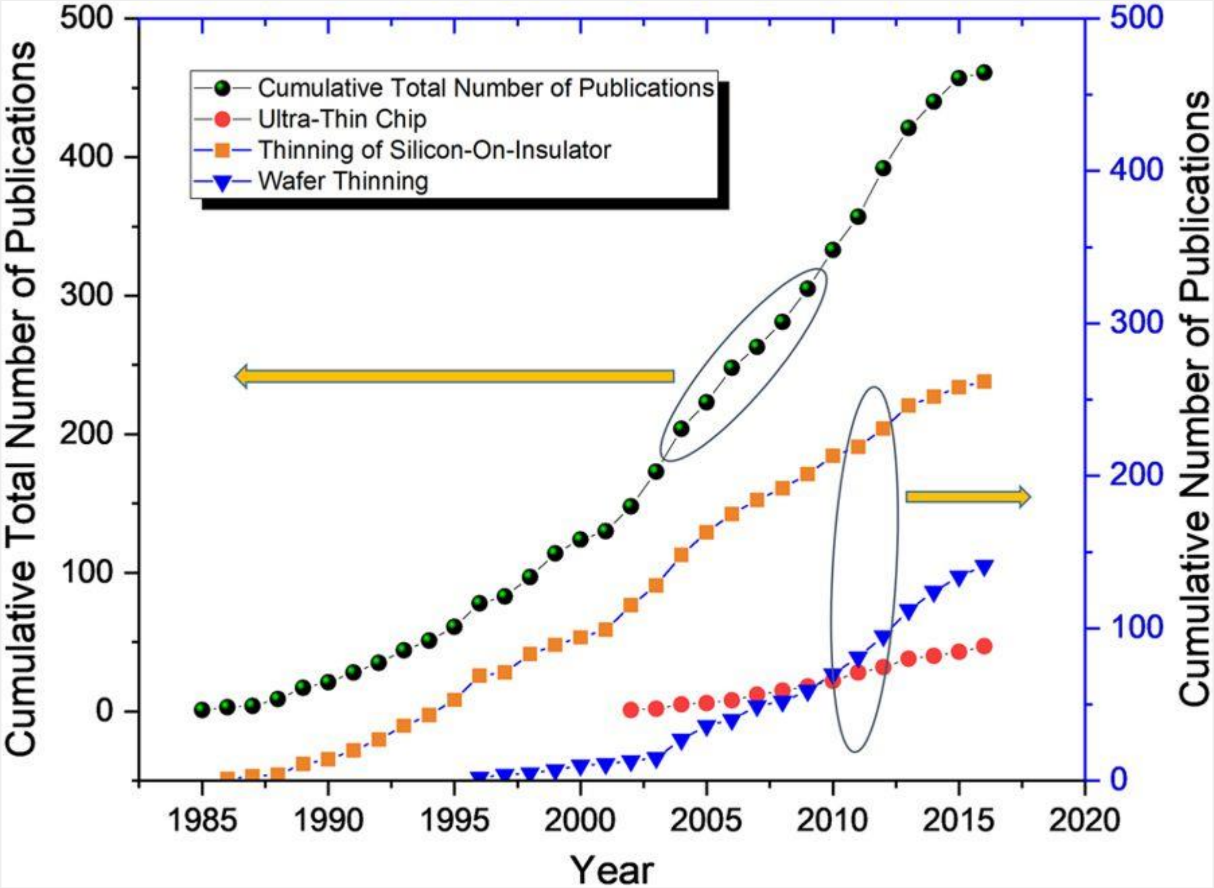
Outline

- Industry trends towards thinner die
- Challenges of thin die wafer removal
- Solutions for today’s devices
- The next steps for thinner die
- Conclusion
- Q&A



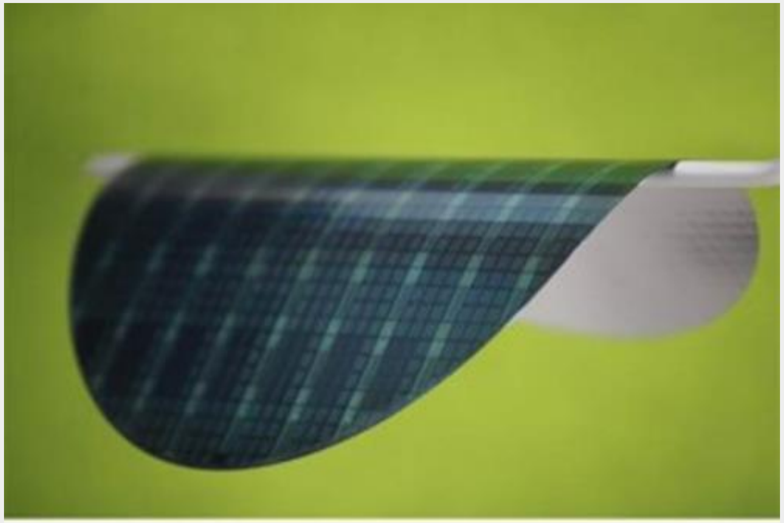
Growth of Interest



Cumulative number of publications in major areas related to thin-Si based electronics, including UTCs [*Source*: Web of Science]

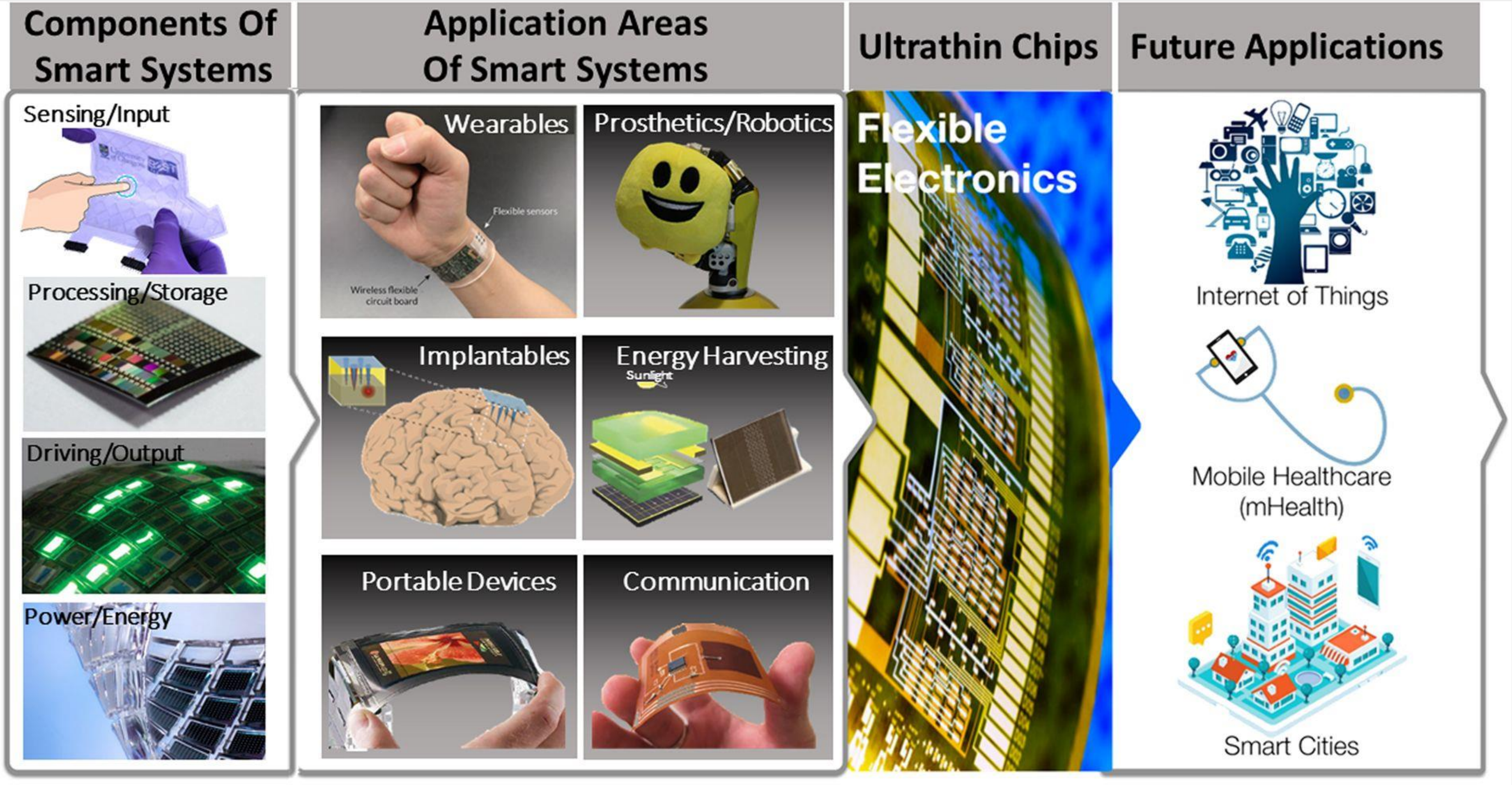
Industry Trends: Applications

- Communications/Radar (MMICs)
- Power (IGBTs & Power MOSFETS)
- Wearables (Flexible Electronics)[1]
- Mobile Devices (2.5 & 3D Integration: SiP, PoP)[2]



[*Source:* 1. npj Flexible Electronics(2018) 2:8 ; doi:10.1038/s41528-018-0021-5
2. G. Parès, A. Attard, F. Dosseul, A. N'Hari, O. Boillon, L. Toffanin, G. Klug, and G. Simon (2013) DEVELOPMENT OF AN ULTRA THIN DIE-TO-WAFER FLIP CHIP STACKING PROCESS FOR 2.5D INTEGRATION. International Symposium on Microelectronics: FALL 2013, Vol. 2013, No. 1, pp. 000516-000522.]

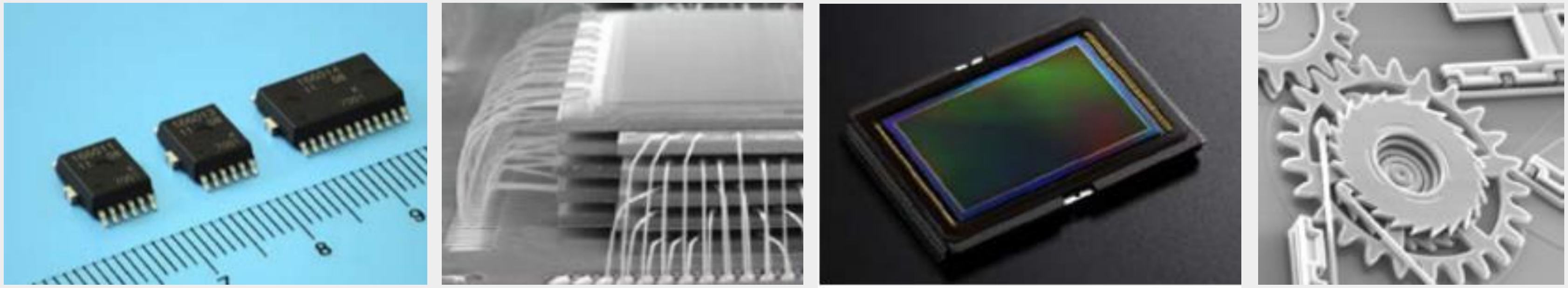
Ultra thin devices in the future for flexible electronics



[*Source*: npj Flexible Electronics(2018) 2:8 ; doi:10.1038/s41528-018-0021-5]

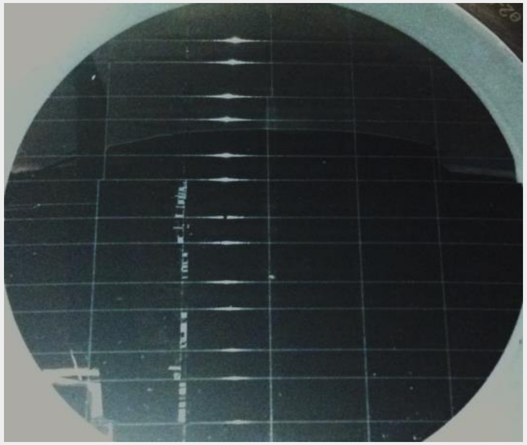
Industry Trends

- Drivers[1]
  - Reduce package size
  - Reduce device size
  - Increase performance
- Materials
  - Si
  - GaAs
  - Sapphire
  - GaN
  - InP
  - SiC



[*Source:* 1. Laura Mauer, John Taddei, and Scott Kroeger (2017) Wafer Thinning for Advanced Packaging Applications. Additional Conferences (Device Packaging, HiTEC, HiTEN, & CICMT): January 2017, Vol. 2017, No. DPC, pp. 1-26.]

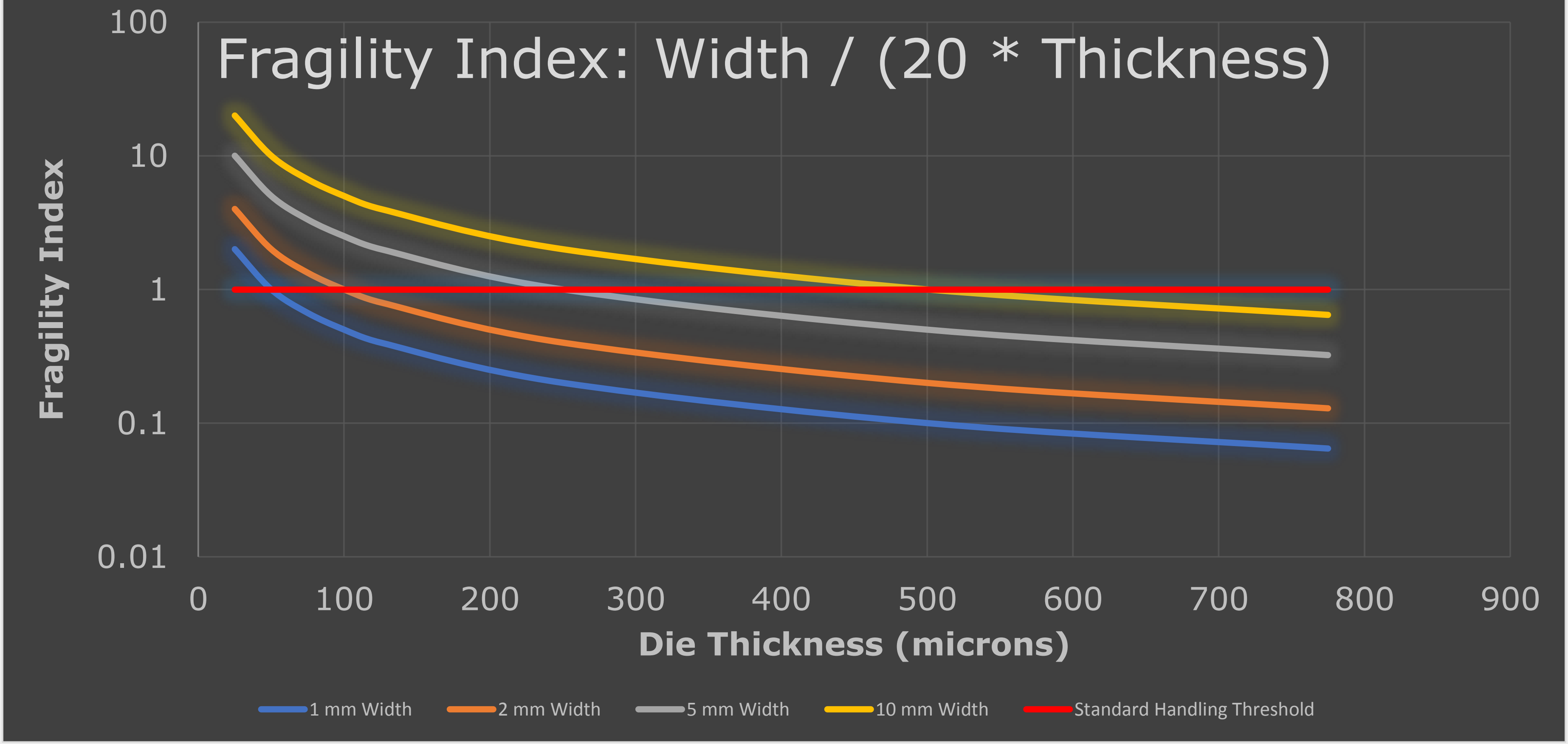
Challenges of Removing Thin Die from Wafer (Manual or Machine)



35 x 15 x 0.05 mm Si

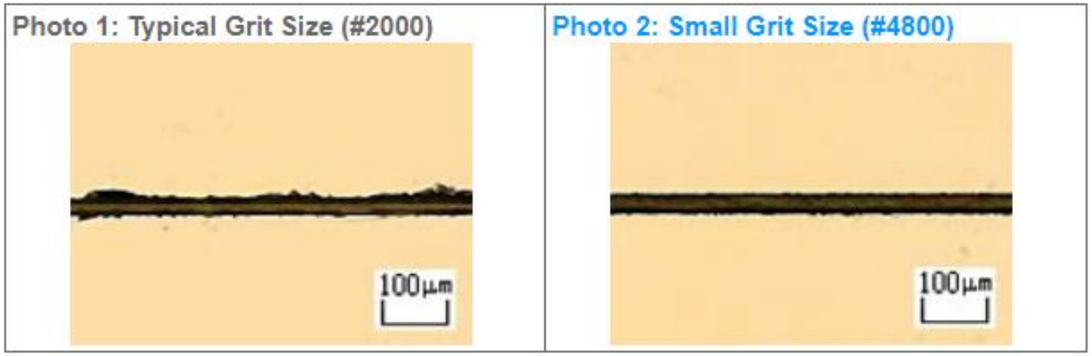
- Low Yield (breakage/microcracking)
  - Varying tape adhesion
  - High contact force
  - Lack of planarity of tool to device
  - Poor quality (upstream processing issues)
- Low Speed (higher cost to manufacture)
  - Needed to reduce force on device
  - Needed to allow time for tape to peel from device

Threshold for Special Handling by die thickness at varying widths



Solutions: Up-stream Processing

- Singulation
  - Dicing Before Grinding
  - Stealth Dicing
  - Blade Grit
  - Step Cut
  - Processing Conditions
  - Polishing/Etching
- Dicing Tape
  - Selection (UV vs non-UV)
  - UV cure process

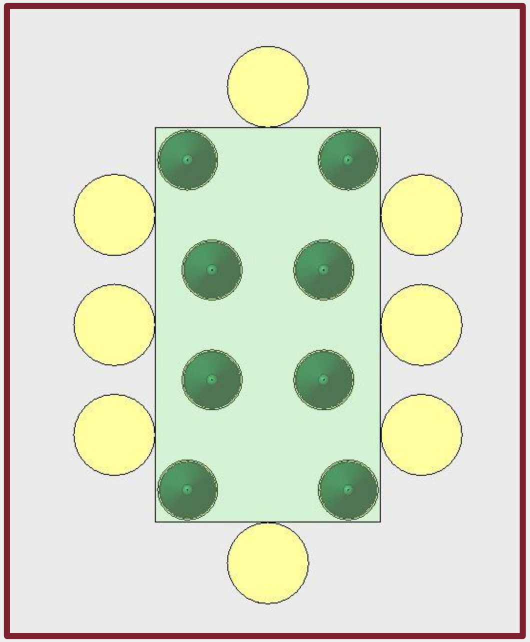


[*Source:* DISCO http://www.discousa.com/eg/solution/library/dicing_thin.html]

Solutions: Tooling Design

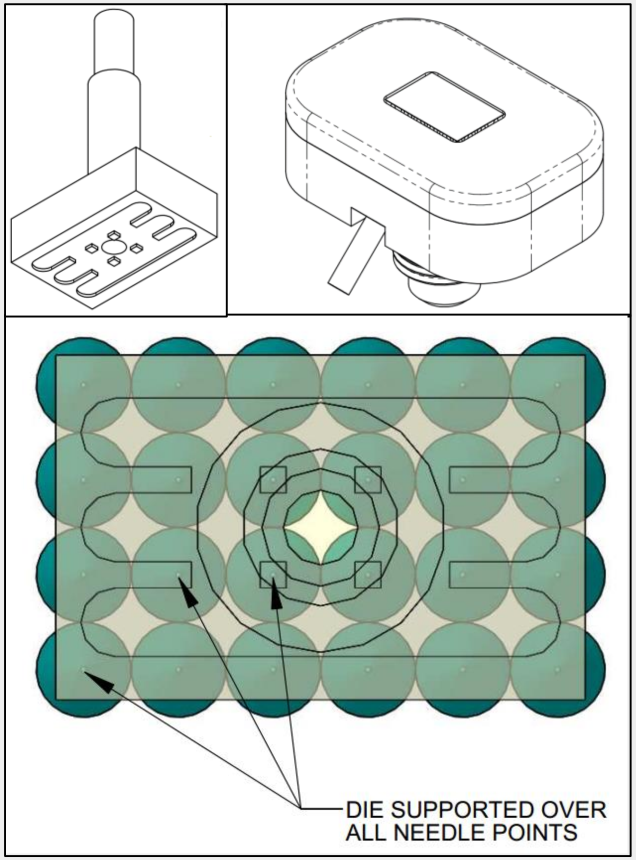
- Pick-up Tool
  - Surface vs. Non-Surface Contact
  - Material (Rubber, Vespel, Tungsten Carbide)
- Ejector
  - Vacuum Holes
  - Needle Configuration
  - Needle Radius

Ejector Design for
6x3x0.05 mm Device



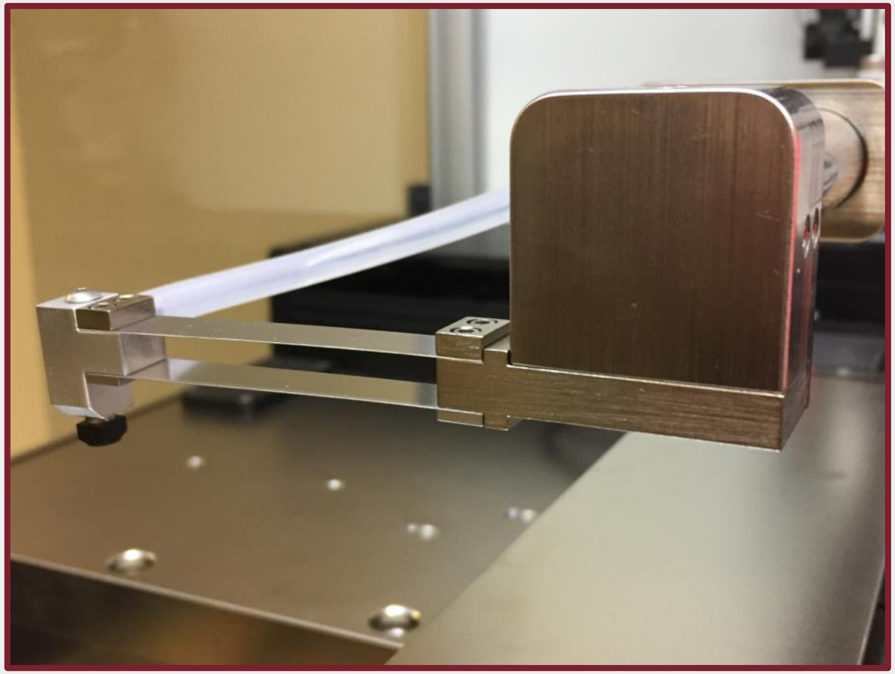
Solutions: Tooling Design

- Tooling designed to work together
  - 0.6 x 0.4 x 0.002 inch Si die
  - Pick-up Tool: Tungsten Carbide Surface Contact Vacuum
  - Ejector: 24 tungsten carbide needles, 75 micron tip radius



Solutions: Process Control

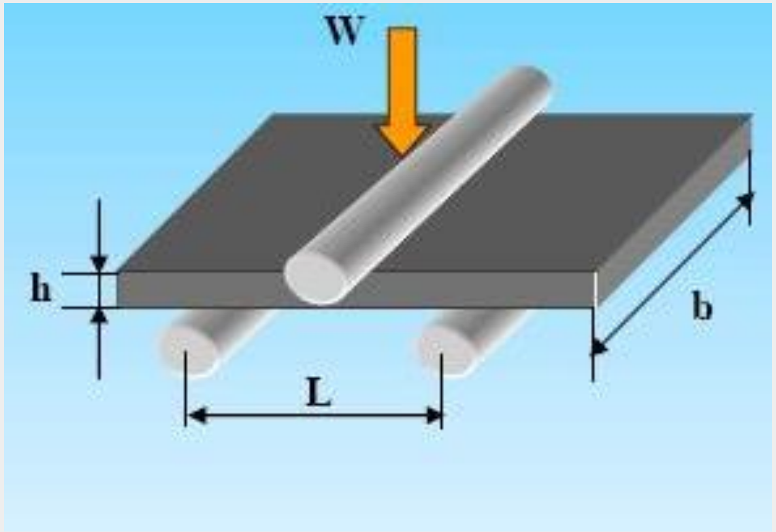
- Speed
- Alignments & Planarization
- Force Minimization (flexure based pick-up head)
- Role of Vacuum



Case Study: 10 mm x 10 mm

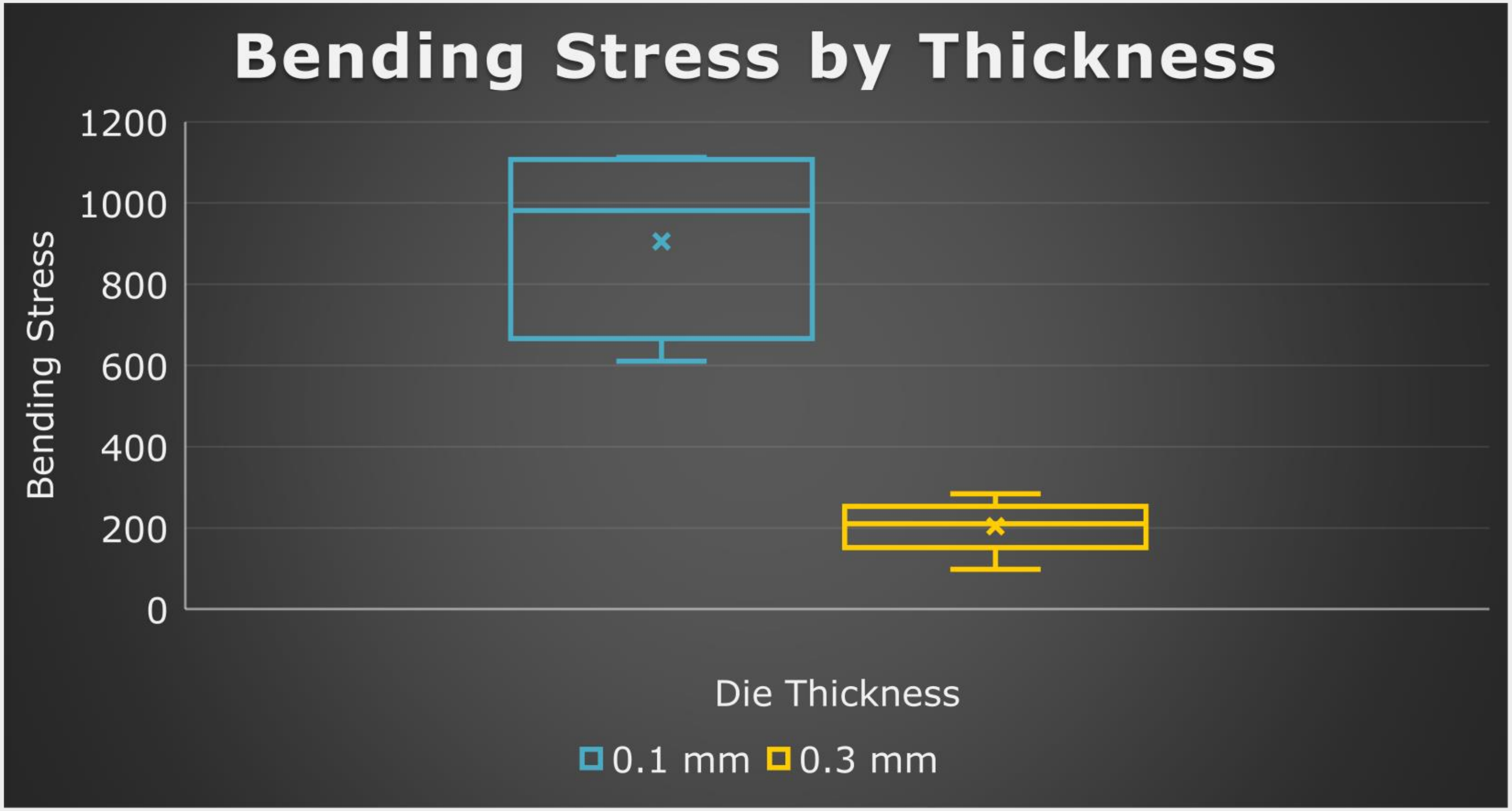
Comparison of 100 micron thick die vs 300 micron thick die

Initial Evaluation:
Die Strength via
Three Point
Bend Test



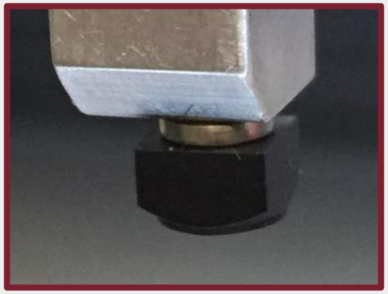
Data collected using Royce Instruments 650 Universal Bond Tester

Case Study: 10 mm x 10 mm



Data collected using Royce Instruments 650 Universal Bond Tester

Case Study: 10 mm x 10 mm



- Tooling Design
  - Pick-up Tool
    - Nitrile Rubber
    - 5 mm OD
  - Eject Head
    - 16x Eject Needles (75 um tip radius)
    - Needle envelope 7.24 x 7.24 mm

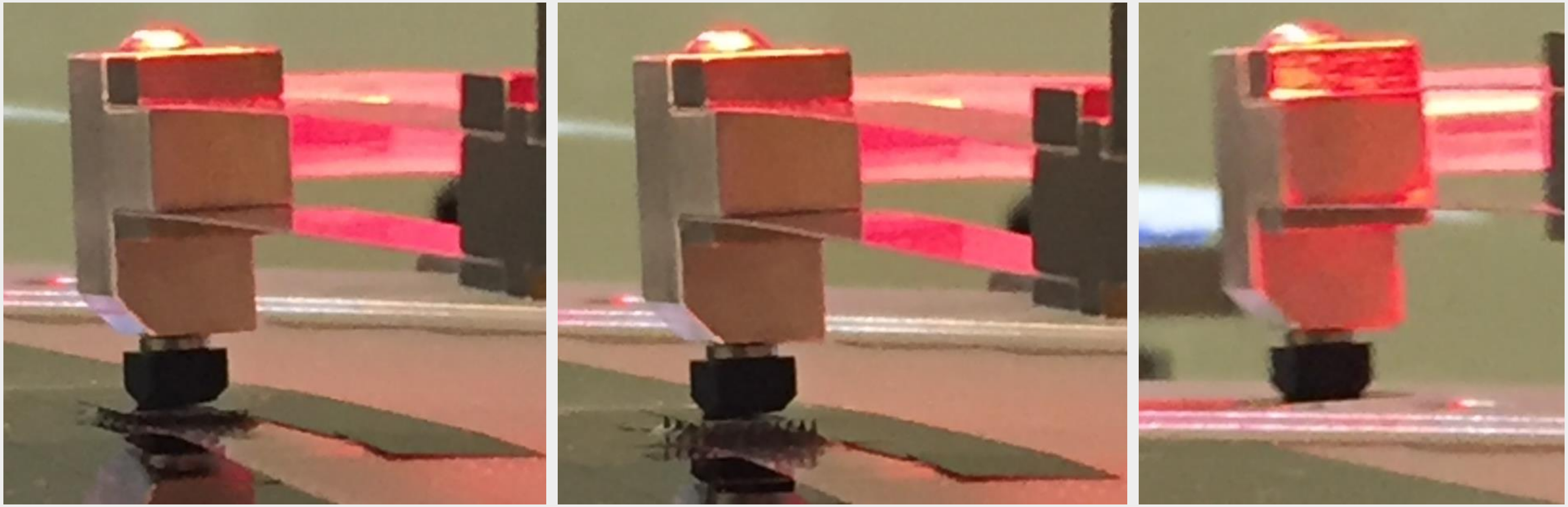
Same tooling used for both die thicknesses

Case Study: 10 mm x 10 mm

Parameter	**100 µm thickness**	**300 µm thickness**
Eject Height (µm)	2550	2150
Eject Velocity (% of maximum)	15	100
Delay Before Lift (milliseconds)	1000	0
Throughput (units per hour)	325	1200

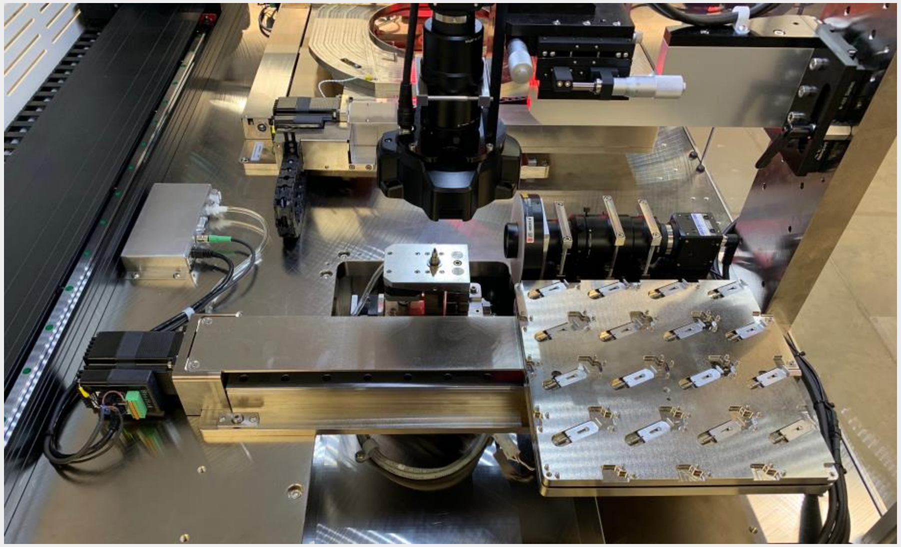
Data collected using Royce Instruments AP+ Automated Die Sorter

Case Study: 10 mm x 10 mm



100% Successful Die Removal from Dicing Tape

Case Study: 10 mm x 10 mm



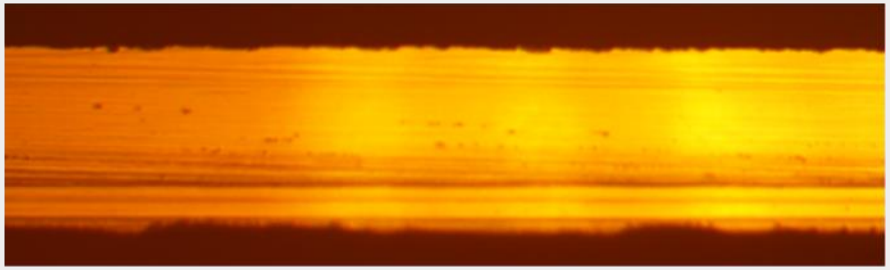
In-line inspection after pick, before place

Post-Pick Top Surface or Side-Wall Inspection for Quality Verification

Thin Die Post-Pick Defects

- Backside Chipping
- Sidewall Cracks
- Surface Contamination
- Metal Delamination

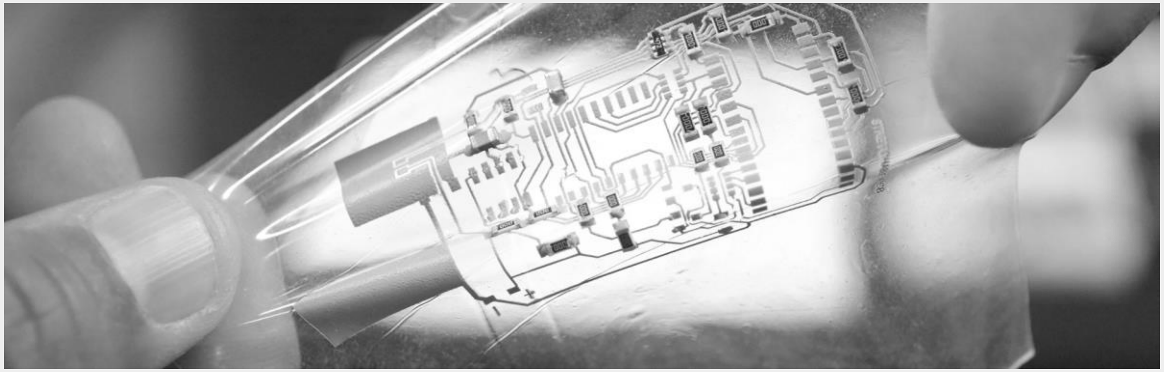
Edge as viewed from top of die
(optics magnification 200x)



Edge as viewed from side of die
(optics magnification 200x)

Next Steps: Industry Direction

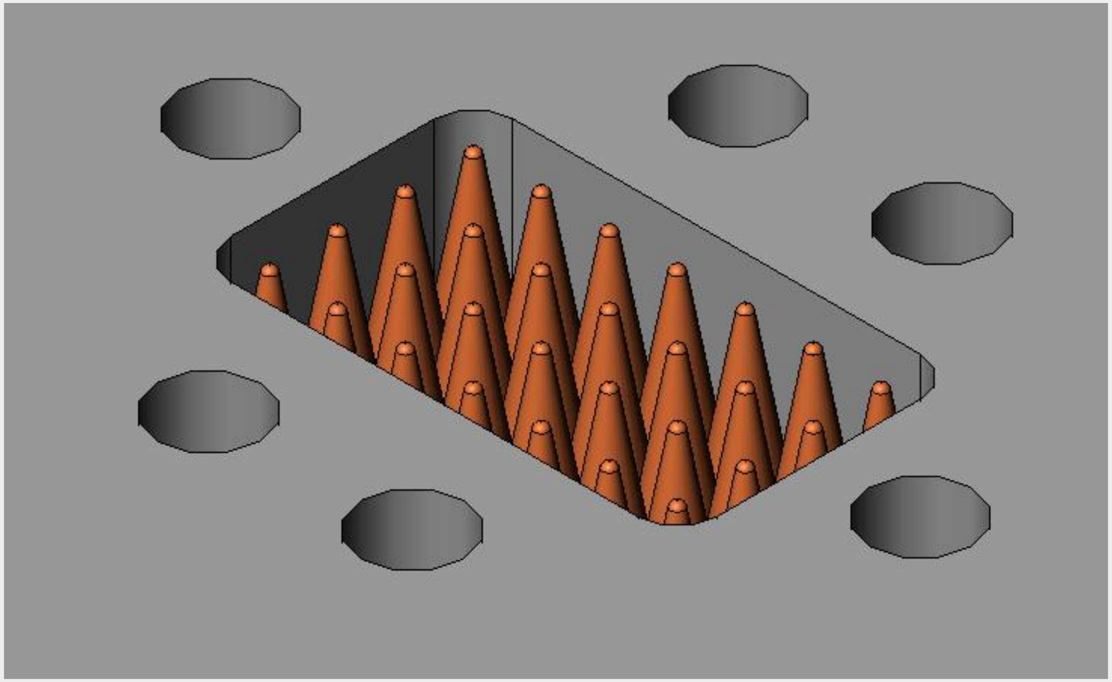
- Larger devices with same thickness
  - 20 mm x 20 mm x 0.075 mm GaAs
  - 25 mm x 25 mm x 0.055 mm Si
  - 30 mm x 30 mm x 0.100 mm Si
- Thinner devices (<25 micron thickness)



[Source: *NextFlex*]

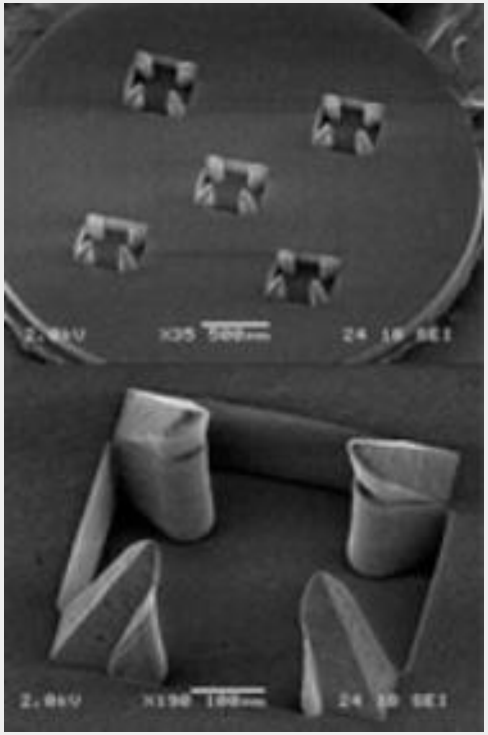
Next Steps: Current Limitations

- Dependent on upstream processing success
- Device size specific
- Scalability of packed needle array design
- Maintaining tool planarity



Next Steps: R&D Areas

- Die eject without needles
- Needle array micro-machining
- Advanced software process control
  - Dynamic force monitoring
  - Synchronized lift
  - Vacuum control
- Increase throughput



Stainless Steel 4x4 Microneedle Array

[*Source*: https://doi.org/10.1016/j.mser.2016.03.001]

Conclusion

- 50 to 100 micron thick devices able to be processed via optimization of tape, singulation process, die eject process parameters, and tooling design
- As device fragility increases, advances in handling technology needed

Q & A

Thank you!

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