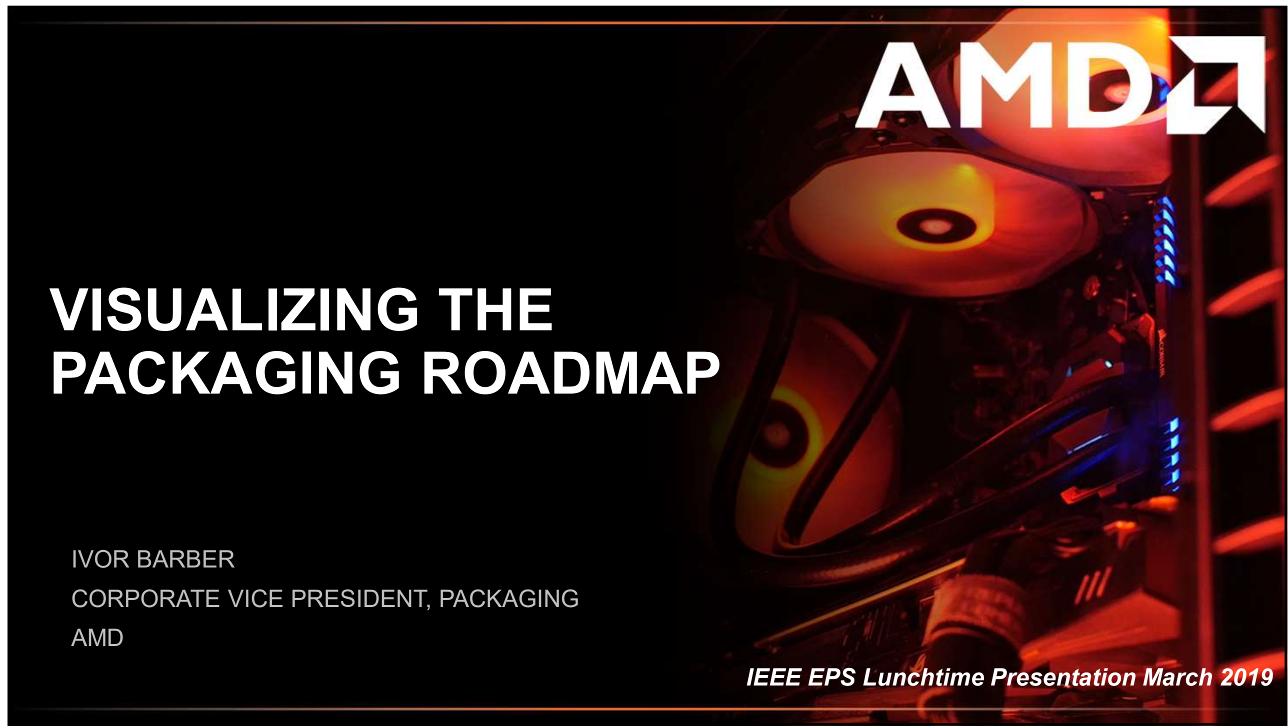


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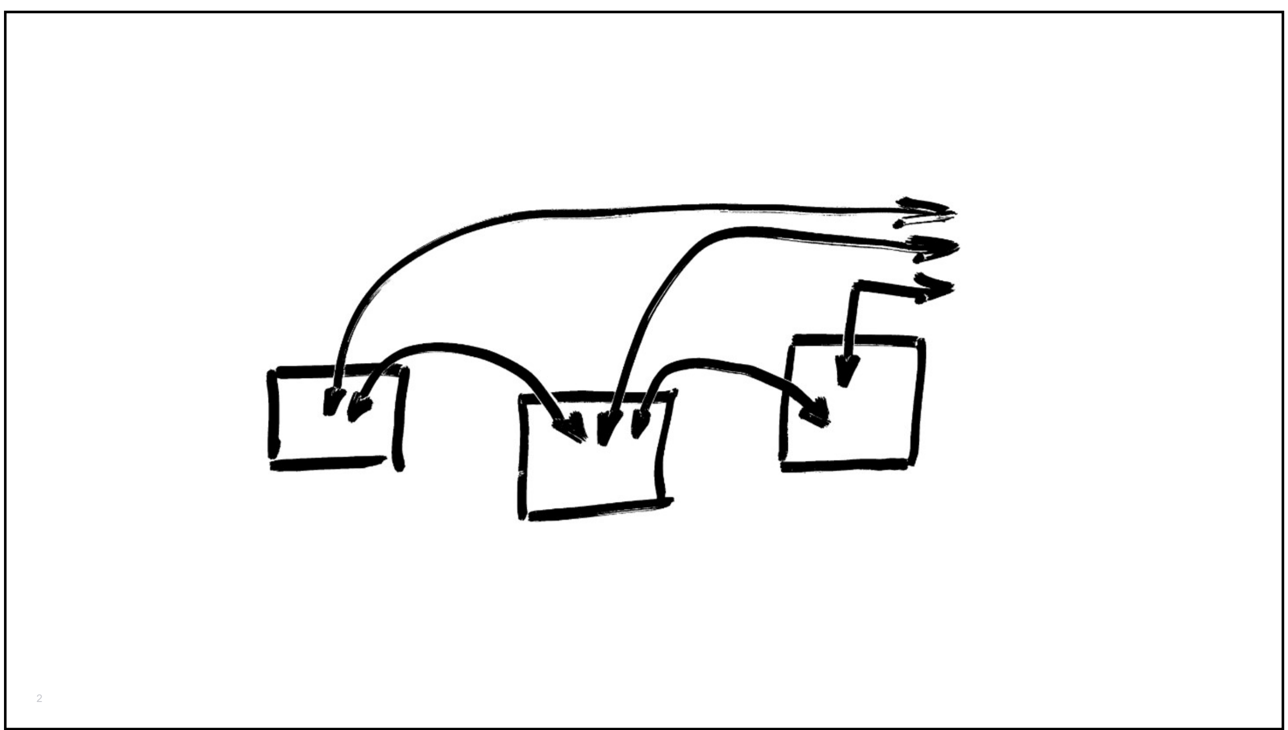

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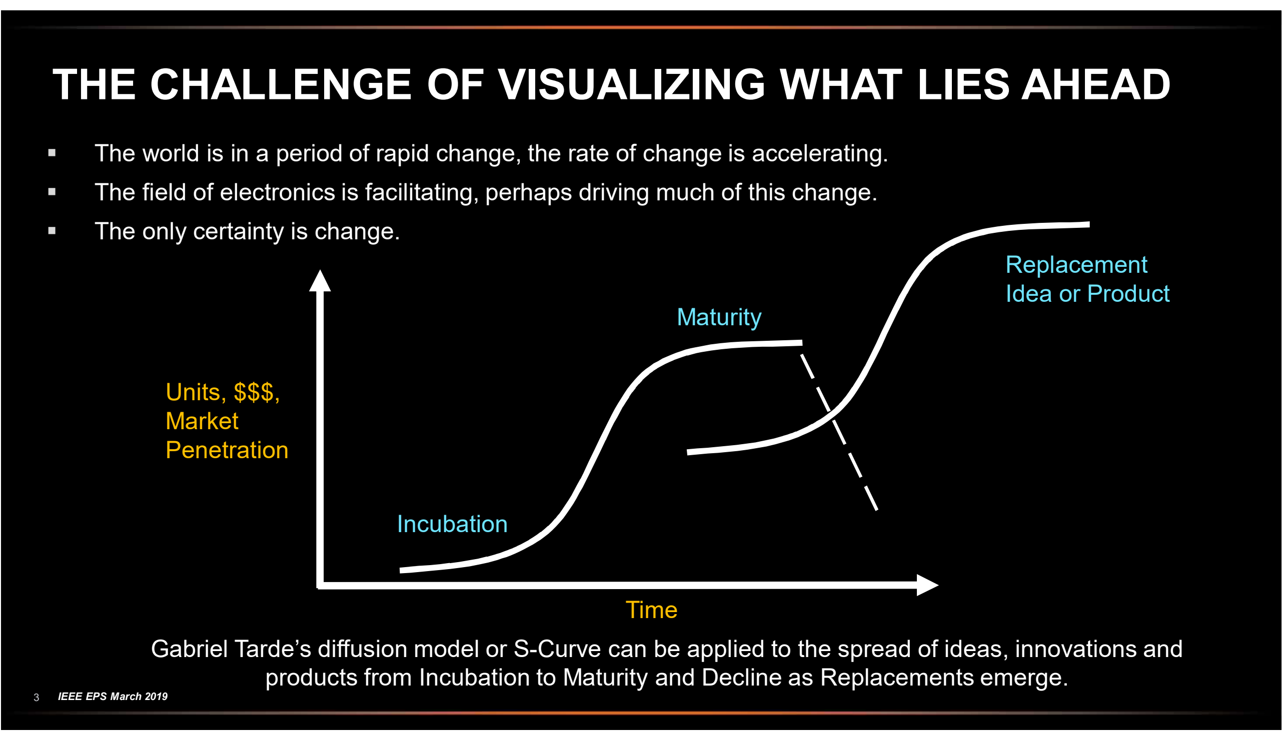


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# NEXT GENERATION PACKAGING (1990'S)

Brainstorming a list of the desirable attributes of a next generation package format.

- Organic
- Array Based
- High Pin Count
- Surface Mount
- Highly Manufacturable
- High Yielding
- Highly Reliable
- Low Cost

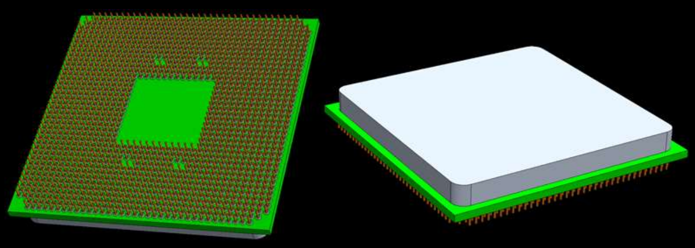




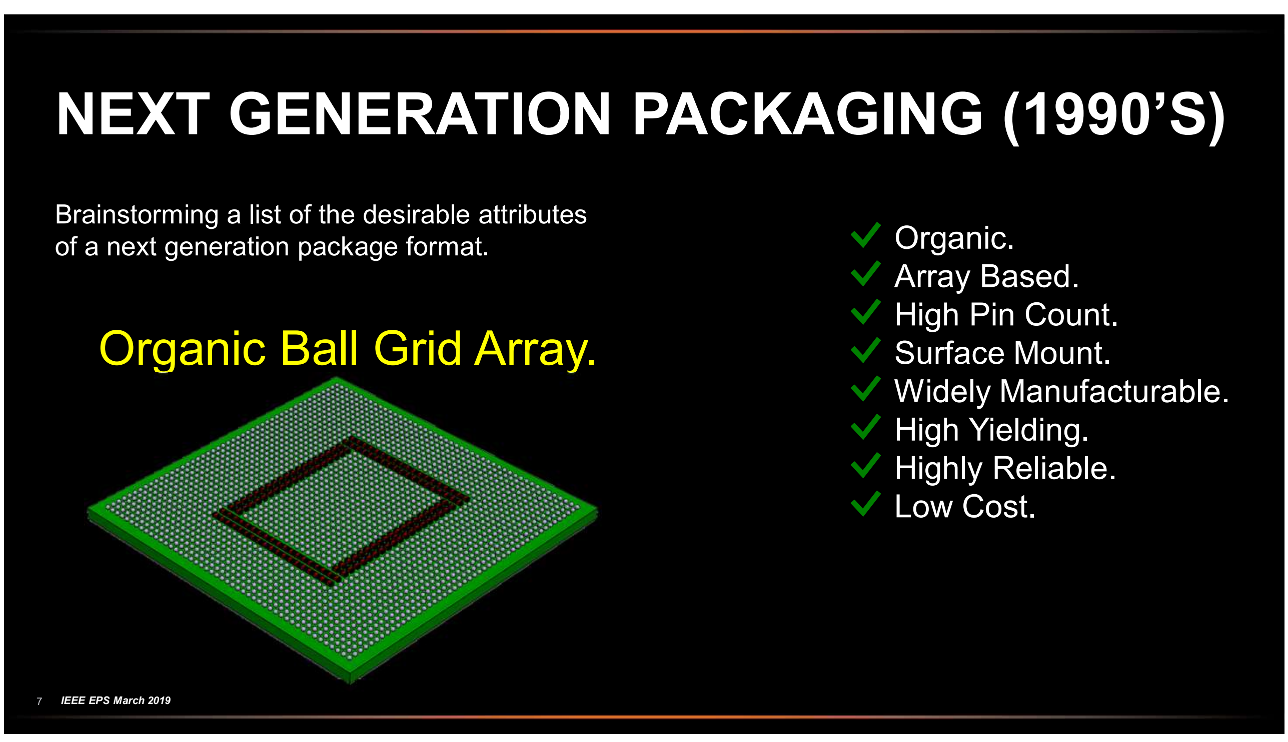
# NEXT GENERATION PACKAGING (1990'S)

Brainstorming a list of the desirable attributes of a next generation package format.

Organic, Fine Pitch, Surface Mount Pin Grid Array.



- ✓ Organic.
- ✓ Array Based.
- ✓ High Pin Count.
- ✓ Surface Mount.
- X Widely Manufacturable.
- X High Yielding.
- ✓ Highly Reliable.
- X Low Cost.

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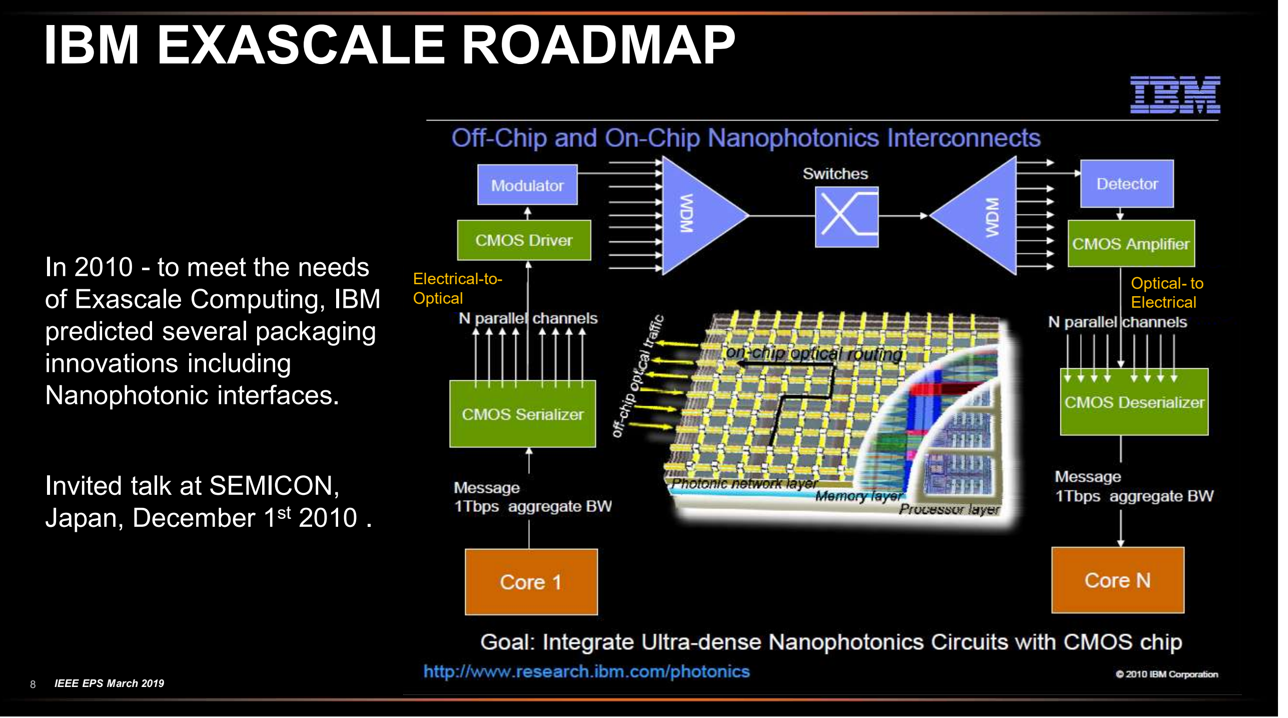


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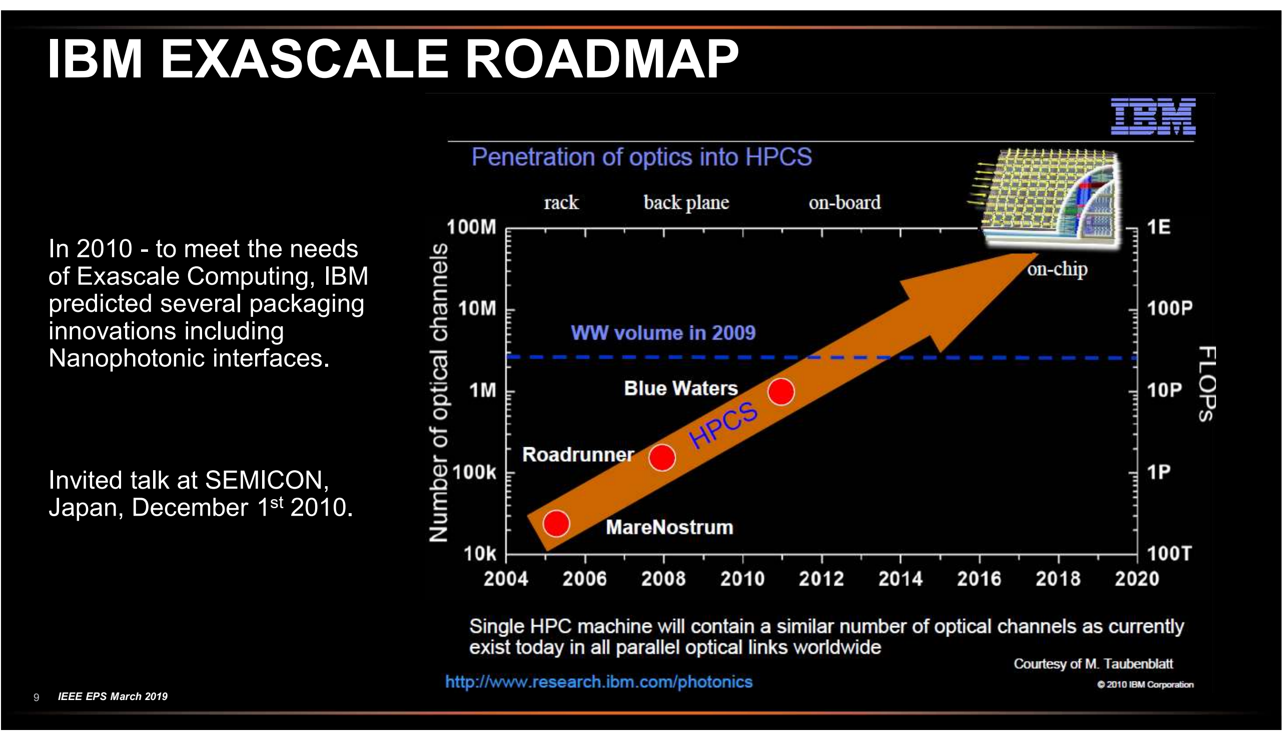
# IBM EXASCALE ROADMAP

In 2010 - to meet the needs of Exascale Computing, IBM predicted several packaging innovations including Nanophotonic interfaces.

Invited talk at SEMICON, Japan, December 1st 2010.




9 *IEEE EPS March 2019*

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# THE EMERGENCE OF MULTI-DIE PACKAGING

- The slowing of Moore's Law as an economic driver has led to renewed interest in multi-die packaging.
- Traditional SOC scaling has hit cost barriers which make die partitioning economically viable for high end packaging.
  - Xilinx used silicon interposers with TSV (2.5D).
- Traditional SOC scaling has fundamental barriers which prohibit monolithic integration of analog, logic and memory circuits.
  - Multi-die packaging will replace both Moore's Law and SOC scaling as the economic and technological driving force of the Semiconductor Industry.

10 *IEEE EPS March 2019*

Attribution : Bill Bottoms, Various HIR Roadmap Presentations

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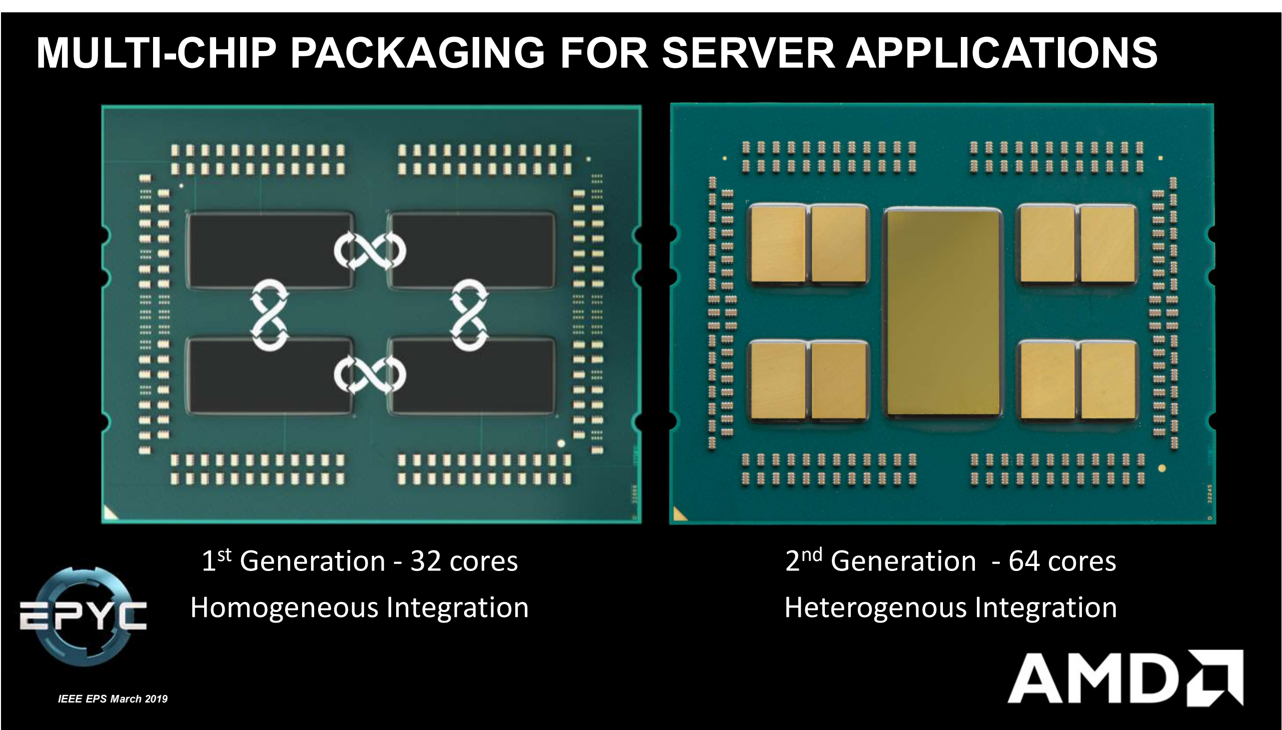


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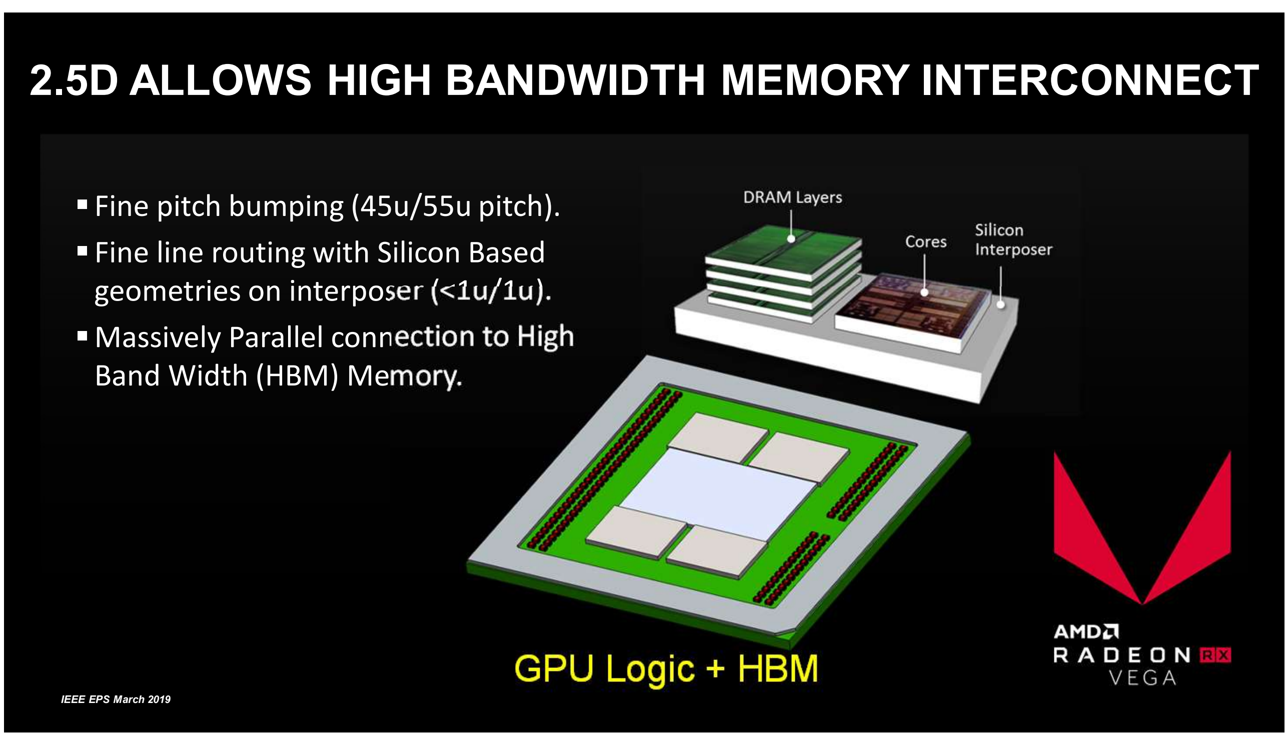


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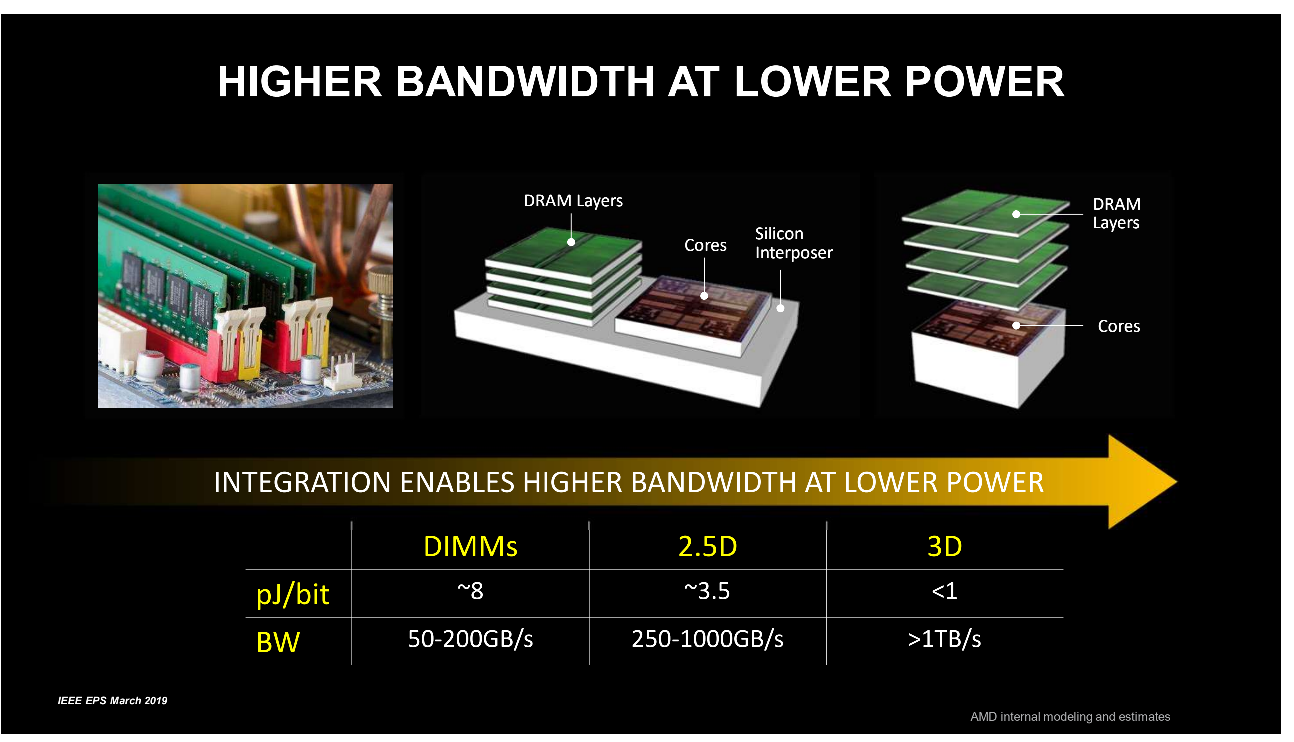


| | DIMMs | 2.5D | 3D |
|---|---|---|---|
| pJ/bit | ~8 | ~3.5 | <1 |
| BW | 50-200GB/s | 250-1000GB/s | >1TB/s |

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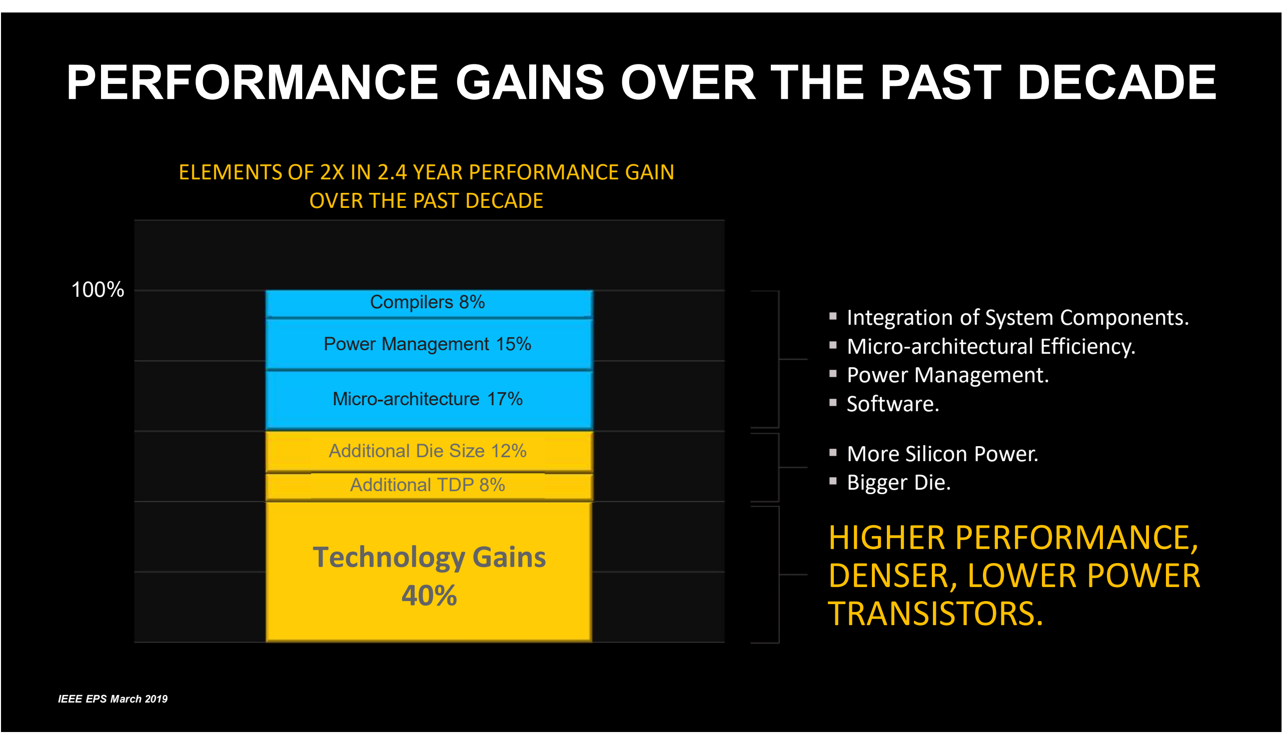


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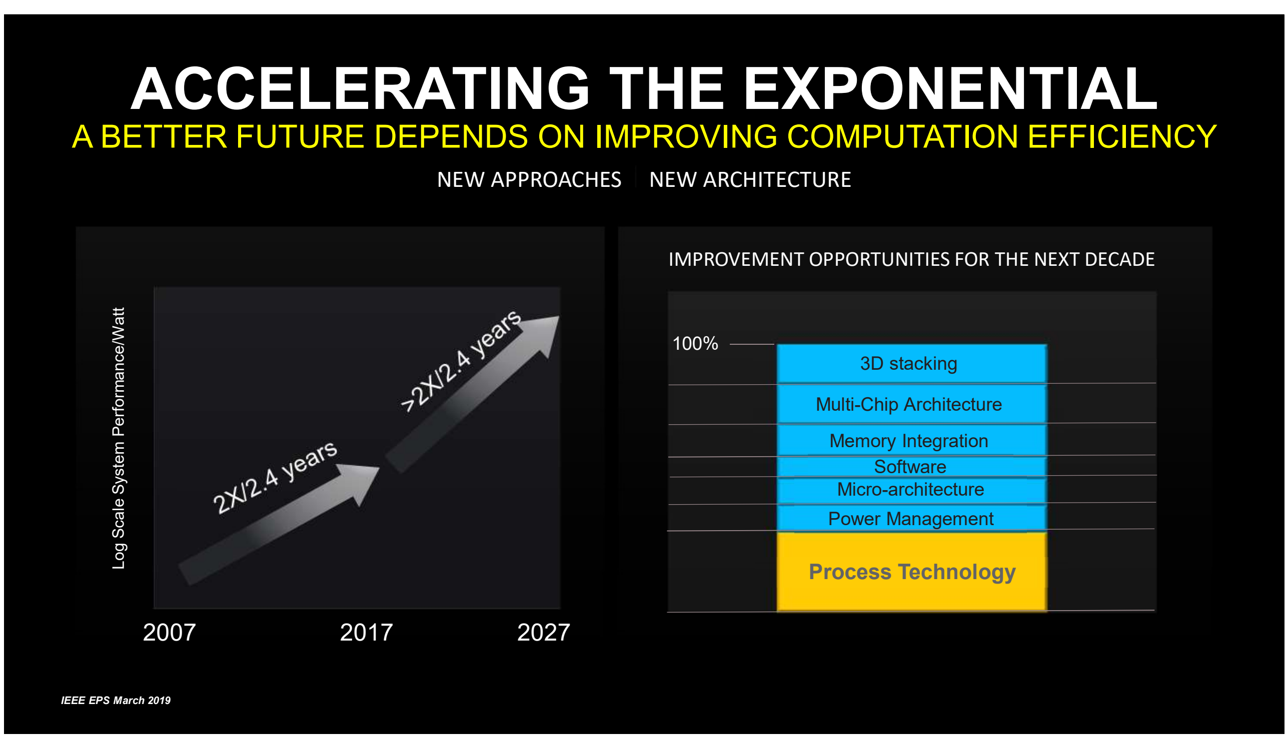


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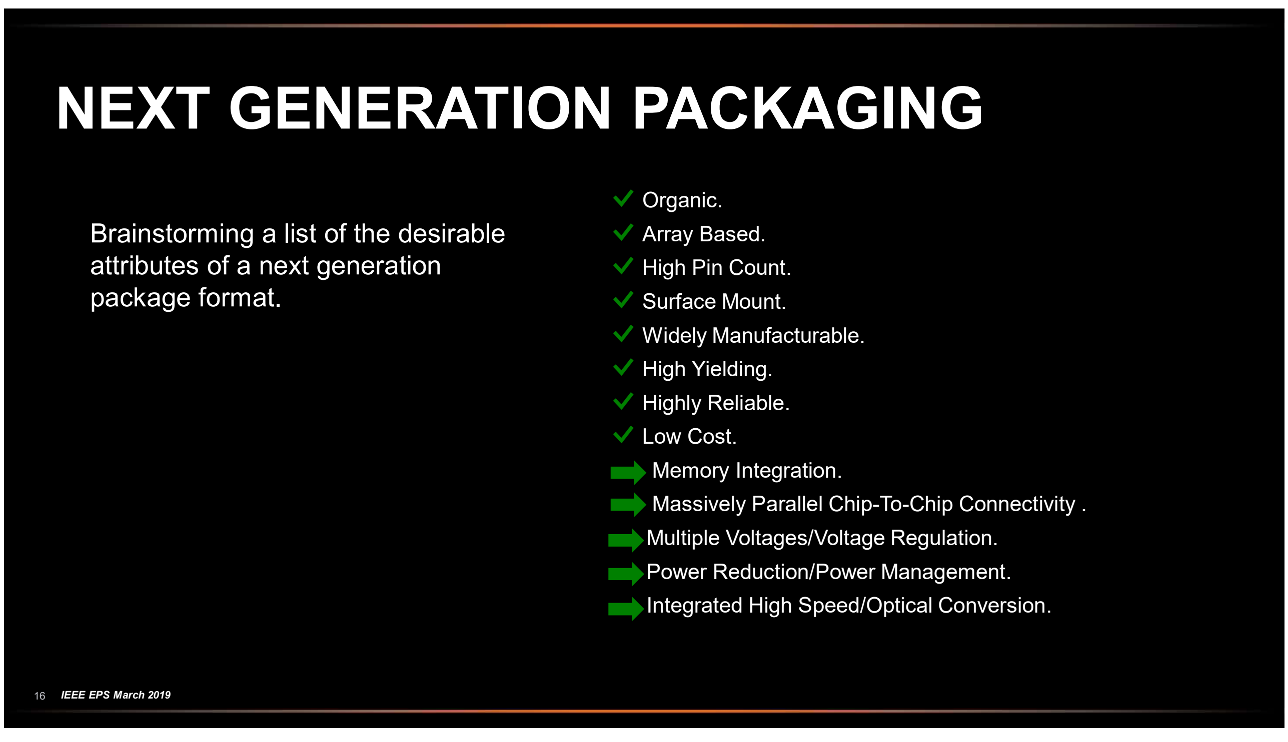


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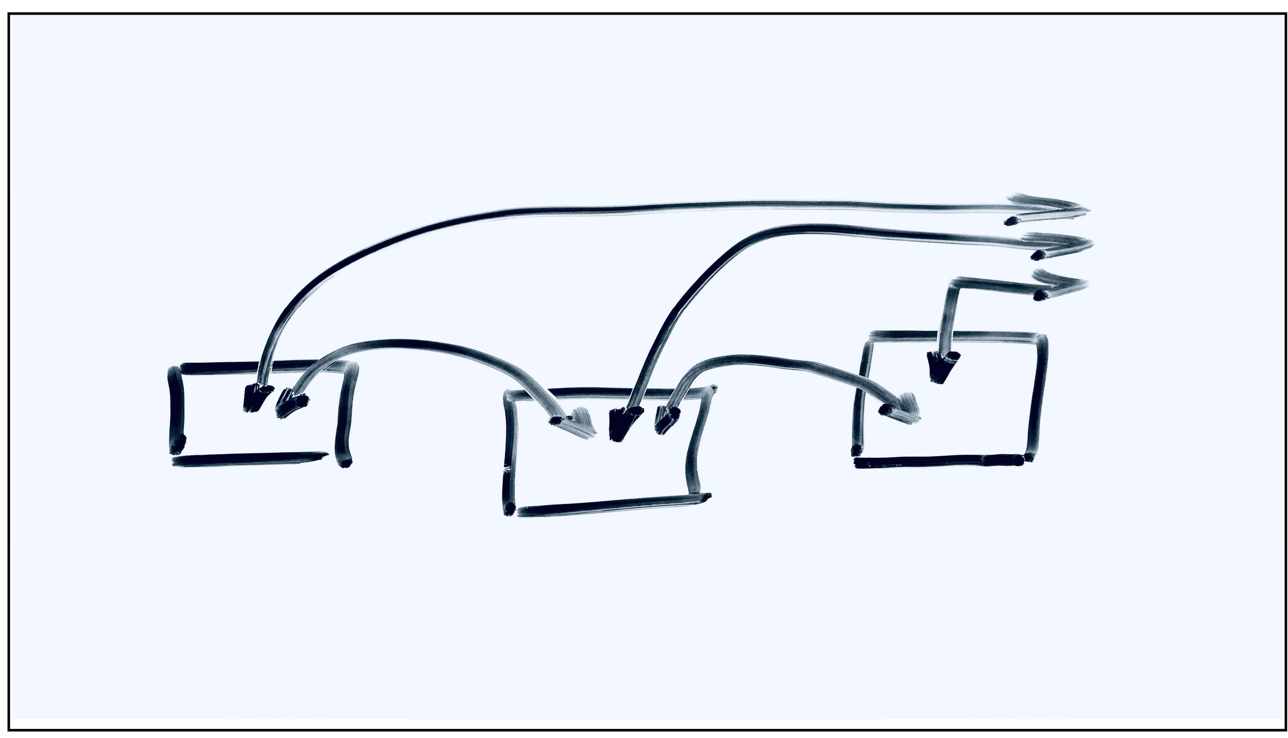

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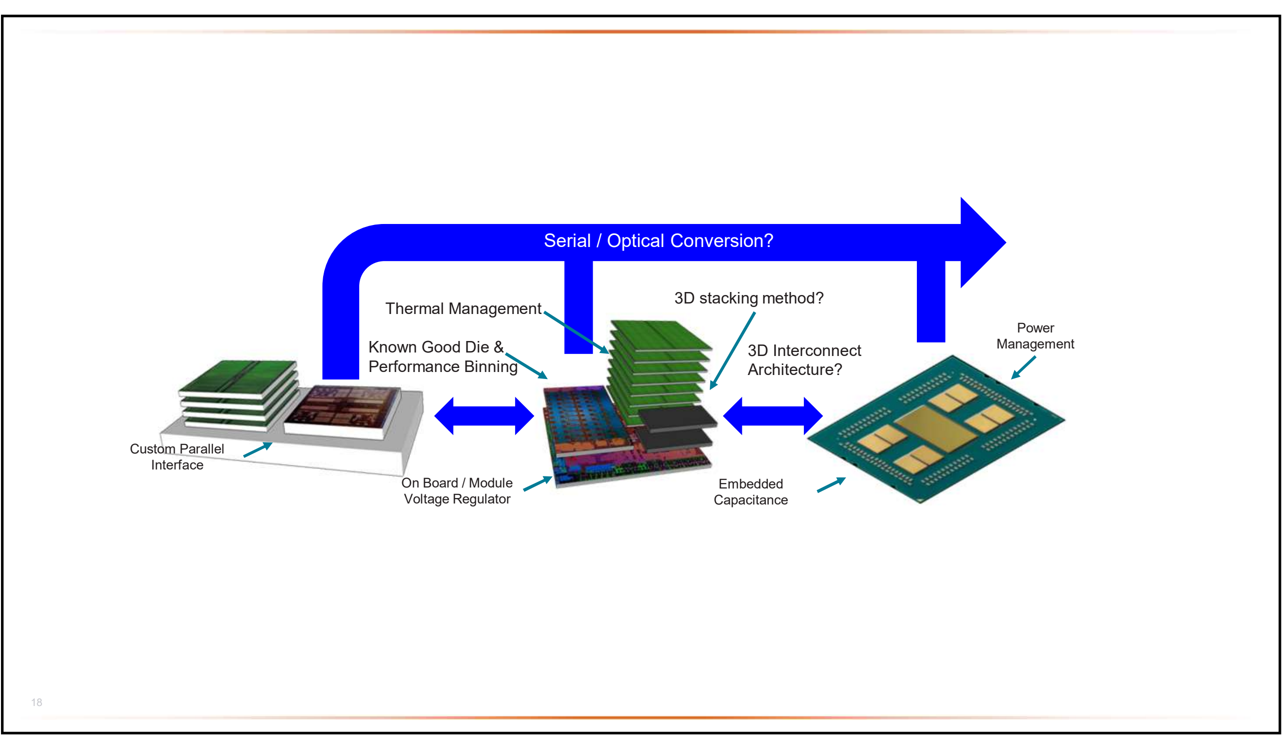


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# THANK YOU

# END NOTES

- Slide 14, 15 Lisa T. Su, Samuel Naffziger, and Mark Papermaster, “Multi-Chip Technologies to Unleash Computing Performance Gains over the Next Decade,” IEDM Conference 2017”.