



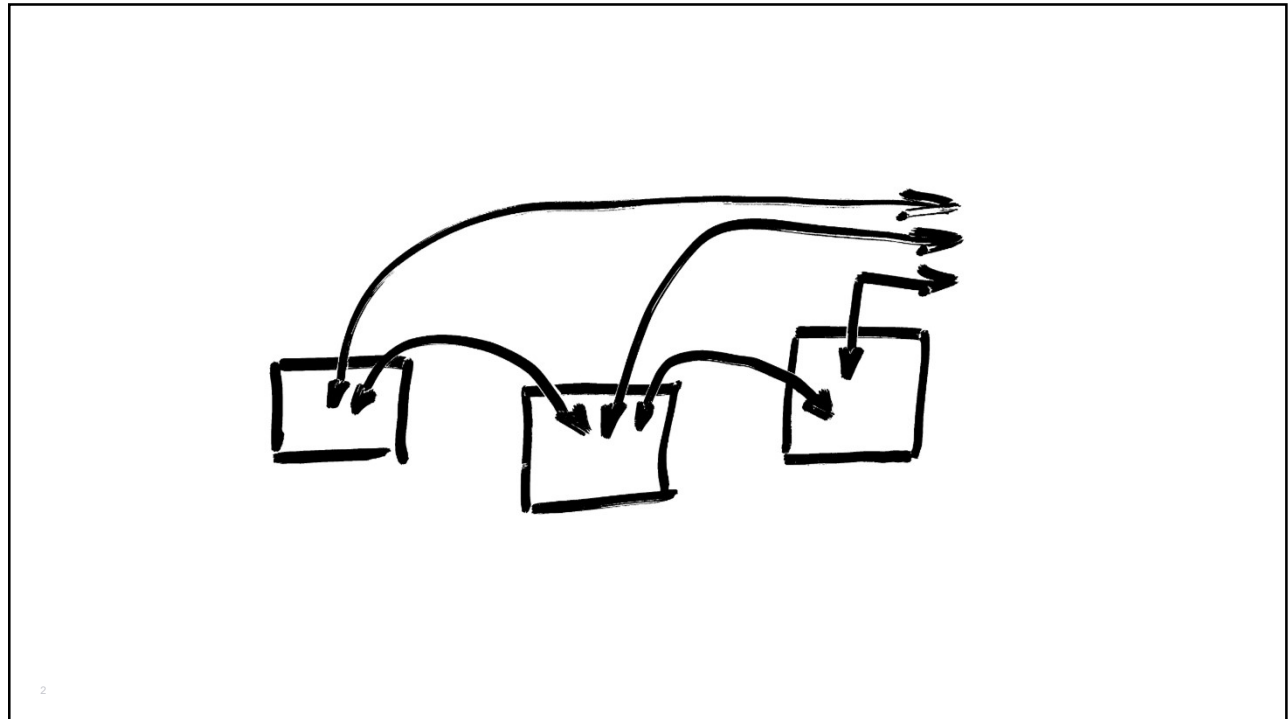
AMD

VISUALIZING THE PACKAGING ROADMAP

IVOR BARBER
CORPORATE VICE PRESIDENT, PACKAGING
AMD

IEEE EPS Luncheon Presentation March 2019

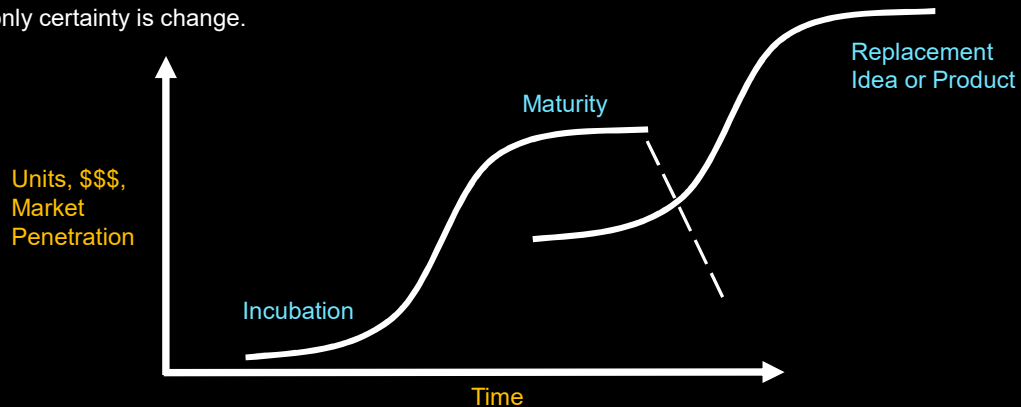
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THE CHALLENGE OF VISUALIZING WHAT LIES AHEAD

- The world is in a period of rapid change, the rate of change is accelerating.
- The field of electronics is facilitating, perhaps driving much of this change.
- The only certainty is change.



Gabriel Tarde's diffusion model or S-Curve can be applied to the spread of ideas, innovations and products from Incubation to Maturity and Decline as Replacements emerge.

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DISRUPTIVE CHANGE CAN HAPPEN QUICKLY



1900

Easter parade in 5th Avenue, New York, in 1900
U.S. Bureau of Public Roads. Photographer unknown. - National Archives and Records Administration, Records of the Bureau of Public Roads. Image 30-N

December 1, 1913

The Ford Motor Company introduced the first moving automobile assembly line, reducing chassis assembly time from 12 1/2 hours in October to 2 hours, 40 minutes.



1913

Library of Congress : George Grantham Bain Collection

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NEXT GENERATION PACKAGING (1990'S)

Brainstorming a list of the desirable attributes of a next generation package format.

- Organic
- Array Based
- High Pin Count
- Surface Mount
- Highly Manufacturable
- High Yielding
- Highly Reliable
- Low Cost

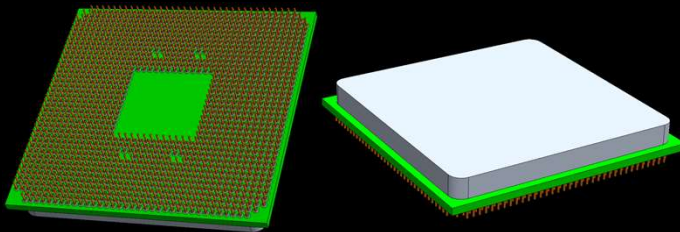
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5

NEXT GENERATION PACKAGING (1990'S)

Brainstorming a list of the desirable attributes of a next generation package format.

Organic, Fine Pitch, Surface Mount Pin Grid Array.



- ✓ Organic.
- ✓ Array Based.
- ✓ High Pin Count.
- ✓ Surface Mount.
- ✗ Widely Manufacturable.
- ✗ High Yielding.
- ✓ Highly Reliable.
- ✗ Low Cost.

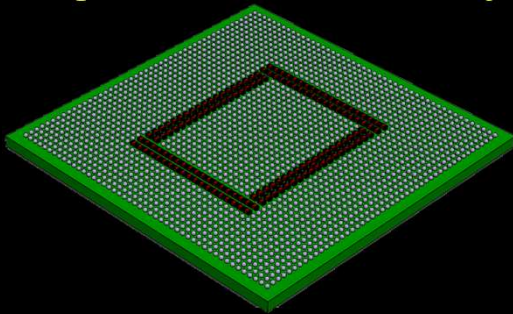
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NEXT GENERATION PACKAGING (1990'S)

Brainstorming a list of the desirable attributes of a next generation package format.

Organic Ball Grid Array.



- ✓ Organic.
- ✓ Array Based.
- ✓ High Pin Count.
- ✓ Surface Mount.
- ✓ Widely Manufacturable.
- ✓ High Yielding.
- ✓ Highly Reliable.
- ✓ Low Cost.

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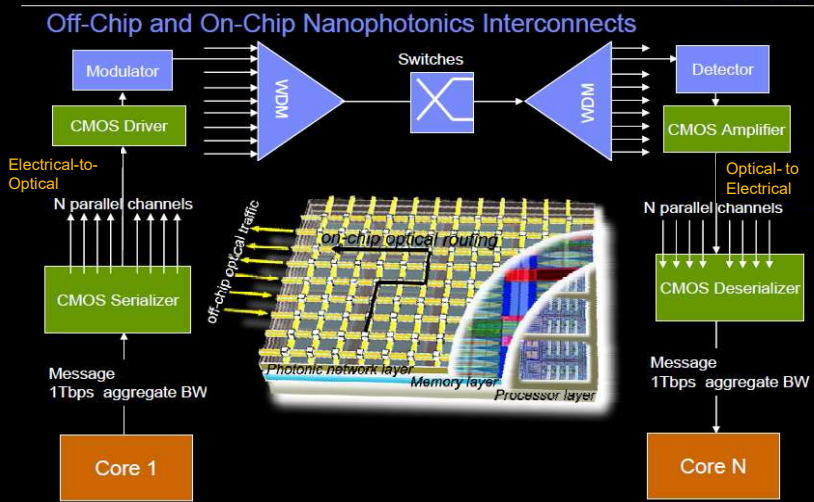
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IBM EXASCALE ROADMAP



In 2010 - to meet the needs of Exascale Computing, IBM predicted several packaging innovations including Nanophotonic interfaces.

Invited talk at SEMICON, Japan, December 1st 2010 .



Goal: Integrate Ultra-dense Nanophotonics Circuits with CMOS chip

<http://www.research.ibm.com/photonics>

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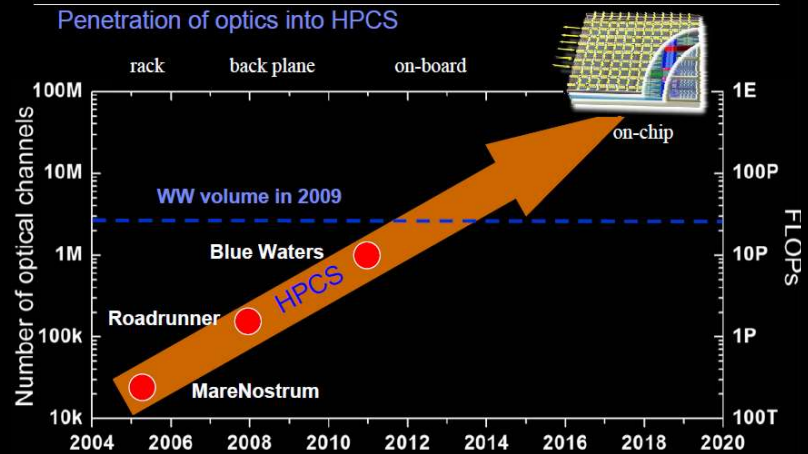
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IBM EXASCALE ROADMAP

In 2010 - to meet the needs of Exascale Computing, IBM predicted several packaging innovations including Nanophotonic interfaces.

Invited talk at SEMICON, Japan, December 1st 2010.



Single HPC machine will contain a similar number of optical channels as currently exist today in all parallel optical links worldwide

<http://www.research.ibm.com/photronics>

Courtesy of M. Taubenblatt

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THE EMERGENCE OF MULTI-DIE PACKAGING

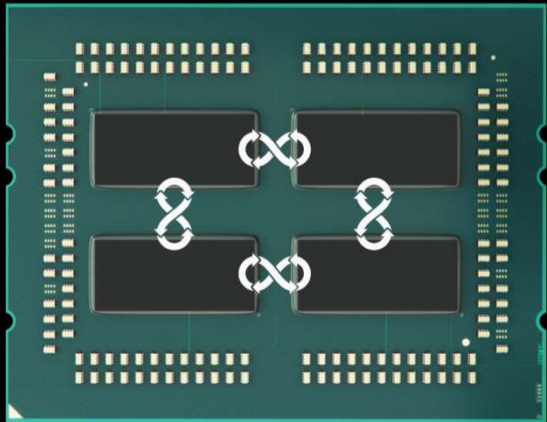
- The slowing of Moore's Law as an economic driver has led to renewed interest in multi-die packaging.
- Traditional SOC scaling has hit cost barriers which make die partitioning economically viable for high end packaging.
 - Xilinx used silicon interposers with TSV (2.5D).
- Traditional SOC scaling has fundamental barriers which prohibit monolithic integration of analog, logic and memory circuits.
 - Multi-die packaging will replace both Moore's Law and SOC scaling as the economic and technological driving force of the Semiconductor Industry.

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Attribution : Bill Bottoms, Various HIR Roadmap Presentations

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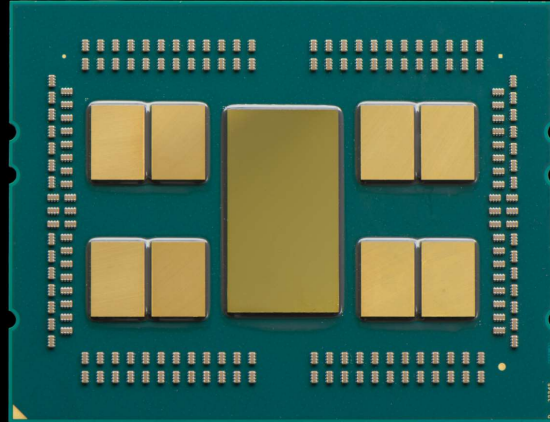
MULTI-CHIP PACKAGING FOR SERVER APPLICATIONS



1st Generation - 32 cores
Homogeneous Integration



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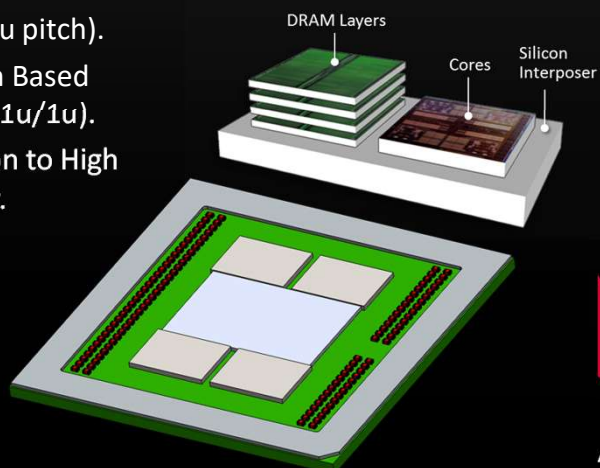
2nd Generation - 64 cores
Heterogenous Integration



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2.5D ALLOWS HIGH BANDWIDTH MEMORY INTERCONNECT

- Fine pitch bumping (45u/55u pitch).
- Fine line routing with Silicon Based geometries on interposer (<math><1\mu/1\mu</math>).
- Massively Parallel connection to High Band Width (HBM) Memory.



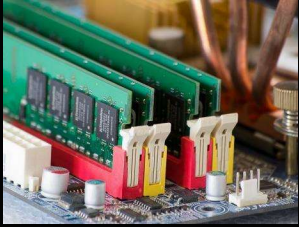
GPU Logic + HBM

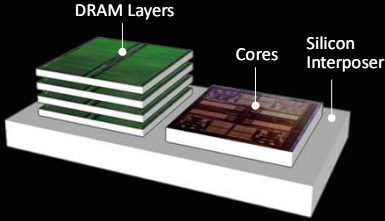


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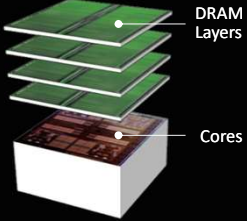
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HIGHER BANDWIDTH AT LOWER POWER





DRAM Layers
Cores
Silicon Interposer



DRAM Layers
Cores

INTEGRATION ENABLES HIGHER BANDWIDTH AT LOWER POWER ➔

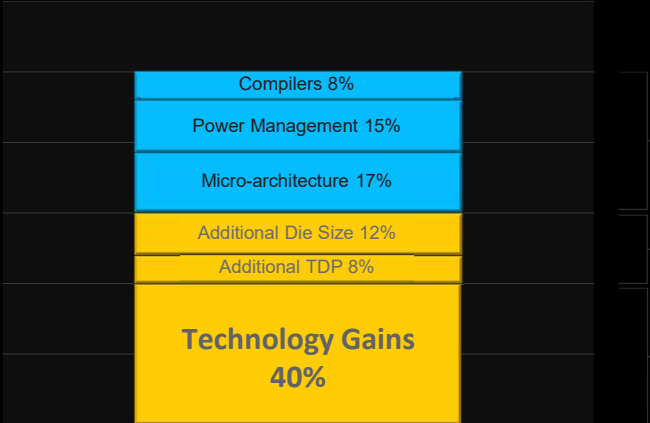
	DIMMs	2.5D	3D
pJ/bit	~8	~3.5	<1
BW	50-200GB/s	250-1000GB/s	>1TB/s

IEEE EPS March 2019 AMD internal modeling and estimates

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PERFORMANCE GAINS OVER THE PAST DECADE

ELEMENTS OF 2X IN 2.4 YEAR PERFORMANCE GAIN OVER THE PAST DECADE



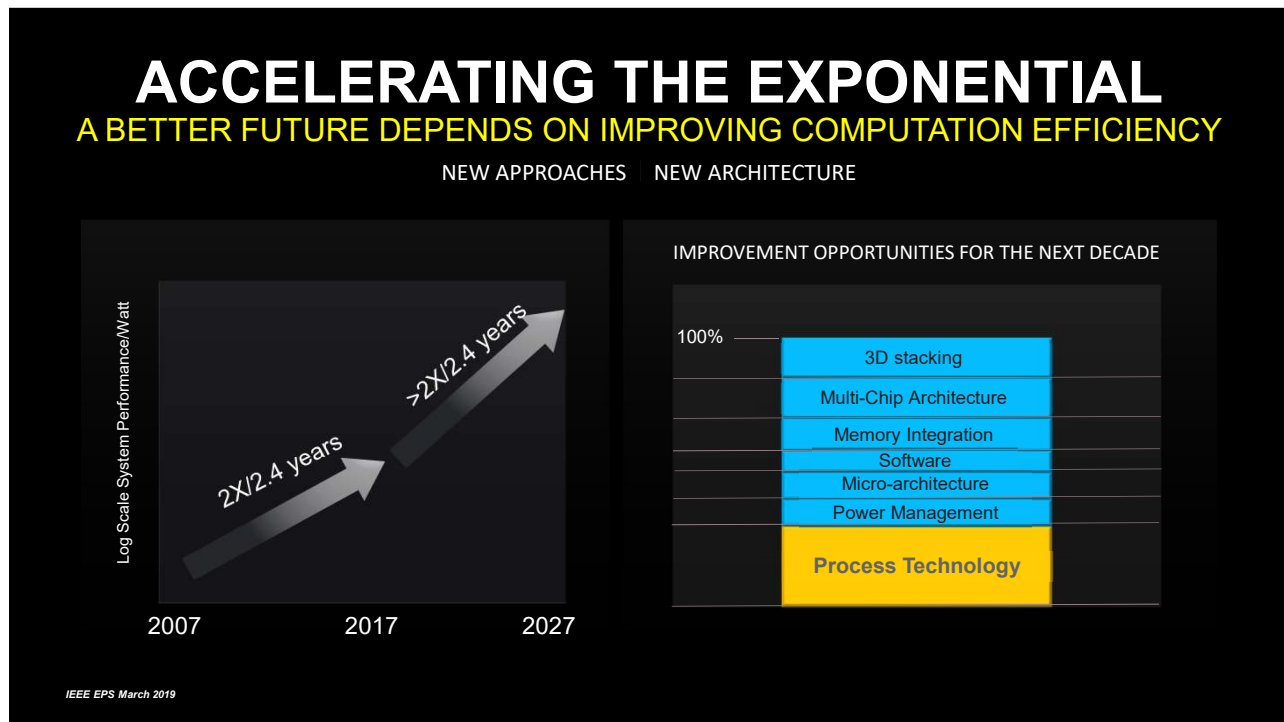
- Integration of System Components.
- Micro-architectural Efficiency.
- Power Management.
- Software.

- More Silicon Power.
- Bigger Die.

HIGHER PERFORMANCE,
DENSER, LOWER POWER
TRANSISTORS.

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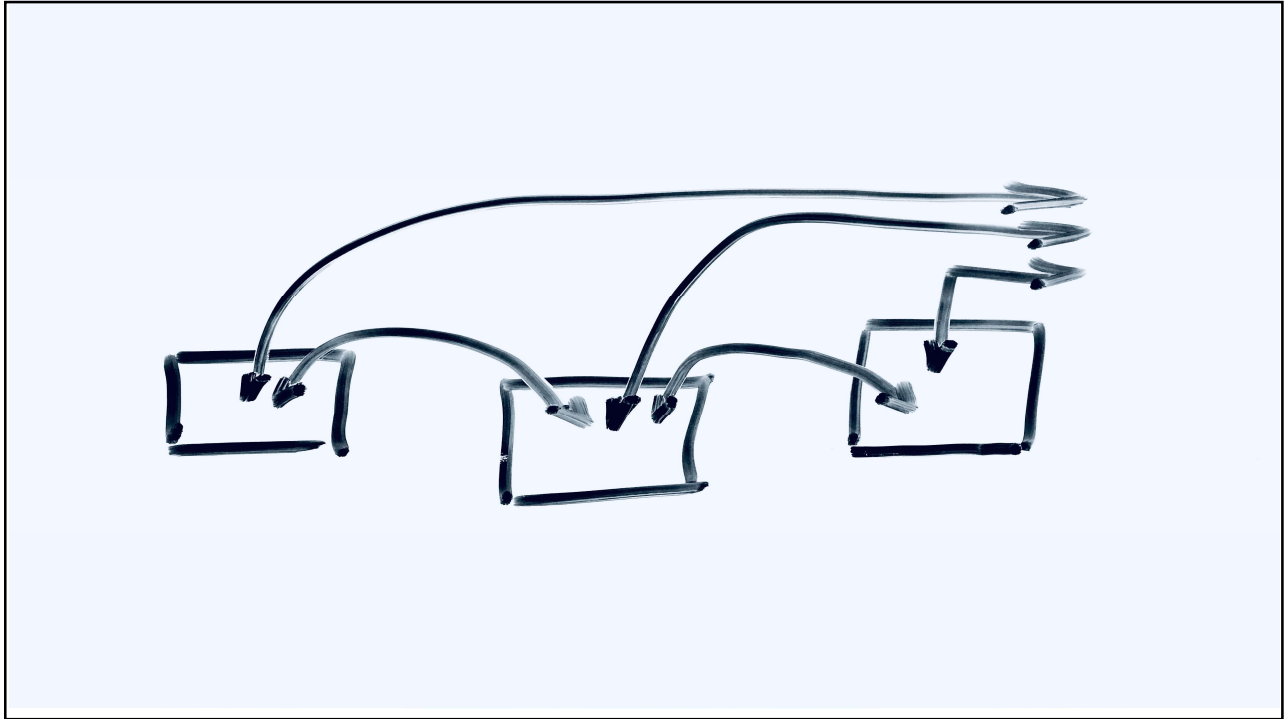
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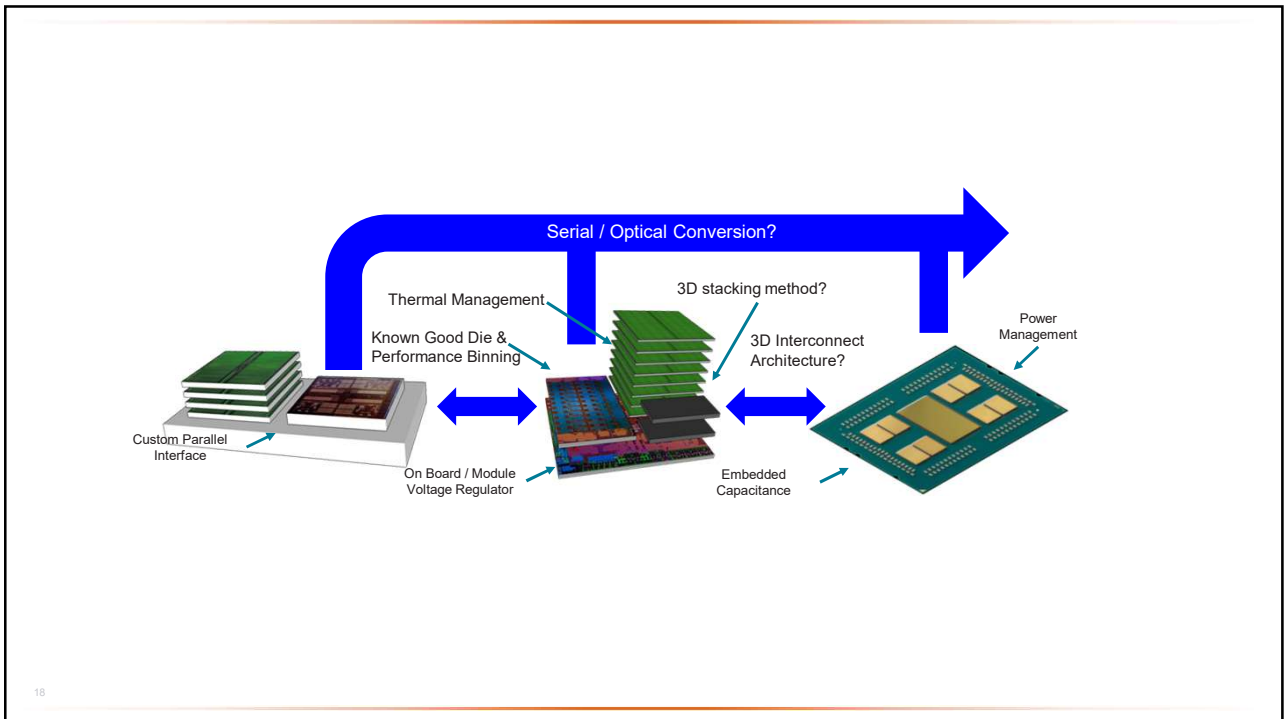
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THANK YOU



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END NOTES

- Slide 14, 15 Lisa T. Su, Samuel Naffziger, and Mark Papermaster, "Multi-Chip Technologies to Unleash Computing Performance Gains over the Next Decade," IEDM Conference 2017".

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