MEPTEC Report

FALL 2018

A Quarterly Publication of The Microelectronics Packaging & Test Engineering Council

Volume 22, Number 3

MEPTEC 2018

HETEROGENEOUS INTEGRATION: THE PATH FORWARD

REALIZING THE COST AND PERFORMANCE BENEFITS

Monday, December 5, 2018 - San Jose, CA

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Wirebonding Variables: How Much Can the Design and Process Engineers Control?

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Amtech was established in 1993 by a core team of Silicon Valley professionals. The team's roots coming from the design, engineering and manufacturing of emerging technologies including Thick-Film Hybrid Microelectronics, Chip-On-Board and Chip-On-Flex. These technologies were used to create products incorporating Micro-SMT, Die Attach, Wire Bond, Lid Seal and Encapsulation processes.

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INSIDE THIS ISSUE

Amkor Technology®

50 FIFTY YEARS

1968 - 2018

A proud legacy. An exciting future.

As the original pioneers of the OSAT industry, Amkor has helped define and advance the technology manufacturing landscape. Since 1968, we've delivered innovative packaging solutions with the service and capacity global customers rely on.

We're proud of what we've done, and can't wait to show you what's next.

www.amkor.com

MEPTEC
THE NEXT GENERATION

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ON THE COVER

MEPTEC continues to cover leading-edge topics in semiconductor packaging with its Fall 2018 Symposium "*Heterogeneous Integration: The Path Forward.*" Industry leaders will present the latest updates on technical and business issues related to integration of different types of semiconductor devices. This field has been identified as the next critical area for the semiconductor industry to continue to advance, as progress via Moore's Law scaling becomes increasingly cost-prohibitive or prevented by insurmountable technical challenges.

INTEL ACQUIRES NETSPEED SYSTEMS FOR CHIP DESIGN

Intel has announced the acquisition of **NetSpeed Systems**, a San Jose, California-based provider of system-on-chip (SoC) design tools and interconnect fabric intellectual property (IP). Deal terms were not disclosed. NetSpeed's highly configurable and synthesizable offerings will help Intel more quickly and cost-effectively design, develop and test new SoCs with an ever-increasing set of IP. The NetSpeed team is joining Intel's Silicon Engineering Group (SEG) led by Jim Keller. NetSpeed co-founder and CEO, Sundari Mitra, will continue to lead her team as an Intel vice president reporting to Keller.

www.intel.com

DYCONEX INTRODUCES AUTOMATED FINAL INSPECTIONS

DYCONEX AG, an MST company and the world's leading supplier of ultra-complex printed circuit board solutions, now offers customers automated final inspections to further optimize testing of their printed circuit boards.

Thorough and readily reproducible testing of printed circuit boards is the goal of the automated final inspection newly introduced by DYCONEX. This gives companies the option of having their products tested by a scanner system – swiftly and with constant comparability and repeat accuracy, in a process that supplements final inspection by qualified DYCONEX employees.

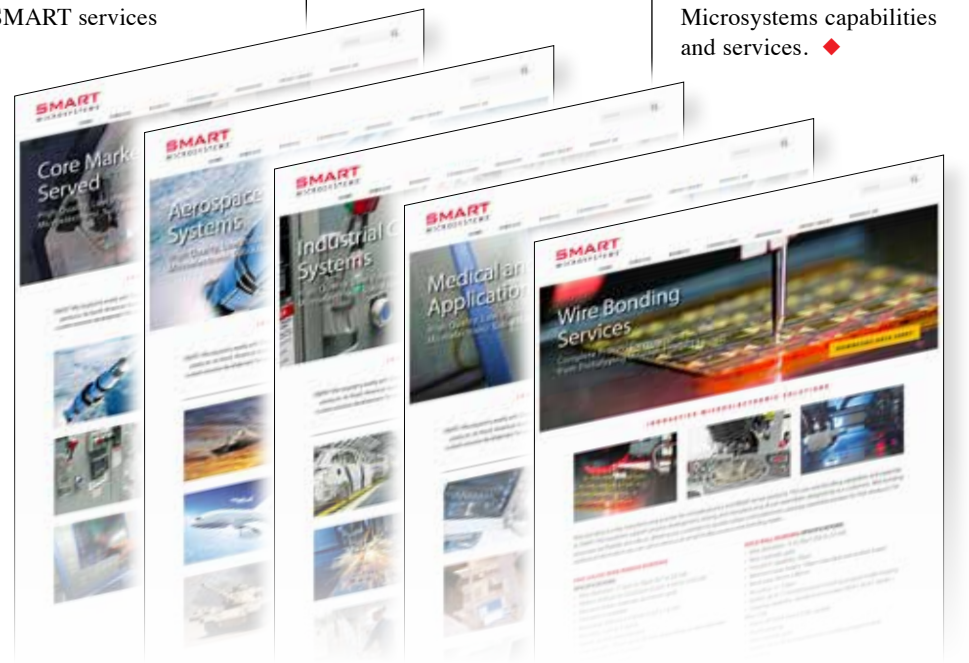
www.mst.com/dyconex

SMART Microsystems Launches New Website

North America's leading full-service microelectronic assembly supplier works with Design Engineers to provide high-quality, low volume microelectronic sub-assemblies

BUILT WITH DESIGN Engineers in mind, SMART Microsystems' new website provides comprehensive technical information for all SMART services and capabilities, as well as providing easy communication links to SMART's engineers and technical resources.

Visit the new SMART Microsystems website at www.smartmicrosystems.com or call 440-366-4203 for more about SMART Microsystems capabilities and services. ◆



Samtec Introduces New Flyover™ QSFP28 Cable System

SAMTEC PROUDLY ANNOUNCES THE release of the new Flyover™ QSFP28 Cable System. This system allows sideband signaling via press-fit contacts to improve airflow, reduce loss, and mitigate skew. The FQSFP series offers features including:

- 28G NRZ/56G PAM4 data rates per channel
- 3.5 W heat dissipation
- Aggregate data rates of 100 Gbps NRZ/200 Gbps PAM4
- Compatibility with all MSA QSFP pluggables
- A variety of heat sink options
- Multiple End 2 options
- Localized press-fit control and power contacts

The Samtec Flyover™ QSFP28 Cable System consists of the FQSFP assembly, the QSFPC cage, HS-QSFP heat sink, and LP-FQSFP light pipe. The FQSFP offers multiple End 2 options including DCH, ECUE, and ARC6. FQSFP utilizes 30 & 34 AWG 100 Ω Eye Speed® Ultra

Low Skew Twinax Cable.

Using the FQSFP series allows for a much longer electrical trace and convenient selection for the endpoint of the SerDes termination. The process of routing through the FQFSP series allows designers to locate the QSFP interface much further from the ASIC or processor than traditional PCB routing would allow. This also removes the need for expensive retimers or power hungry drivers and receivers.

For more information visit the Flyover™ QSFP28 Cable System landing page or download the Flyover QSFP Application Design Guide at www.samtec.com. ◆

Nordson SONOSCAN Unveils Gen7™ Tool on Windows® 10

NORDSON SONOSCAN, a leader in the development and production of acoustic micro imaging (AMI) tools, announces its new Gen7™ laboratory style acoustic micro-imaging tool. The new Gen7 AMI tool enhances operator productivity and part throughput rate by providing greater versatility in transducer movement, faster scanning of samples, and faster processing of data.

Orders are now being taken for the Gen7 AMI tool, which, like its predecessors in the Nordson SONOSCAN C-SAM® line, is designed for analytical work on small numbers of samples, although it can also screen modest quantities of components. Among its differentiating features:

- 50% higher screening throughput from faster transducer motors.
- Scan area significantly enlarged, so more parts can be scanned at one time.
- Upward and downward range of Z movement of the transducer more than doubled to enable scanning of samples having a greater range of height variation.
- Windows® 10 operating system and Sonolytics 2™ user interface have replaced Windows® 7 and Sonolytics™, respectively.
- Intel's i7 seventh generation chips make the system's computer hardware 33% faster, giving, for example, quicker delivery of Digital Image Analysis.
- Both monitors have high resolution 4K screens to reveal more detail.
- Includes Waterplume™ technology, so a separate C-SAM tool is not needed to image IGBT modules.

For more information about Nordson SONOSCAN visit www.nordsonsonoscan.com or call 847-437-6400. ◆

SEMI Integration of ESD Alliance Underway

SEMI HAS ANNOUNCED THAT ALL LEGAL requirements have been met for the ESD (Electronic Systems Design) Alliance to become a SEMI Strategic Association Partner. Full integration of the Redwood City, California-based association representing the semiconductor design ecosystem is expected to be complete by the end of 2018. The integration will extend ESD Alliance's global reach in the electronics manufacturing supply chain and strengthen engagement and collaboration between the semiconductor design and manufacturing communities worldwide. As a SEMI Strategic Association Partner, the ESD Alliance will retain its own governance and continue its mission to represent and support companies in the semiconductor design ecosystem.

The ESD Alliance will lead its strategic goals and objectives as part of SEMI, leveraging SEMI's robust global resources including seven regional offices, expositions and conferences, technology communities and activities in areas such as advocacy, international standards, environment, health and safety (EH&S) and market statistics.

With the integration, SEMI adds the design segment to its electronics manufacturing supply chain scope, connecting the full ecosystem. The integration is a key step in streamlining SEMI members' collaboration and connection with the electronic system design, IP and fabless communities. The Strategic Association Partnership will also enhance collaboration and innovation across the collective SEMI membership as ESD Alliance members bring key capabilities to SEMI's vertical application platforms such as Smart Transportation, Smart Manufacturing and Smart Data as well as applications including AI and Machine Learning.

All ESD Alliance member companies, including global leaders ARM, Cadence, Mentor, a Siemens business, and Synopsys, will join SEMI's global membership of more than 2,000 companies while retaining ESD Alliance's distinct self-governed community within SEMI. Follow the ESD Alliance at esd-alliance.org. ◆

ULTRATAPE EXPANDS ITS LINE OF SECURITY AND TAMPER EVIDENT ADHESIVE TAPE AND LABEL PRODUCTS

UltraTape has recently expanded its tamper evident tape and label offering. UltraTape's tamper evident tape and label products are ideal for authentication, theft reduction and protection against counterfeiting and piracy. These self-voiding products, commonly used for healthcare/pharmaceutical applications, are available in a variety of adhesive/backing combinations as well as colors. They can be made with a special "void" or "opened" message that appears upon removal or can be customized with additional features specific to a customer's authentication program. *www.cleanroomtape.com*

MEXICO'S HIGHEST ENVIRONMENTAL AWARD GIVEN TO KYOCERA

Kyocera has been awarded Mexico's highest honor for environmental protection — the national "*Recognition of Environmental Excellence*" award — for the third consecutive year. Presented by Mexico's Federal Environmental Protection Agency (PROFEPA), the award recognizes state-of-the-art environmental compliance practices at Kyocera's manufacturing facilities in Tijuana, Baja California, especially the reduction of energy and water consumption. Kyocera was one of 58 companies in Mexico to receive the "Excellence" award, and one of just seven to receive the award for three consecutive years. *www.kyocera.com*

F & K DELVOTEC RECEIVES RESEARCH SEAL "INNOVATIVE THROUGH RESEARCH"

There are 3.5 million companies in Germany, less than one percent of them research – a extremely important group. Because only those who do research can discover new things and innovations and create growth. The "*Stifterverband für die Deutsche Wissenschaft*" (Donors' Association for the Promotion of Sciences and Humanities in Germany), founded in 1920, regularly awards a special seal of approval to creative companies engaged in research in recognition of their special research efforts. Since 2016, **F&K DELVOTEC** has also belonged to this circle of award-winning companies. With the "*Innovative through Research*" seal, the Stifterverband acknowledges the special responsibility that the company assumes for the state and society. *www.fkdelvotec.com/en/*

STANFORD NANOFABRICATION FACILITY PARTNERS WITH FINETECH

Finetech is pleased to have recently formed a partnership with the Stanford Nanofabrication Facility (SNF) located in the newly opened Paul G. Allen Building in Stanford, California.

The FINEPLACER® Lambda, a flexible submicron die bonder for precision die attach and chip packaging, is an integral part of the SNF lab's equipment capabilities. This collaboration enhances the support and availability of Finetech's technical knowhow, thereby enabling

Amkor Delivers Industry's First Package Assembly Design Kit to Support Mentor's High-Density Advanced Packaging Tools

Amkor SmartPackage™ Speeds Accurate Design and Verification of Heterogeneous Integration Package Solutions

AMKOR TECHNOLOGY, Inc. has announced it has partnered with Mentor to release Amkor's SmartPackage™ Package Assembly Design Kit (PADK), the first in the industry to support Mentor's High-Density Advanced Packaging (HDAP) design process and tools. Amkor's award-winning High-Density Fan Out (HDFO) process can now be used in conjunction with Mentor's software to deliver early, rapid and accurate verification results of advanced packages required for Internet-of-Things, automotive, high-speed communications, computing and artificial intelligence applications.

The complex and compact design of devices for today's smart applications is driving the need for sophisticated packaging techniques such as heterogeneous integration and Advanced System-in-Package. These solutions combine one or more ICs of different functionality with increased I/O and circuit density in 2.5D (side-by-side) and 3D constructions. With Amkor's SmartPackage PADK and Mentor's proven HDAP tool flow, mutual customers of Amkor and Mentor have the ability to create and review multiple assemblies and LVS (layout vs. schematic), connectivity, geometry and component spacing scenarios using Amkor's HDFO process. The graphic environment features robust data and is straightforward to use before and during the implementation of physical design, resulting in faster sign-off and fewer verification cycles.

"Amkor was the first OSAT company to join the Mentor OSAT Alliance program, and now the first to build and make available a PADK for its customers," said AJ Incorvaia, vice president and general manager of Mentor's BSD division.

The OSAT Alliance program helps promote the adoption, implementation and growth of HDAP throughout the semiconductor ecosystem and design chain, enabling system and fabless semiconductor companies to have a friction-free path for emerging packaging technologies.

For more information visit www.amkor.com. ◆

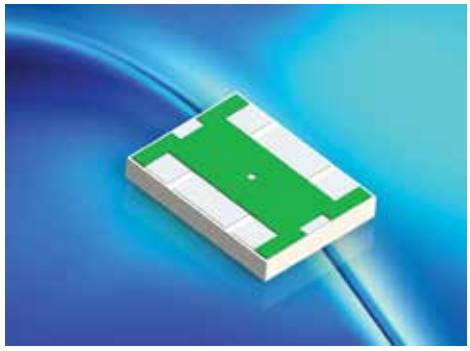
Barry Industries Introduces DC-40GHz Chip Attenuators with 1.26:1 Max VSWR for Broadband Applications

BARRY INDUSTRIES ANNOUNCES THE introduction of AS1209BA-XXXXFN-YY broadband, DC to 40GHz chip attenuators. The AS1209BA-XXXXFN-YY has 22.5dB or better return loss to 30GHz and 18.5dB to 40GHz.

Barry Industries is an ISO9001:2015 certified, ITAR registered manufacturer of high quality thick film attenuators, resistors, terminations and high temperature co-fired ceramic (HTCC) packaging.

The AS1209BA-XXXXFN-YY is a compact, 1209 (3.05 x 2.29mm) size SMT 'flip-chip' and is constructed of robust thick film with solderable terminals. This 50 ohm impedance device is available in 0dB to 10dB nominal attenuation in half dB increments. Attenuation tolerance is less than 0.75dB over a 40GHz range. It is RoHS/ REACH compliant and is rated at 500mW on a 100°C mounting surface temperature.

With its broadband performance, stable thick film design and 1.26:1 Max. VSWR over a DC-40GHz range, the AS1209BA-XXXXFN-YY is ideal for applications operating within the proposed 5G bands.

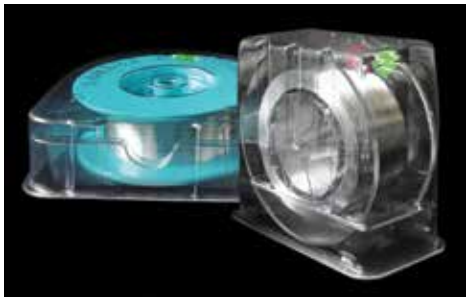


The AS1209BA-XXXXFN-YY is available in bulk or tape and reel packaging for high speed pick and place assembly.

Since 1977, Barry Industries has been supplying the defense, medical and communications industries with highest quality thick film chip resistors, terminations, attenuators high temperature co-fired ceramic (HTCC) packaging. For more about the AS1209BA-XXXXFN-YY, the product data sheet, and sample inquiry form, please visit www.barryind.com or call 508-226-3350, e-mail: sales@barryind.com. ◆

TANAKA Announces New Packaging for Storing Power Bonding Wire

TANAKA Precious Metals announces invention of new packaging to increase the storage life of Power Bonding Wire



TO PROLONG SHELF LIFE AND MINIMIZE handling issues, it is generally recommended to store spools of heavy gauge bonding wire in the upright position. Storing spools vertically, with the hub parallel to the shelf, reduces the potential for wire entanglement during de-reeling. However, old-style spools are susceptible to accidentally lying flat with the hub perpendicular to the shelf. Prolonged disorientation during storage with the windings oriented in the non-optimal position may increase the likelihood of wire entanglement. TANAKA's new type No.88K and No.120K spools solve this problem by automatically orienting the windings in the optimal position during storage without the chance of disorientation caused by operator misplacement. The new spool design virtually eliminates accidentally falling over during storage on the shelf.

TANAKA's new proprietary spool design is a superior storage vessel for TANW power aluminum wire, as well as for TANAKA CP-1 power copper wire. Heavy gauge bonding wire is typically used in the manufacture of power semiconductor packages as well as for welding of batteries and a host of applications found in the automotive industry.

TANAKA's new see-through No. 88K and No. 120K spools are 100% clear, allowing full viewing of the wire without obstruction. Tanaka offers heavy gauge wires in diameters of 100um (4-mils) up to 600um (24-mils). On average, 100 to 1000 meters of heavy gauge wire can be stored on TANAKA's No. 88K spool.

TANAKA TANW power aluminum wire and type CP-1 power copper bonding wire are stocked in North America by TopLine through a distribution agreement with TANAKA.

To learn more, please visit www.tanakawire.com or call 800-776-9888.

TopLine manufactures a wide range of daisy chain semiconductor packages for process development, experimentation, machine evaluation, solder training, and SMT assembly practice. TopLine products provide hands-on learning for engineers. Contact TopLine Corporation, Tel (800) 776-9888; Email: info@TopLine.tv.

Founded in 1885, the **TANAKA Precious Metals** group has grown to be a diversified precious metals leader first in Japan, and now in the rest of the world. Contact TANAKA America, Inc., 235 Vineyard Court, Suite 150, Morgan Hill, CA 95037, Tel 408.778.3217; http://pro.tanaka.co.jp/en, or LinkedIn profile at https://www.linkedin.com/company/tanaka-precious-metals/ ◆

Henkel Builds Global Innovation Center

HENKEL HAS LAID THE CORNER STONE for the new global innovation center of its Adhesive Technologies business at the company's headquarters in Düsseldorf. The company will invest more than 130 million euros to erect a state-of-the-art building. Once completed, the facility will allow more than 350 Henkel experts to develop new technologies and applications for a variety of industries. The building will also serve as a global customer center, where Henkel will present new solutions for adhesives, sealants and functional coatings. The opening of the innovation center is planned for the end of 2020.

Visit www.henkel.com for more. ◆

innovative solutions and strengthening the position of Finetech tools in leading edge research.

SNF is a vibrant research community where users work in areas that cover a wide range of disciplines, such as optics, MEMS, biology, chemistry, as well as the more traditional areas of electronics device fabrication and process characterization/development. Having the bonder in the facility provides Finetech a resource by having access to a highly respected Silicon Valley research nanofabrication lab.

Dr. Usha Raghuram, SNF senior tech staff says, "The addition of this bonder to our lab has filled in a much needed gap for bonding between small substrates, with superior alignment accuracy. The simplicity to configure and use makes the bonder a perfect fit for students looking to further their developments and inventions."
www.finetechusa.com

PALOMAR TECHNOLOGIES ENLARGES ENGINEERING LAB

Palomar Technologies announced it is enlarging its engineering laboratory to meet the increased demands of customers developing advanced photonics solutions, such as LiDAR, 3D sensors, gene sequencing and high power LEDs. The upgraded laboratory will be used to further strengthen Palomar's focus on partnering with customers, giving them insight into, and an opportunity to contribute to, Palomar's technology road map and development of the next generation of systems and assembly solutions.
palomartechnologies.com ◆

COUPLING & CROSSTALK

By Ira Feldman

Electronic coupling is the transfer of energy from one circuit or medium to another. Sometimes it is intentional and sometimes not (crosstalk). I hope that this column, by mixing technology and general observations, is thought-provoking and "couples" with your thinking. Most of the time I will stick to technology but occasional crosstalk diversions may deliver a message closer to home.

Milking It!

I OBSERVED RECENTLY TWO different companies "milking" their businesses for good and for ill. With the proper perspective, consumers can see how well an organization manages and cares for their products – tangible goods and services. Not just in the headline news which may be indicative outliers (airline mistreatment of passengers, anyone?) but in everyday interactions and purchases.

What does milking a business – be it cows or dishwashers - have to do with high technology? Everything when it can be instructive! Looking at "consumer" product management successes and failures, it is important to **remember that "industrial" customers are consumers too.** They consume products on a commercial basis and in personal life. Their experiences and expectations crossover between the consumer and the commercial domains. You would not accept shoddy merchandise at home, so why accept it at work? And If you receive white-glove treatment from vendors at no extra cost in the office, you will seek the same at home. As the bar is raised, any product that falls short will be a disappointment.

Whey to go! Who would have thought a dairy plant would be sexy let alone a destination? Count my family among the million plus annual visitors to the Tillamook Creamery. We once again made the journey enjoying Oregon's coastal scenery with the Tillamook factory being the "anchor" of the day. *Am I nuts? Not only stopping once when my children were eight years old but again with them in high school?* Great scenery, fun factory tour, great cheese, and delicious ice cream. *Tempura battered cheese curds, anyone?* What's not to like? Unless you are lactose intolerant…

Two things really stood out at Tillamook on this recent visit. The first, immediately upon arriving, was their brand-new visitors' center followed by the second which was their production line. Their prior visitor setup, while functional and educational, was vintage 1970s. The newly expanded visitors' center is sleek and modern with museum-quality interactive displays, tasting area, and expanded gift store (no surprise). And the original ice cream stand has been transformed into a comprehensive food court.

> Think an Apple store crossed with a Walt Disney theme park. Or perhaps a BMW showroom for cheese.

Beyond the building architecture itself, what impressed was how well everything – the building and the content - was executed as a marketing exercise. Everything from the pictures on the walls, the videos, the food served, to the gift store items were selected and coordinated to reinforce their brand identity and message. Yes, they emphasize their multi-generational roots and continued ownership by the farmers' families. (Tillamook is a cooperative.) What was truly impressive was how well this message was executed in contrast to the folksy "haphazard" prior version. **Think an Apple store crossed with a Walt Disney theme park. Or perhaps a BMW showroom for cheese.** The level of sophistication is orders of magnitude ahead of other factory tours and visitor centers we have seen. **They clearly take great pride in their products and are not following the herd!**

The second remarkable item was the stark contrast of the actual production equipment to the modern visitor center. They are indeed proud that some of their production equipment (cheese curdling vats in particular) date back to when the plant was built in the 1940s. The entire facility had been designed for continuous operation and to allow cleaning and servicing of equipment "in place".

And though the basic recipe for making cheese has not changed over time, they have continuously improved their processes, updating their production line over the years with automation, new production equipment, and technology. The fact that they have been able to do this in the original building while utilizing sections of their original equipment, demonstrates that **they understood the fundamentals of their processes and business from the start.**

The takeaway from visiting Tillamook? Great cheese and ice cream! But we knew that already… The experience creates a very positive impression about the brand (score one for Marketing!) and their operations. They demonstrate their pride in their business by continuously investing in it. Tillamook has been busy milking cows, not the business!

What is in a name? Mature product organizations have a stage-gate product development process that includes robust design for x (DFx) criteria reviewed at each checkpoint. The "x" stands for a wide range of functional and usage areas including Manufacturing, Assembly, Service, Quality, Reliability, Usability, etc. At each checkpoint the product is reviewed against best practices (from prior products and industry knowledge) and corporate goals to insure robustness of the design in each area.

Design for manufacturing (DFM), for example, examines all aspects of the design to make the product as simple and economical to manufacture as possible. A typical DFM checklist item is the number and types of fasteners. Why have five different types screws – some Phillips and some hex head drive – when these all can be replaced with two types of Torx screws?

Usability and Installation are key areas that should be in any DFx review process. So, it was very surprising to run into multiple issues with the recent installation of a high-end General Electric (GE) dishwasher during our kitchen remodel. GE has a very engineering-centric product development culture with a strong reputation for white goods (home appliances). Expectations were high from the outset and there was noticeable attention to details in many areas of the

design.

The installation went smoothly until the very end when the unit was to be secured to the cabinets with trim. The specifications for this unit say "24 inch minimum" width which matches the standard United States dishwasher cabinet opening of 24" [610 mm]. With the smallest required finish trim installed, the unit is 24.5" [622 mm] wide. Needless to say this caused problems as our cabinets are 24" wide with typical engineering precision.

The next step was no better. The unit is supposed to be anchored on each side using openings in the interior of the dishwasher. The access to these openings are blocked by the top rack of the dishwasher so it was impossible to see the screws let alone reach them with a tool. Simple solution - remove the top rack, right? Nope. In this model, unlike others, the rack is only removable by a "factory technician". After much cursing, the engineers of the household persevered in removing the top rack in order to fasten the unit to the cabinets. And successfully reinstalled the rack to finish the installation.

There is absolutely no way this dishwasher, as configured, passed a reasonable DFx check for installation. Perhaps the designers never bothered to try installing this configuration into a standard 24" wide opening? If so, **their product managers failed by either not identifying the actual use case or insisting an actual check be done.** Or perhaps a change was made to the product configuration without bothering to check again…

Of course there is more to this story. We purchased our GE appliances based on previous experience, brand reputation, and high rankings in *Consumer Reports*. Unbeknownst to us the entire GE white goods business was purchased by Haier in early 2016. Clearly GE lost interest in the business over the years and was "milking it" prior to the sale. **Once their pride of ownership was lost, quality and innovation suffered likely increasing the imperative to sell.** Not only did Haier buy the business **they purchased the name too!** I would argue that both companies should be concerned about product quality – Haier as the manufacturer and seller *and* GE because their name is still on it.

In the end it is all about taking pride in a business and properly setting customer expectations to ensure future success. Anything less leads to customer dissatisfaction. Exceeding expectations separates the winners from the losers!

For more of my thoughts, please see my blog http://hightechbizdev.com.

As always, I look forward to hearing your comments directly. Please contact me to discuss your thoughts or if I can be of any assistance. ◆

IRA FELDMAN is the Principal Consultant of Feldman Engineering Corp. which guides high technology products and services from concept to high volume manufacturing. He engages on a wide range of projects including technical marketing, product-generation processes, supply-chain management, and business development.
(ira@feldmanengineering.com)

INDUSTRY INSIGHTS

By Ron Jones

At the Bottom of It All . . .

IF YOU ASK PEOPLE WHAT THINGS makes life more enjoyable, comfortable, productive, healthy and safe, they might say:

- Myriad electronic gadgets
- Smart phones with an app for everything
- Movies with incredible CGI effects
- Smart appliances and home systems
- Lightning fast internet, e-mail and the web
- Social media and networking
- The world at your fingertip with Goggle
- Diagnostic health tools and DNA analytics
- Cars with more features and increased safety
- ... and on and on.

If you look for a common thread in this list, it is they are all based on technology ... electronic technology to be specific ... semiconductor technology to be even more specific.

I looked at a teardown analysis of the Apple iPhone X and counted 19 IC's, ranging in size from the main processor to smaller controllers and specialty devices. IC's obviously make up a significant percentage of the cost of a phone. Electronic gadgets are typically chock full of IC's.

The semiconductor content in automobiles has been growing for decades and is expected to accelerate with increasing demand focused on self-driving (autonomous) vehicles, vehicle-to-vehicle (V2V) and vehicle-to-infrastructure (V2I) communications, as well as on-board safety, convenience and environmental features. Electric vehicles also have a higher content than fuel versions.

The amount of compute power required for animated films or CGI effects in normal films is astronomical. The rendering of a single frame can take hours of time on a large server farm.

The number of servers that support the World Wide Web is in the range of 100 million, each with processors, logic and memory. It is estimated that Microsoft, Google and AWS each have over a million servers on their networks.

So these gadgets, cars, servers, medical imagers, space shuttles, linear accelerators, et al. are built on semiconductor technology. This raises the question of what technology are semiconductor integrated circuits built upon ... and the answer is the technology of the earth ... atomic elements.

We start with silicon, the third most plentiful element which makes up 15% of our planet's crust. We purify it and it becomes the basis of the wafer that most semiconductors are built upon. We add pinches and dabs of other elements as dopants, e.g. boron, aluminum, gallium, indium, phosphorus, arsenic, antimony, bismuth, lithium and germanium. To make the interconnections on the surface of the wafer, we use aluminum, gold, chromium, germanium, copper, titanium, tungsten, tantalum, nickel, silver and platinum. We make the connections to the various packages with gold, silver and copper. Virtually everything in the finished wafer was added from elemental sources.

There have been process improvements over the years, of course, but we still make the semiconductor wafers using multiple passes of spin, expose, develop, etch, strip, deposit or implant, clean, oxidize ... rinse, repeat.

The semiconductor industry is relatively self-sufficient:

- We build specialized factories for wafer fabrication and testing
- We build specialized factories for package assembly and testing
- We design and make our own unique equipment for wafer processing and metrology
- We design and make our own unique equipment for package assembly
- We write our own software for circuit design and characterization

The transistor was invented in 1947 and the integrated circuit around 1958. By 1968, we were building large volumes of small scale integration (SSI) integrated circuits such as TTL 7400 series logic circuits. These were typically packaged 14 or 16 lead PDIP packages and the average chip had 15 to 20 transistors.

This was not a "one and done" scenario, however, as we continued to make increasingly more complex chips and more complex packaging schemes to house them. Moore's law was hypothesized in 1965 and has been the metronome for the industry for 5 decades. It doesn't matter whether Moore's law merely predicted what would have happened anyway or whether it was a self-fulfilling prophesy that continuously drove us, the outcome is the same. We have experienced constant improvement in cost, size and performance over the past 50 years.

The table below calculates the speed, cost and performance of an automobile had it followed the same trajectory as the integrated circuit over the same time period.

If autos had kept up with processor clock speeds, your average car would have a top speed of 5 million miles per hour ... plan for your next off-ramp accordingly.

continued on page 13

Speed	1968	2018	Impact
Clock Speed	100 kHz	5 GHz	$5x10^4$ frequency
Auto Speed	100 mph	5,000,000 mph	$5x10^4$ speed
Cost			
Transistor cost	$0.01	$5.5 x 10^{-10}	$1/18x10^6$ reduced cost
Auto Cost	$3000/car	6000 cars/dollar	$1/18x10^6$ reduced price
Performance			
MIPS	0.092	1,000,000	$11x10^6$ increase
Auto Mileage	20 mpg	220 million mpg	$11x10^6$ better mileage

MEPTEC2018

HETEROGENEOUS INTEGRATION: THE PATH FORWARD

REALIZING THE COST AND PERFORMANCE BENEFITS

12.5.2018

WEDNESDAY, DEC. 5, 2018 | SEMI GLOBAL HEADQUARTERS | MILPITAS, CA

SYMPOSIUM 8:00AM - 5:00PM | EXHIBITS 9:30AM - 6:30PM | RECEPTION 5:00PM - 6:30PM

KEYNOTE SPEAKER

Heterogeneous Integration Roadmap and SiP

William "Bill" Chen, ASE Fellow and Senior Technical Advisor, ASE Group

KEYNOTE SPEAKER

Disruption is Coming: Adapt, Change or Be Left Behind

Keith Felton, Product Marketing – IC Packaging, Mentor Graphics Board Systems Division

KEYNOTE SPEAKER

Heterogeneous Integration: Is it Ready for Changing the Packaging Landscape?

Risto Puhakken, President, VLSI

MEPTEC continues to cover leading-edge topics in semiconductor packaging with its Fall 2018 Symposium ***"Heterogeneous Integration: The Path Forward."*** Industry leaders will present the latest updates on technical and business issues related to integration of different types of semiconductor devices. This field has been identified as the next critical area for the semiconductor industry to continue to advance, as progress via Moore's Law scaling becomes increasingly cost-prohibitive or prevented by insurmountable technical challenges. With progress in many areas, cost and performance benefits are finally being realized, and previously impossible combinations of devices are now possible.

Don't miss this unique opportunity to get up to speed at MEPTEC's symposium "Heterogeneous Integration: The Path Forward" on December 5, 2018 in Milpitas, CA.

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Game Changers

Mary A. Olsson
Former Chief Analyst, Gary Smith EDA and
Former Vice President of Research, Gartner Dataquest

Drivers, Opportunities and Disruptors

In 2004, as CISCO approached its 20th anniversary, John Chambers announced that CISCO's future investment strategy would address the evolution of networking – Intelligent Information Network. By 2006 Chambers noted that CISCO and the industry were in the midst of a market inflection that would change the total landscape of networking, and become the platform for the next generation technology spend.

By 2010 Korea and Cisco developed a set of SmartCity guidelines. By 2013 Cisco was at the center of major market transitions – cloud, mobility, video – referenced as the Internet of Everything (IoE). By 2018 a new level of competitors/disruptors: Amazon, GE, Google, IBM, Intel, Nvidia, Synopsys and Texas Instruments to name just a few, joined the fray, rolling out compute products for AI and machine learning. By November 2013 Cisco released its Smart+Connected™ City Wi-Fi, an integrated solution that could provide citywide connectivity and establish a platform called the Internet of Things (IoT). After three years and investments of more than $6 billion in R&D, CISCO had acquired 12 more companies to enhance their high growth areas of security, collaborative services, IOT platforms, cloud software and silicon. CISCO management also realized that "no one company could deliver the full breadth of technology solutions" that would be required to build the entire IOT infrastructure".

From 2012 to 2016 consolidation and advancements in process nodes enabled development of complex core designs, driving the need for more high-performance computation, driving the need for solutions to thermal and power management. As noted throughout 2018 MEPTEC publications, the success of these platforms requires integration skills and tools at the package (3D stacked die/ packages, flip chip/ WLP, PoP/SiP/BGA) and PCB levels. Advancements in PCB tools, designs and libraries became key to power/thermal/test and security issues are key in these new platforms.

Overall, 2018 is a key year for Industrial IOT, automotive/autonomous vehicles, deployment of 5nm\3nm EUV, 3G/4G growth and shifts to 5G standards and investment. If Cisco's early forecast of 50 billion devices and machines connected by 2020 comes to fruition, massive investment to support this expanding infrastructure is required. Recent research and review of several companies and industry applications indicate that massive amounts of investments for future cycles (2022 through 2035) are being made in fabrication and foundry, for new system platforms including the following:

New Platforms

- Data analytics (Big Data)
- Industrial IOT
- Machine Learning (M2M)
- 3D Design models
- New memory and Storage products
- Artificial Intelligence
- Robotics/Drones
- Automotive ADAS
- Security/ID/Data Protection of IoT Edge Devices
- 5G standards for high bandwidth
- Optical & NFV (Network function virtualization) networks
- Silicon Photonics
- SOI, III-V, Graphene materials

Short-Term: Changing Landscape and Chaos

First quarter 2018 opened with a great deal of discussion and marketing of IoT roadmaps, testing and field trials of 5G NR (New Radio) standards, high-performance computing, AI in chip developments, business cyber security and cyber security ownership, 3D design and analysis of high-speed signals and signal integrity across PCBs. The strategic impact of new architectures and new technologies looks to radically change today's landscape of semiconductor, EDA and OEM companies.

Texas Instruments quarterlies and 10Ks consistently proved that their decade of strong R&D spending created high growth analog/Mixed signal and embedded product solutions for industrial automation enabled growth in advanced robotic systems. Within the IoT SOC set of devices, significant volumes of analog, mixed signal and sensor circuitry is required. As such one of the leading suppliers like TI will be well positioned for collaboration.

QUALCOMM CDMA Technologies (QCT), the largest provider of 3G/4G chipset and software technology, partners with nearly 60 3G/4G network operators around the globe and has the largest 3G/4G engineering team in the wireless industry. QCT realizes that 5G products are years away. However, QCT is currently building a 5G-software test and verification test team in vendor lab/field tests.

At the PCB level engineers found design time decreased instead of moving faster especially as incredibly complex chip processes, new materials, advanced package designs and board level connectivity advanced from research to reality. Design flow errors, waste and product recalls, re-work and extra prototypes increased and costs exceeded original budgets. The PCB and package design industry is being dragged into power consuming and heterogeneous

applications. Adding layers of complexity requires different layers of integration and increases power supplies and power consumption. The "next generation" of system platforms listed requires new solutions that reduce wiring, coding, time to market, cost and improves efficiency. The acquisition of Mentor Graphics and Solido of Canada, by Siemens, creates a powerful competitor in multiple industries.

After a decade of consolidation within the semiconductor and EDA industries disruptors like financial investors, Google, Quantum AI Lab, IBM Advanced Process Technology Research, Global Foundry, Nvidia, Silicon Catalyst, SkyWater Technology Foundry, and Intel Foundry and Intel Capital will play a strong role in changing the entire landscape of electronics.

As noted by Kailash Narayanan of Keysight EEsof Technologies, IoT is likely to be a significant enabler of many disruptive business models and market efficiencies. Security updates and services will lead to more new products, new business models that will rely on networks of sensors and actuators, linked by radio and connected to the cloud for data analytics. For system reliability even the smallest of components and boards must be designed for stability, security and reliable longevity. As J. Sawicki of Mentor Graphics/Siemens recently stated, introducing new tools in EDA for next generation platforms will take an enormous amount of energy to develop the tool; an enormous amount of energy to get people to start looking at it, and an enormous amount of energy to get your first couple of customers to employ that tool in critical infrastructure systems.

According to the 2016 Industrial Internet Consortium report, an *Industrial Internet of Things* (IIoT) ***system*** connects and integrates industrial control systems with enterprise systems, business processes and analytics. An IIoT system enables significant advances in optimizing decision-making, operations and collaborations among a large number of increasingly autonomous control systems. These systems differ from traditional industrial control systems by being connected extensively to other systems and people, increasing their diversity and scale. They also differ from traditional information technology (IT) systems in that they use sensors and actuators in an industrial environment. These are typically systems that interact with the physical world where uncontrolled change can lead to hazardous conditions. This potential risk increases the importance of safety, reliability, privacy and resiliency beyond the levels expected in many traditional IT environments. Such IIoT systems may also have data flows that include multiple intermediary organizations, requiring security approaches beyond simple approaches such as link encryption. Having long lifetimes, IIoT systems include legacy installations and are regulated because human health and safety is at risk. The cultures of operational and information technology worlds differ, leading to a need to integrate these cultures for IIoT systems. Securing all of these differences will take new methods that will require new system software and hardware. All of this leads to significant investment from all of the players.

Mary Olsson was formerly a Chief Analyst for Gary Smith EDA. Previously she was Vice President of Research with Gartner Dataquest responsible for strategic competitive analysis on emerging process technologies in EDA and semiconductors, fabless and mixed-signal design companies. Before joining Gartner in 1981, Ms. Olsson worked for the Technology Analysis Group of Burroughs. Ms. Olsson holds a Bachelor of Arts degree from San Jose State University. Ms. Olsson has been a speaker on the industry for DQ@DAC, ICCAD, the Chinese American Semiconductor Professional Association, Chinese Institute of Engineers, SEMI Financial Investment Conferences, SAC, ISHM/IEEE, IBM Technology Seminars and is currently a Special Advisor to the Microelectronics Packaging and Test Engineering Council (MEPTEC).

Ms. Olsson has also written several articles and reports on the industry for IEEE, EDN, Semiconductor International, Red Herring, EE Times and MEPTEC. She has been an active volunteer for the Santa Clara Valley Junior Achievement Program, Leukemia Society, and the Bill Wilson Center's Independent Living and Juvenile Hall Training Projects.

Mary can be reached at maryolsson@mac.com. ◆

COLUMN

INDUSTRY INSIGHTS

continued from page 11

If autos had kept up with the cost of a transistor in an IC, you would be able to buy 6000 cars for a dollar, each costing a small fraction of a cent ... garages for all those cars would be prohibitive, however.

If autos had kept up with processor performance, your average car would get 220 million miles per gallon. That is 8,800 times around the earth or 7 times the distance to Mars ... on a gallon.

There have been predictions for years that Moore's Law would run out of gas ... no pun intended. Moore's Law is not ending, it is merely morphing. We are using the vertical dimension to pack more circuits. We are using software to leverage the performance of IC's like never before. We are finding new materials and processes that continue driving progress. You can call it whatever you want, but semiconductors will continue getting faster, cheaper, smaller, and more efficient with more functionality for a long time to come.

If semiconductors did not exist, we would still have a world with food, clothes, houses and books. We would still have TV's, though you'd have to go to the store occasionally to test and replace the vacuum tubes.

What we have, for better or for worse, is today's high tech world. The evolving technologies, products and services that most people take for granted are enabled primarily by the continual improvements in semiconductor industry.

I would declare that no other industry comes close to the total impact that our industry has made on the world over the past 70 years. I think we can all be proud to be a part of this unique phenomenon. It is at the bottom of it all ... ◆

RON JONES is CEO of N-Able Group International; a semiconductor focused consulting and recruiting company. N-Able Group utilizes deep semi supply chain knowledge and a powerful cloud based software application to provide Conflict Mineral Compliance support services to companies throughout the semiconductor supply chain including fabless, foundry, OSAT and materials suppliers. Email ron.jones@n-ablegroup.com for more info.

AmTECH MICROELECTRONICS, INC.

Your Advanced Microelectronics and Complex Micro-SMT Solution

AMTECH MICROELECTRONICS was established in 1993 by a core team of Silicon Valley professionals. The team's roots coming from the design, engineering and manufacturing of emerging technologies including Thick-Film Hybrid Microelectronics, Chip-On-Board and Chip-On-Flex. These technologies were used to create products incorporating Micro-SMT, Die Attach, Wire Bond, Lid Seal and Encapsulation processes.

The team work experience started in the early 1980s designing and manufacturing hundreds of multilayer Thick-Film hybrids on Alumina and Aluminum Nitride substrates. These assemblies incorporated multiple die, many times up to (30) die per hybrid device. These hybrids often required trace widths as small as 100um built on ceramic substrates with thicknesses as low as 250um. They were part of ISHM (IMAPS), and gained a great deal of experience with MIL-STD-883, a military Test Method Standard for Microcircuits. It covers requirements for environmental, mechanical and electrical tests for microelectronics, including visual inspection (monolithic, hybrid and passive components), wire bond strength (DPT and NDPT), die shear as well as many other test methods.

Surface Mount Technology was developed in the 1960s and became widely used in the mid-1980s. By the mid-1990s, the great majority of high tech electronic printed circuit board assemblies were dominated by surface mount devices. Printed circuit board based technologies have always been more price competitive than ceramic hybrids. As the printed circuit board technology matured, Chip-On-Board and Chip–On-Flex became a more cost effective option and began replacing the ceramic hybrids. During the 1990's these microelectronic assemblies were referred as Multi-Chip Modules on ceramic MCM-C, on laminate MCM-L or on silicon MCM-D.

Clearly over the last five years the traditional SMT market has been trending fast to ultra-small Semiconductor industry requirements. There is a growing demand for Advanced Microelectronics products incorporating Micro-SMT (miniature bottom termination components) and Semiconductor IC Assembly. It is difficult in today's market to identify a U.S. source with a strong Engineering team that offers both of these disciplines at one location. OEMs generally have to deal with two different suppliers, one for SMT and one for IC Assembly.

AmTECH has been a leading edge technology supplier of Advanced Microelectronics and Complex Micro-SMT Assembly since 1993. Their customer's products come with very unique requirements for product miniaturization, performance, quality and reliability. They like to think of AmTECH as an extension of their customer's Engineering and R&D team. All of the people at AmTECH are committed to driving quality and innovation at every level of the organization.

THE KEY IS A KNOWLEDGEABLE AND EXPERIENCED ENGINEERING TEAM

AmTECH's "Hands-On" Engineering team, skilled manufacturing Technicians and experienced assembly Operators solve manufacturing challenges and accelerate time-to-market for each product they manufacture. They provide customers with 25-years of leadership and experience in solving design, engineering, and manufacturing challenges that come with Advanced Microelectronics Assembly.

They are defining a new standard of excellence as a manufacturer of highly sophisticated microelectronics products. These products require high levels of value added engineering, laser-focus attention to detail and technical expertise. AmTECH is recognized for its strong Engineering team and deep understanding of today's leading edge technologies. This includes substrate technology (ceramics, laminates and silicon); multiple heterogeneous assembly processes, and advanced automated equipment capabilities.

Amtech's team has a proven record in new product introduction (NPI) where they have been responsible for product launches in a variety of industries. In the early-2000s AmTECH started assembling prototypes for Fiber Optic Transceivers. These products grew to a very high volume in production prior to moving to Asia for low cost manufacturing five years later.

Later in the mid-2000s AmTECH supported original design manufacturing (ODM) companies building medium volume production Camera Modules. These modules were for next generation cellular phones and built on thin-rigid printed circuit boards and rigid-flex incorporating Micro-SMT, precision die placement and wire bonding. AmTECH currently supports Automotive/LiDAR, Medical, Biotech, Industrial, Photonics and many other markets requiring Advanced Microelectronics with heterogeneous assembly processes.

QUALITY

• Their New Product Introduction (NPI) process includes a Design for Manufacturing review (DFM) to ensure products are designed for optimum yield before they go into production.

• AmTECH's manufacturing team has a stop-on-defect policy to prevent products with failures moving down the manufacturing line.

• AmTECH manufacturing engineers immediately solve problems when they occur.

• Solder paste inspection prior to pick & place and 100% post-reflow 3D High Resolution AOI.

• XRAY inspection of all bottom termination components including void analysis.

• Metrology for all critical measurements of substrate and assembly.

• Functional test when required by customer.

MICROELECTRONICS ON LAMINATE AND CERAMIC SUBSTRATES

AmTECH works with leading edge technology products on a variety of substrates:

• Rigid PCB: ≥1.00mm to ≥3.0mm thick

• Thin-Rigid and Rigid-Flex PCB: ≥0.3mm to ≤1.0mm thick

• Flex PCB: ≥0.1mm to ≤0.2mm thick

• Ceramic LTCC (<1000°C), Thick-Film and Thin-Film

• Ceramic HTCC (>1600°C), for high reliability and hermeticity

AmTECH is one of a few electronics manufacturing companies that focus on Advanced Microelectronics and solves complex manufacturing challenges that require high levels of engineering and technical expertise. Their core focus is Microelectronics, and their infrastructure and cleanroom are designed to support its complexity.

3D High Resolution AOI and XRAY.

AMTECH PROVIDES:

• State-of-the-Art Microelectronics center in Silicon Valley

• Certified to ISO 9001:2015 quality standards

• ITAR Registered, Cleanroom: ISO-7, Class 10K

• Workmanship: MIL-STD-883 and IPC-A-610

• Complex higher level heterogeneous assembly

ADVANCED MICROELECTRONICS CAPABILITIES INCLUDE:

• Precision Die-Attach, Flip-Chip and Multi-Chip

• Gold and Aluminum fine pitch wire bonding

• Plasma Cleaning for wire bond surface preparation

• Wire Bond Pull, Die Shear and Ball Shear Test

• Glob Top, Dam & Fill, Underfill and UV Encapsulation

• Complex Micro-SMT Assembly

• 3D High Resolution AOI and 160Kv XRAY Inspection

• Metrology for all critical measurements of substrate and assembly.

DIE ATTACH, also known as Die Bond, is the process of attaching a die or multiple die to Rigid, Rigid-Flex, Flex PCB or Ceramic substrate. Precision X/Y placement accuracy and repeatabil-

AmTECH Markets

Automotive/LiDAR

Medical/Biotech

RF Wireless/Microwave

ity requirements for die placement, die height, bond-line-thickness and rotation are critical in Advanced Microelectronic products.

FLIP CHIP is a method of interconnecting IC chips with solder bumps/balls that have been deposited onto the top-side IC chip pads to a substrate. The IC chip is flipped over during assembly so that its top-side faces down.

• X/Y Placement +/-10um accuracy @3s, Theta Placement +/-0.15° accuracy

• Die Attach die size: 0.25mm – 50mm (0.010" to 2.0")

• Flip Chip die size: 0.5mm – 25mm (0.020" to 1.0")

• Flip Chip pitch: 0.15mm to 0.3mm (0.006" to 0.012")

• Die thickness: 0.1mm – 0.7mm (0.004" to 0.028")

• Die/ Flip-Chip pick from: wafer, waffle pack, Gel-Pak and JEDEC tray

• Die/ Flip-Chip place to: Rigid, Rigid-Flex, Flex PCB or Ceramic substrate

WIRE BONDING: There are three main wire bonding processes that AmTECH offers for interconnecting bare-die IC Chips to Rigid, Rigid-Flex, Flex PCB or Ceramic substrates.

• Gold Ball Wire Bonding (Thermosonic @ +150°C)

• Gold Wedge Wire Bonding (Ultrasonic @+150°C)

• Aluminum Wedge Wire Bonding (Ultrasonic @+25°C)

GLOB TOP, DAM & FILL, UNDERFILL AND UV ENCAPSULATION

Encapsulation processes are used to protect fragile die and wire bonds. AmTECH analyzes the epoxy fluids, the assembly, the parts, and your accuracy requirements so we can recommend the best process. AmTECH's innovations and in-depth knowledge of dispensing technology and materials have continuously led the industry while focusing on customer needs for the best dispense and encapsulation process.

• Glob top with rigid black encapsulant for high reliability applications.

Flip Chip and Precision Die Attach.

Ultra Fine-Pitch Wire Bonding.

Complex Micro-SMT Pick & Place.

• Glob top with flexible UV light/moisture-cure clear encapsulant.

• Dam & Fill two-part dispensing process for large die with high count wire bonds.

• Underfill JET and Auger dispensing for CSP and Flip-Chip components.

COMPLEX MICRO-SMT

AmTECH provides Complex Micro-SMT Assembly with lead-free (RoHS) and tin-lead (Non-RoHS).

• DFM: engineering review of PCB Fab, PCB Design and Assembly documentation.

• High-performance solder paste printing down to 150um diameter (6) mils.

• Precision placement of SMD components: +/-25um for ICs, +/-35um for Passive.

• Custom reflow soldering thermal profile for RoHS and Non-RoHS.

• Ionograph for ionic contamination cleanliness testing.

• Advanced 3D High Resolution Automated Optical Inspection.

• 160Kv XRAY Inspection including BGA and Flip-Chip void analysis.

AmTECH has a high level of expertise in the development and production of miniaturized electronics for sophisticated applications that come with very unique requirements for product performance, quality and reliability. They put a premium on service, quality, and on-time delivery. They are a company with a state-of-the-art facility in Silicon Valley and a company that is proud of its Engineering team and its latest generation equipment for Advanced Microelectronics. AmTECH's main goal is to bring their customers peace of mind as they work with them through the development and manufacturing.

EXPERIENCE YOU CAN TRUST

They believe product development and manufacturing should be worry-free, no matter how complex your project is. AmTECH has over 25-years of experience in the design, engineering and manufacturing of microelectronics devices. They fully understand their state-of-the-art automated equipment capabilities, and they offer engineering expertise in material science for substrate, solder, au wire, al wire, and all types of die-attach and encapsulation epoxies.

They have seen a growing demand for Advanced Microelectronics for Automotive/LiDAR, Medical/Biotech, IoT devices, and all types of devices for portable and flexible hybrid electronics (FHE). They strongly believe this trend will continue well into the future. All of these new products require extreme attention to detail and expertise during Design, Engineering and Manufacturing.

For more information about **AmTECH Microelectronics** call 408-612-8888 or visit www.amtechmicro.com. ◆

standards

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We connect the breadth of the entire electronics supply chain by including applications such as the Internet of Things, Artificial Intelligence, Machine Learning, and other adjacent markets.

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- 22nd Fab Management Forum
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- Executive Keynote Opening
- SEMI Networking Night

KEY FACTS

More than ...

- 35% visitors represent engineering job functions
- 70% involved in purchasing decisions
- 33% are executives and senior managers
- 8,700 visitors from 85 countries registered in 2017

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Wirebonding Variables: How Much Can the Design and Process Engineers Control?

Dr. Chris Lykke, Fellow and Chief Statistician
Phil Marcoux, Consultant and
MEPTEC Advisory Board Member

A PRIOR ARTICLE IN THE MEPTEC Report discussed design factors under the part designer's control that could enhance manufacturability of the wire bonding step of the package assembly process. The article concludes by encouraging production engineering involvement early in the design process. (*Ref: Product Design for Manufacturability, William Boyce, Smart Microsystems, pg. 24 MEPTEC Report Vol. 22 No. 2*)

In analyzing the MEPTEC Report article it was concluded that the author's advice for early intervention would work for companies that have dedicated manufacturing operations in close proximity to the design and where design to production cycles are short. However, for many organizations, there are limitations:

1) Package assembly is contracted to OSATs located thousands of miles from the design operation and production doesn't start until several months or years have passed since the design phase.

2) The design engineers have limited latitude to make changes that deviate from the printed or suggested design guidelines.

3) The primary source of loss in yields involves multiple factories usually attributed to vendors/materials/temperatures of which the design engineer has little or no control.

The authors decided to construct a hypothetical example to illustrate the challenge a designer faces when they sub-contract their IC package assembly and when the assembly is performed at or even shared among different factories. Below is the example that ranks five common causes of post packaging yield loss resulting from out-of-control material/part design and out-of-control assembly technology factors.

Yield Loss Cause	% of Total Defects
1. Presence of Contaminants/Glass on Pads	50% (material/ fab process)
2. Voiding in the Bonds	30% (assembly technology and/or material/fab process)
3. Looping Shorts	10% (assembly technology)
4. Bond Placement Issues/Probe Damage	5% (assembly technology)
5. Substrate Issues causing no-sticks	5% (assembly technology)
6. Equipment Related Issues	0% (assembly technology)

Assume a 300mm wafer with 1000 net good die after wafer testing and delivered for assembly. Further assume 100% good post singulation and die attach yield.

After wirebonding, yield defects were found on 100/1000 (10%) of the die (see table above).

In this hypothetical example, the main source of defects is pad contamination (50%) and voiding (30%). These may or may not be related and they may or may not have been caused during wafer fabrication as opposed to being caused by the assembly processes. For this example, the designers may only have some very remote influence over #4 (Bond Placement), so they have little to no direct influence on yield improvement. However, they probably do feel the direct impact caused by the immediate yield losses and by the possible field failures from parts that fail later in time.

The authors stress the concept of "Critical to Function" as a guiding principal for quality and production management. Critical to Function or CTF is an objective formula technique for discriminating inputs that are **deal-breakers** (these significantly impact yields and costs) versus inputs that are **cosmetic or tolerable**. When implemented, it can become a valuable tool for helping the various teams within a customer's facility or a contractor's facility to mobilize for improvement.

It should be the expanded role of both design and process engineers to prioritize where process and design changes can be implemented to make substantial changes in yield. Going one step further involves (1) proposing an objective test for separating out critical from noncritical to function factors and (2) making collaborative customer-based process or design changes that reduce CTF failures. As an example of a design improvement, if there is adequate space on the chip, one can create "back-up" or redundant bond pads for CTF circuit connections, i.e. those connections which render the chip dead if there's no connection. Also, weak connections can be identified as CTF if they impact critical to function connections, such as the power and ground connections.

The process engineers can then create methods to screen out or work with the material experts to constrain problem factories and set up the best processes for manufacturing solutions.

This could include the additional documentation step of die to wafer traceability. For example, we may encounter faulty sections of a wafer that have wire

no-sticks or obvious weak bonds during the wirebonding of a high volume product consisting of wafer lots up to 25 wafers. For such a case, we could opt to segregate the die from a suspect wafer rather than subject the entire wafer lot of 25 wafers to segregation.

This level of traceability could then give the assembler, the process engineers, and the customer the ability to better improve overall wirebonding capability. This could be accomplished by implementing CTF tests that target catching these "weak link" issues.

Conclusion

The bond yields for ICs can vary depending on material related contamination, temperature/humidity, and equipment problems more so than design influenced factors. The hypothetical model in our example illustrates that the impact both design and process engineers have can be minimized if they only have influence on noncritical to function factors.

So, the above example presents a case that the causes of the yield losses are often not anything designers can directly compensate for by design. However, by taking on an expanded role, they can provide Critical to Function notification and tests which alert the assemblers to potentially dire consequences caused by these types of defects.

Dr. Chris Lykke, Ph.D. *has been a Chief Statistician and Fellow at several large medical device companies (Baxter Healthcare, Alza/J&J, Abbott, and Cepheid/Danaher) and has made multiple contributions to develop and improve quality testing in both R&D and process manufacturing. His expertise in Design of Experiments (DOE), data mining, reliability failure testing and survival analyses, and process modeling /capability/ sampling plan testing has helped create new products and incorporate scaled-up test methods for product transfer and manufacturing. He particularly enjoys working on Critical-to-Function failure problems and recent applications that tie to his background in discriminant analysis and neural network models, powerful predictive methods linked to current Artificial Intelligent applications.*

Phil Marcoux *has been co-founder and CEO of three companies and business and technical advisor to many others. He is co-inventor and owner of over 38 issued patents in the area of Wafer Level Packaging, Chip Scale packaging, Silicon Interposers, 3D and 2.5D packaging. Author of many articles and texts on SMT, 3D IC assembly, and one of the first textbooks on fine pitch SMT packaging and processes titled "Fine Pitch Surface Mount Technology". Published by Van Nostrand in 1992. ISBN 0-442-00862-7. In 2007 Phil was named "The Father of Surface Mount Assembly in the US" by the IPC resulting from his founding and management of AWI (Santa Clara, CA). AWI (founded in 1981) was one of the first companies in the US to install AI based equipment and specialize in automated electronic design and assembly.* ◆

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William Boyce
SMART Microsystems Ltd.

OFTEN SMART MICROSYSTEMS will receive a request to fabricate a part for which there is either an incomplete engineering drawing, or there is no drawing at all. This concern is not unique to SMART and can be heard echoed throughout the industry. With the recent advancements in solid modeling and 3D printing technology, it is often assumed that the engineering drawing is going by the way of the dinosaur and Dodo bird. As modeling software has improved, there has been a movement toward paperless forms of documentation. However, this shift does not mean the end of the engineering drawing. For mechanical components, sub-assemblies, and assemblies, the drawing contains critical information that is not found anywhere else. This information, such as geometric dimensioning and tolerancing (GD&T), dimensional tolerances, critical fabrication or assembly information in the form of drawing notes, and title block, is all parts of a larger picture that is necessary to fabricate the part. Although tolerances and GD&T can be found in the solid models of today, they lack the big picture perspective required by most suppliers to fabricate the part. If the assembly happens to contain a machined part, the machinist will need to have instructions and dimensions to fabricate said part. Typically, machinists will not work solely from a solid model.

GD&T symbols are the first thing to pay attention to on an engineering drawing. These symbols are the system for defining and communicating engineering tolerances. GD&T symbols are typically tied to a datum. The part drawing requirements are derived from the next higher assembly. This is to say, the part, and therefore the drawing requirements, flow from the top down. It follows that the datums contained in the GD&T symbols also flow from the top down. As an example, when designing a fixture to hold a customer part for a specific process, the customer driven geometric requirements are derived from the same datums. If the bottom most surface of the part is the datum by which all others are referenced, then the tooling and fixtures must be designed accordingly. An understanding of things like flatness, parallelism, perpendicularity, concentricity, and position, described with a common descriptive language like GD&T helps get assemblies fabricated properly.

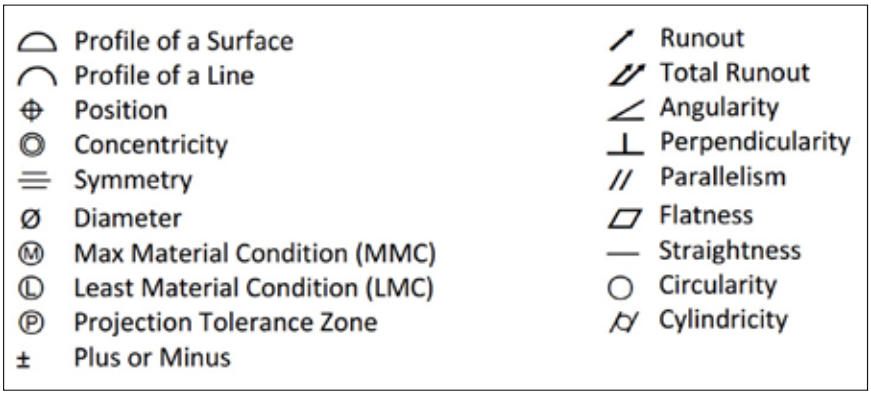

Figure 1. Some common GD&T symbols.

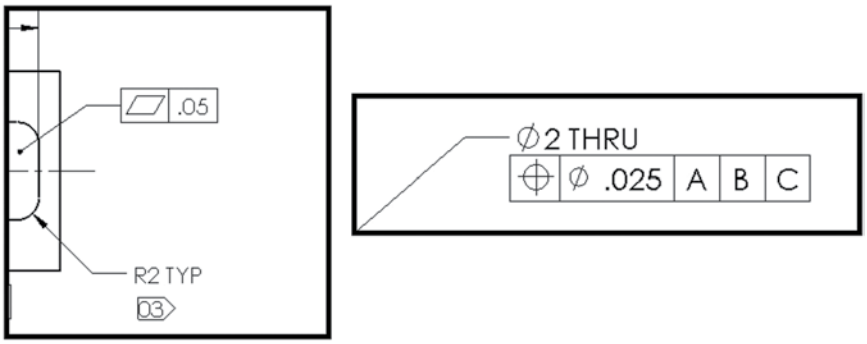

Figure 2. Sample images from an engineering drawing using GD&T symbols.

Dimensional tolerancing on a drawing is the next thing that should be looked at. Tolerancing communicates, among other things, how big the process window will be when the part is fabricated. These dimensional tolerances are also derived from the next higher assembly, but have a more direct impact on cost and manufacturability. As a general rule, the tolerance for a specific feature dimension should not be any tighter than is absolutely necessary to achieve the desired objective (fit, form, and function) of the next higher assembly. This is because the tighter the tolerance, the higher the cost, and the lower the manufacturability. As an example, if a specific through hole is 0.5mm with a tolerance of ±0.10mm, this part will be likely manufacturable at relative volumes at reasonable cost. If that tolerance is tightened to ±0.001mm, depending on the depth, many tool houses may no-bid the project at any cost. Another thing to look for in an assembly drawing is tolerance stack. If the tolerance of the completed assembly is tighter than the combination of tolerances of the individual components in the assembly, then, by definition, the assembly may not be manufacturable in volumes greater than one. Additionally, the parts ultimately may not function as intended over the production life of the product.

Possibly the most important section of a drawing is the drawing notes. Critical

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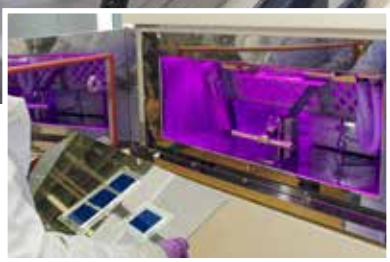

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fabrication or assembly information, in the form of drawing notes, should be contained on every drawing. These are arguably the most critical instructions and requirements of any engineering drawing package. This is a critical section of the complete drawing, which is commonly overlooked. The drawing notes should be numbered. These numbers can correspond to specific sections of a drawing. As an example, the drawing may call out "see note 10" and note 10 may contain specific cautionary requirements like "this surface for Au wire bonding, must be free of any foreign contamination to include but not limited to the following list". Alternatively, a note may contain specific plating requirements, or compliance with a certain page and section of a specification such as Mil Std 883. The drawing notes are the final word of critical assembly or fabrication instructions.

The title block of a drawing may seem relatively unimportant. However, just the opposite is true. A title block contains the general tolerance information, the units in which the document is dimensioned, the authority under which it was released, and the most current revision. An engineering drawing is a record of work scope and should be treated as such. If the drawing is changed later, the revision needs to be changed accordingly, and the work scope needs to be reassessed.

There are several reasons that an engineering drawing is an invaluable tool. The mere act of generating this document forces the engineer and design team to think critically about every aspect of the process and the part. To create a complete engineering drawing, critical thought must be given to how a part is fabricated, assembled, and measured. The ability to measure a process or part is very important. In the engineering world, anything that cannot be measured does not exist. Therefore, without the ability to measure the process, the part cannot be fabricated. It is easy to forget that just because everything fits together perfectly in SolidWorks does not mean it will fit together in reality. That is not how things work in the real world of manufacturing. To ensure successful manufacturing, a thoughtful and complete engineering drawing must be generated. There simply are no substitutions or shortcuts. ◆

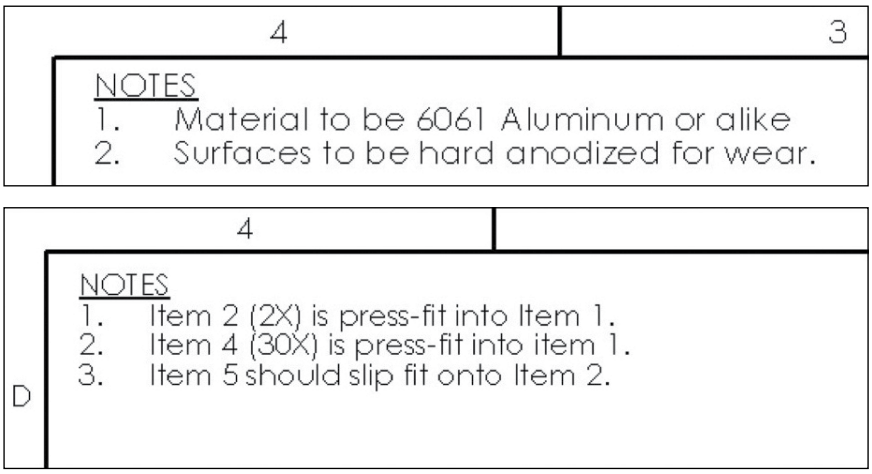


Figure 3. Sample engineering drawing notes - arguably the most critical instructions and requirements of any engineering drawing package.

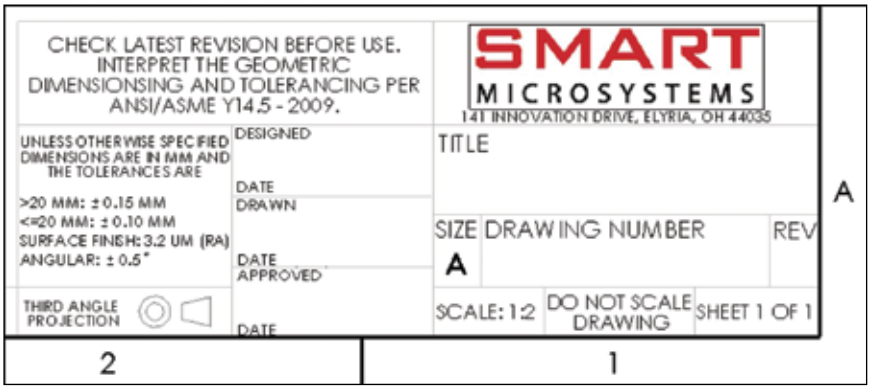
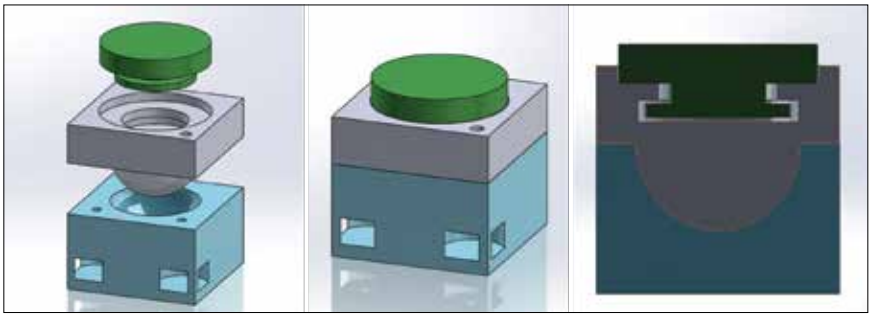


Figure 4. Sample engineering drawing title block.



3D Modeled Assembly (Exploded View) | 3D Modeled Assembly (Isometric View) | 3D Modeled Assembly (Cross-Sectioned View)

Figure 5. 3D modeled assembly views generated using 3D CAD software.

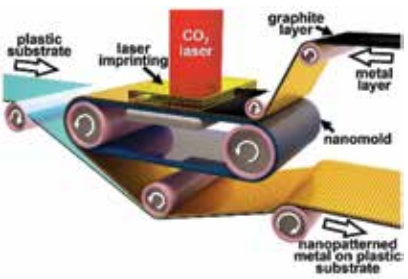
William Boyce is the Engineering Manager at SMART Microsystems. He has served in senior engineering roles over the last 19 years with accomplishments that include manufactured automotive sensors. He is certified in EIT and Six Sigma Green Belt and is an industry recognized expert in Al wire bonding. Additionally, he designed and led the metrology lab and machine shop at Sensata. Mr. Boyce earned a Bachelor of Science in Engineering degree from the University of Rhode Island and has been a member of the IMAPS New England Chapter for over 10 years.

State-of-the-Art Technology Briefs

A special feature courtesy of Binghamton University

We are pleased to continue this feature in the MEPTEC Report, brought to us by new Advisory Board member Dr. Gamal Rafai-Ahmed from Xilinx. The State-of-the-Art Technology Briefs contains articles from the Binghamton University S3IP "Flashes." Full text is available upon request through the IEEC Site at: http://www.binghamton.edu/s3ip/index.html.

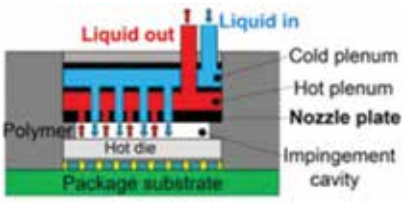
University of Maryland researchers have demonstrated the first single-photon transistor using a semiconductor chip. The device can process 10 billion photonic qubits every second. The photonic chip is manufactured from a semiconductor with holes in a honeycomb configuration. As light enters the chip it reflects and gets trapped by the hole pattern. Analogous to conventional computer memory, the dot stores information about photons as they enter the device. This technique could allow many quantum light transistors to be linked together and can eventually lead to compact quantum computers that process large numbers of photonic qubits. *(IEEC file #10712, Science Daily, 7/6/18)*



Purdue University researchers have developed a new manufacturing technique, using a process similar to newspaper printing for ultrafast electronic devices with smoother and more flexible metals. The method is called roll-to-roll laser-induced super plasticity and uses a rolling stamp like that used for high speed newspaper printing. The technique can induce "superelastic" behavior to different metals by applying high-energy laser shots, which enables the metal to flow into the nanoscale rolling stamp. *(IEEC file #10728, Solid State Technology, 7/20/18)*

University of Washington researchers have discovered a method to encode information using magnets that are just a few layers of atoms in thickness. The researchers used stacks of ultrathin sheets of chromium tri-iodide (CrI3) to exert control over the flow of electrons based on the direction of their spins This breakthrough could revolutionize both cloud computing technologies and consumer electronics by enabling data storage at greater densities and improved energy efficiency. *(IEEC file #10619, Science Daily, 5/3/18)*

Researchers in China have demonstrated a self-powered brain-linked vision electronic skin for mimicking the human retina. Sensory substitution with flexible electronics is one of the intriguing fields of research that takes place in nanotechnology labs around the world. In the future artificial retinas integrated with the human body may not only repair damaged vision but also improve vision to see wider ranges of wavelengths. The design of the brain-linked vision electronic skin is constructing using an integrated flexible system including photodetector array, information analyzer, signal transmitter, and electricity power unit. *(IEEC file #10601, Nanowerk, 4/16/18)*



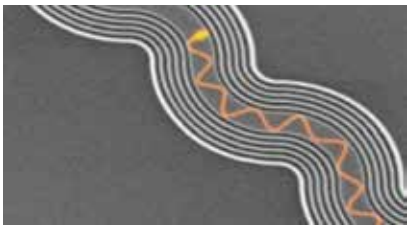
Imec semiconductor researchers have developed a new impingement chip cooler that is a 3D printed 'showerhead' that sprays the cooling liquid directly onto the bare chip. The spouts shoot liquid into a small space in between the cooling system and the surface of the semiconductor before heated coolant is expelled through separate plumbing. The rinse could prevent chips, including 3-D chips, from burning as they go to higher and higher power densities. *(IEEC file #10660, Electronic Design, 5/29/18)*

University of Texas researchers have created boron arsenide crystals that have very high thermal conductivity. The heat dissipation mechanism in these boron arsenide crystals is through the vibrations of the material. As the crystal vibrates, the motion creates phonons (packets of energy) which as quasiparticles carry the heat. Because the semiconducting material efficiently transports heat, it has applications in future electronics to help keep high power devices from overheating. *(IEEC file #10709, Solid State Technology, 7/6/18)*

University of Michigan researchers have developed a technique to stack solution-processed organic solar cells on top of vacuum-processed cells, creating a tandem solar cell. The top cell absorbs infra-red up to 950nm, and the bottom cell absorbs visible light starting at 350nm. Individually the cells can achieve up to 11% efficiency. When stacked together the increase light absorption and efficiency improves to 15% with an anti-reflection coating. It was calculated that an 18% efficiency can be achieved in the future for this type of multi-junction device. *(IEEC file #10600, Electronics Weekly, 4/30/18)*

Argonne National Lab and Harvard University have developed a new class of flat, ultrathin optical devices on a chip. The design uses a MEMS as the platform. The optical lens is controlled with dynamic and high-speed control to actively steer incoming light. The ultrathin lenses have potential to replace bulky traditional and expensive curved lenses in systems. Adding active control to this new class of nanostructures will greatly expand their function in optical technologies. This enables integration of other hybrid structures of varying dimensions. The new dynamic metasurface lens has potential across wider fields, such as MEMS-based microscope systems and holographic and projection imaging. *(IEEC file #10729, ECN, 7/23/18)*

Light Fidelity (Li-Fi) is a high speed, bidirectional and fully networked wireless communication technology like Wi-Fi and has potential to radically change the high-speed data communications sector. Li-Fi, which uses light waves rather than radio waves, will enable users to transmit data using LED bulbs at speeds exceeding current Wi-Fi. Because Li-Fi uses visible light as the transmission medium, it is not subject to the spectral capacity concerns now surrounding Wi-Fi. Li-Fi can be used in places where radio frequencies may interfere with equipment (e.g. hospitals), or locations where Wi-Fi signals cannot reach or are weak (e.g. underground locations). *(IEEC file #10683, ECN, 6/7/18)*



Purdue University researchers have developed a new protective metamaterial "cladding" that prevents light from leaking out of the curvy pathways it travels in a computer chip. Because processing information with light can be more efficient than with electrons used in current devices, it is beneficial to confine the light onto a chip. By controlling the anisotropy (i.e. enables light to travel at different velocities in different directions) of the cladding, they prevented light from leaking off track into other waveguides where "crosstalk," of information could occur. *(IEEC file #10748, Science Daily, 7/30/18)*

University of South Australia researchers have demonstrated a novel and energy-efficient approach to storing data using nano-sized crystals of salt encoded with data using light from a laser. New technologies are required to meet the demands of terabyte or even petabyte storage. One of the most promising techniques of achieving this is optical data storage. Their research shows that these fluorescent nanocrystals could represent a promising alternative to traditional magnetic and solid-state data storage. They demonstrated rewritable data storage in crystals hundreds of times smaller than visible with the human eye. This 'multilevel data storage' can open the way for much higher storage densities. *(IEEC file #10724, ECN, 7/12/18)*

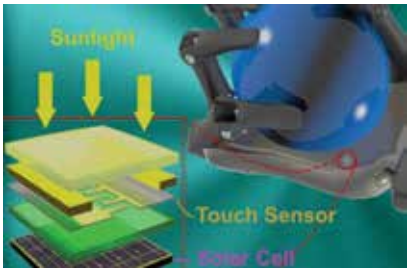
MARKET TRENDS

University of Oklahoma researchers are developing quantum-enhanced sensors that have applications ranging from biomedical to chemical detection. The team demonstrated quantum states of light to enhance the sensitivities of state-of-the-art plasmonic sensors. These sensors can be probed with light and have been shown to operate at the shot noise limit. When interfaced with quantum states of light, the noise floor can be reduced below the classical shot noise limit which makes it possible to obtain an enhancement of the sensitivity. *(IEEC file #10650, Science Daily, 5/15/18)*

Carnegie Mellon University researchers have created a concept smartwatch named the LumiWatch which is able to project and illuminate a touchscreen onto your forearm. The watch is self-contained and can perform independent operations without connection to a smartphone or computer. The smartwatch measures 50mm and consists of a logic board, projector, depth-sensing array, metal enclosure and battery. Projectors are a convenient way to create a temporary screen, which makes them the ideal way to improve the functionality of smartwatches. *(IEEC file #10626, Product Design & Development, 5/3/18)*

The MEMS market is expecting 17.5% growth in value between 2018 and 2023, and to reach $31 billion in 2023. The consumer market segment is the biggest share, with more than 50%. The RF MEMS industry plays a key role in the total MEMS industry development. Combed with the standard MEMS market growth of 9% the CAGR reaches 17.5%. *(IEEC file #10672, Electronics Weekly, 6/4/18)*

University of California researchers have fabricated foldable electronic switches and sensors directly onto paper using inexpensive materials for use in generators, supercapacitors and other applications. The researchers replaced the more expensive metals with molybdenum. The desired circuitry patterns, which are 100 microns wide, are written by a laser beam, ultimately heating the molybdenum to approximately 1,000°C and forming conductors of durable molybdenum carbide. *(IEEC file #10720, R&D., 7/9/18)*



University of Glasgow researchers have developed a way of harnessing the sun's rays to power synthetic skin which could create advanced prosthetic limbs capable of returning the sense of touch to amputees. They made a touch-sensitive covering for prosthetic hands using graphene and integrating photovoltaic cells into this "electronic skin." Graphene's optical transparency, which allows 98% of the light which strikes its surface to pass directly through it, which makes it ideal for gathering energy from the sun. *(IEEC file #10739, Medical Design Technology, 7/19/18)*

The four major contributors to the growth in the semiconductor industry are: artificial intelligence (AI), the Internet of Things (IoT) revolution, Level 3 autonomous vehicles, and high-throughput technologies such as 5G and augmented/virtual reality (AR/VR) The revenues for these technology areas are expected to rise by 7% in 2018. These developments are driving increased demand across all semiconductor segments, *(IEEC file #10671, Electronic Products, 6/4/18)*

RECENT PATENTS

Dielectric-based waveguiding in a multi-layer PCB (Assignee: IBM Corp.) *Patent No.- 15/331614* – Embodiments

herein describe a high-speed communication channel in a PCB that includes a dielectric waveguide sandwiched between two ground layers. The dielectric waveguide includes a core and a cladding where the material of the core has a higher dielectric constant than the material of the cladding. Thus, electromagnetic signals propagating in the core are internally reflected at the interface between the core and cladding such that the electromagnetic signals are primary contained in the core.

Staged via formation from both sides of chip (Assignee: Tessera Inc.) - *Patent No.- 15/842080* – Method of fabricating a semiconductor assembly can include providing a semiconductor element having a front surface, a rear surface, and a plurality of conductive pads, forming at least one hole extending at least through a respective one of the conductive pads by processing applied to the respective conductive pad from above the front surface, forming an opening extending from the rear surface at least partially through a thickness of the semiconductor element, such that the at least one hole and the opening meet at a location between the front and rear surfaces, and forming at least one conductive element exposed at the rear surface for electrical connection.

Through silicon via (TSV) formation in integrated circuits (Assignee: Analog Devices) - *Patent No.- 15/334619* – Integrated circuit substrates having through silicon vias (TSVs) are described. The TSVs are vias extending through the silicon substrate in which the integrated circuitry is formed. The TSVs may be formed prior to formation of the integrated circuitry on the integrated circuit substrate, allowing the use of via materials which can be fabricated at relatively small sizes. The integrated circuit substrates may be bonded with a substrate having a microelectromechanical systems (MEMS) device. In some such situations, the circuitry of the integrated circuit substrate may face away from the MEMS substrate.

Ball grid array formed on printed circuit board (Assignee: Realtek Semiconductor) *Pub. No. - US9955586* – Ball Grid Array (BGA) formed on printed circuit board is provided. The BGA comprises a first solder ball module and a second solder ball module. The first solder ball module comprises a plurality of first solder balls, wherein one of the first solder balls is grounded for shielding two other first solder balls, and one of the first solder balls is floating. The second solder ball module comprises a plurality of second solder balls, wherein two of the second solder balls are grounded and one of the two grounded second solder balls penetrates the printed circuit board through a plated through hole formed on the printed circuit board for shielding two first solder balls.

Copper-based conductive paste in chip package Cu-Cu bonding (Assignee: Shenzhen Inst of Adv Tech)- *Patent No.- CN106205772* – The invention provides a copper-based conductive paste and preparation and application thereof in chip package copper-copper bonding. The copper-based conductive paste is prepared by uniformly dispersing pretreated nano-copper particles in a conductive paste solution and counted by 100% of total mass of the copper-based conductive paste, the nano-copper particles account for 10-90% of the total mass of the copper-based conductive paste. Low temperature high density package integration of interconnected flip chips can be realized.

Metal bonding pads for packaging applications (Assignee: IBM Corp.) *Patent No – 10,020,281*– Methods for bonding a first semiconductor device to a second semiconductor device include forming metal pads including a textured microstructure having a columnar grain structure at substantially the same angular direction from the top surface to the bottom surface. The textured crystalline microstructures enable the use of low temperatures and low pressures to effect bonding of the metal pads. Also described are methods of packaging and semiconductor devices.

BINGHAMTON UNIVERSITY

BINGHAMTON UNIVERSITY *currently has research thrusts in healthcare / medical electronics; 2.5D/3D packaging; power electronics; cybersecure hw/sw systems; photonics; MEMS; and next generation networks, computers and communications. The S3IP Center of Excellence is an umbrella organization comprising five constituent research centers. More information is available at www.binghamton.edu/s3ip*

Integrated Electronics Engineering Center (IEEC) The IEEC is a New York Center of Advanced Technology (CAT) responsible for the advancement of electronics packaging. Its mission is to provide research into electronics packaging to enhance our partner's products, improve reliability and understand why parts fail.

More information is available at ***www.binghamton.edu/ieec***

Center for Autonomous Solar Power (CASP) The CASP center focusses on thin film solar cells and supercapacitors. The recent progress incudes 7.5% efficiency pure sulfide CZTS solar cell without an antireflection coating, and nano-structured transition metal oxide supercapacitor with specific capacitance of 760 F/g, maximum energy density of 8 Wh/kg, and a power density of 13 KW/kg. The CASP team has been invited to take part in the Cohort 5 NEXUS-NY program to explore market opportunity of a dielectric capacitor technology (patent currently drafted) that recently came out of CASP center. More information is available at ***www.binghamton.edu/casp.***

NorthEast Center for Chemical Energy Storage (NECCES) NECCES is working on the limitations to batteries reaching their ultimate potential. Recently they have placed emphasis on a new cathode and a new anode. The LixV0P04 cathode can attain over 300 Ah/kg compared with around 160 Ah/kg for the commercial LiFeP04 cathode. The SnyFe/C composite anode has a more than 50% higher capacity than today's graphite-based anodes.

More information is available at ***www.binghamton.edu/necces.***

Analytical and Diagnostic Laboratory (ADL) The ADL provides an array of analytical and diagnostic tools located in a single facility to address the needs of faculty and industry in understanding materials, structures and failures that are found in electronics packaging. The ADL supports the 5 research centers previously mentioned. The facilities of the ADL are available to our industry partners.

More information is available at ***www.binghamton.edu/adl*** ◆

High Thermal Semi-Sintering Die Attach Paste

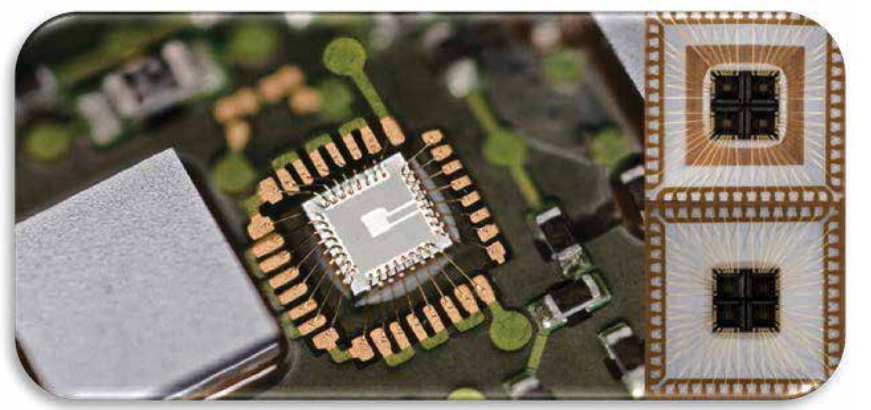
No Solder, No Pressure, No Problem

Raj Peddi, Henkel Corporation

NO MATTER WHERE YOU LOOK, IT seems that nearly every part of the electronics sector is being impacted by the integration of smaller, higher-functioning devices. Smartphones, data centers, automobiles, airplanes, smart home systems and even gaming devices are all packing massive capability into more compact spaces. As consumers, we love what this brings to our lives. As designers and manufacturers, we understand what this brings to the device – more heat! Thermal management isn't a new concern; effectively dissipating heat has always been a key component of reliable operation. Today, however, power densities are being maximized, making managing the thermal load increasingly challenging.

While thermal interface materials are a large part of the equation at the board level, die level thermal management is also an important element of optimized device reliability. Until recently, high thermal die attach solutions were limited to high-lead solders which are subject to impending environmental phase-out legislation; or, silver sintering materials that require integration of complex processes. Even previous generation, so-called high thermal die attach pastes have been unable to deliver ultra-high thermal conductivity because of silver filler interface contact limitations.

With these shortcomings understood, Henkel materials scientists embarked on a development project to formulate a high thermal die attach portfolio that is processed as easily as standard die attach and provides the high thermal conductivity of high-lead solder and pure silver sintering, while delivering the reliability characteristics of resin-based die attach pastes. The result is a semi-sintering – also referred to as hybrid sintering – die attach paste that allows simultaneous silver particle sintering and resin matrix curing. The new, patent-pending LOCTITE® ABLESTIK® ABP 8068T semi-sintering die attach paste series has successfully addressed the regulatory challenges of high-lead solders, thermal conductivity drawbacks of conventional die attach pastes, and processability shortcomings of sintering products that require high pressure.

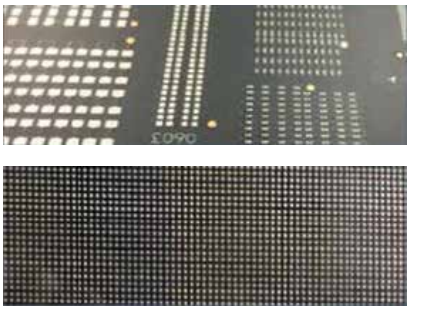


Processability and Performance

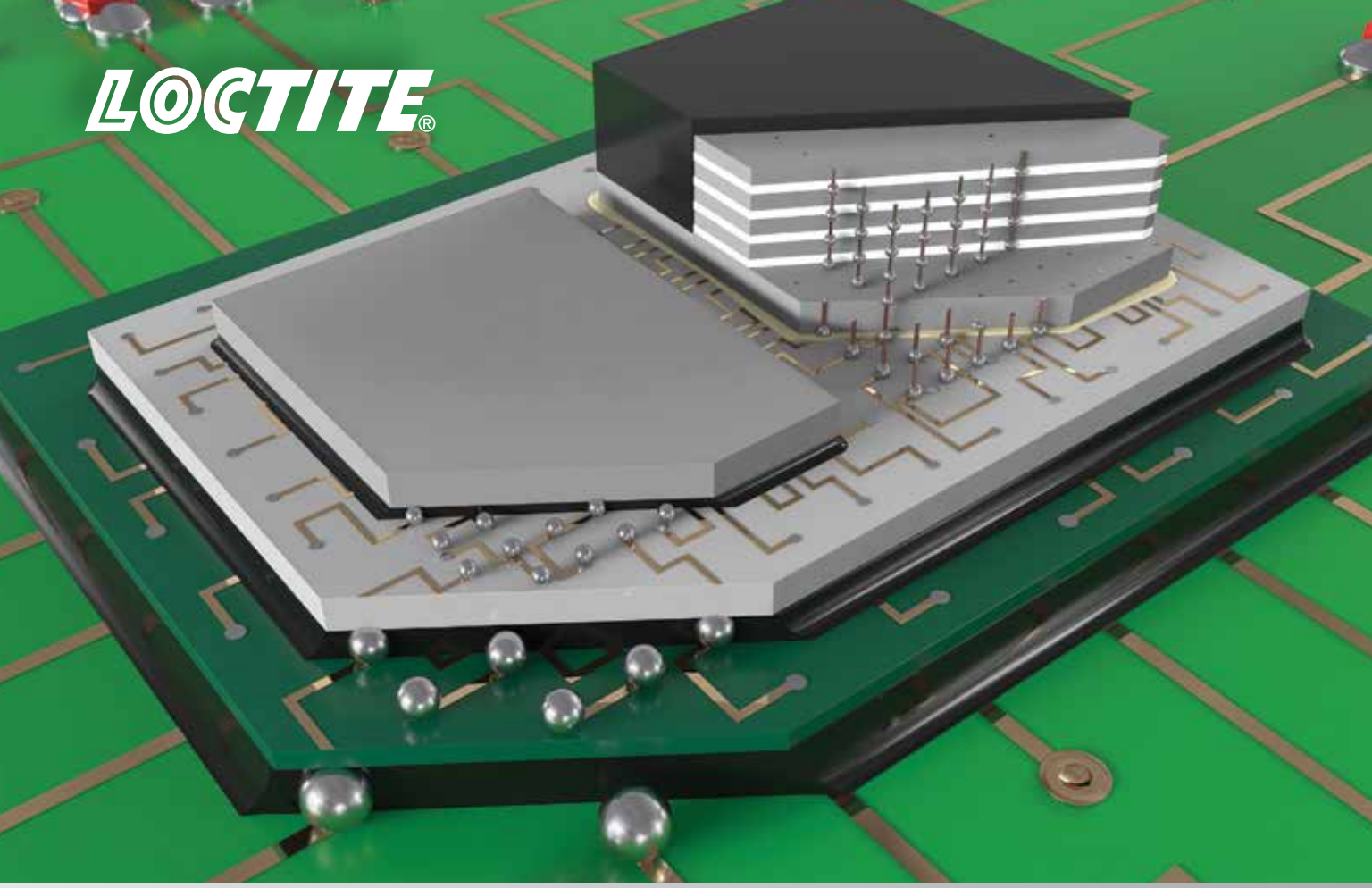
Ease-of-use is a key advantage of LOCTITE ABLESTIK ABP 8068T materials; they can be processed with existing methods, allowing use of needle dispensing and/or printing platforms and standard bonding equipment for maximized UPH. There is no requirement to invest in additional equipment or change current processes; the pressure and high heat needed to achieve sintering with some sintering products aren't necessary. Henkel's semi-sintering materials exhibit no missing dots, paste separation or adhesion degradation after 24 hours of continuous dispensing. Excellent resin bleed out control on different lead frame surfaces is also a characteristic of the new semi-sintering die attach pastes.

Consistent Printing and Dispensing for 24 Continuous Hours

Good printability and consistent dispensing with no separation or missing dots



In many cases, high power applications integrate miniaturized packages where multiple packages are processed on a single strip. Because of this serial approach, the die attach paste materials used must be compatible with long post-dispense times while awaiting die placement and adhesive curing. This time after material deposition and prior to die placement is referred to as 'open time' and, if the paste does not have a long open time and dries out or cures



NON CONDUCTIVE FILM

Advanced Packaging Technologies Get Reliability Boost From NCF Material

Today's smaller footprint, greater I/O package designs dictate use of emerging technologies like through-silicon via (TSV) and copper pillar to address form factor requirements. With this come thinner dies for 3D stacking and higher-density bump, driving the need for greater protection to ensure reliability. In the memory market, where TSV applications with die less than 100 µm thick are common, Henkel's new non-conductive film (NCF) technology provides controlled flow, stability and protection without the concerns associated with paste-based underfill materials and challenges posed by thermal compression bonding.

For more information, contact 1-800-562-8483
or visit us online at henkel-adhesives.com/electronics

Henkel

from exposure, poor wetting, incomplete fillets or inconsistent bond line thicknesses may result and adversely affect reliability. LOCTITE ABLESTIK ABP 8068T's stage time – the time after the die is bonded but before the material is cured – is also very forgiving in order to achieve optimal manufacturability.

The adhesion performance of the LOCTITE ABLESTIK ABP 8068T series semi-sintering pastes on various die sizes (as large as 5 mm x 5 mm) and lead frame finishes (including Ag, Cu, PPF and Au) is also robust. In addition, thermal conductivity of the material when cured at 200°C is 110 W/m-K, which is comparable to pure silver sintered materials.

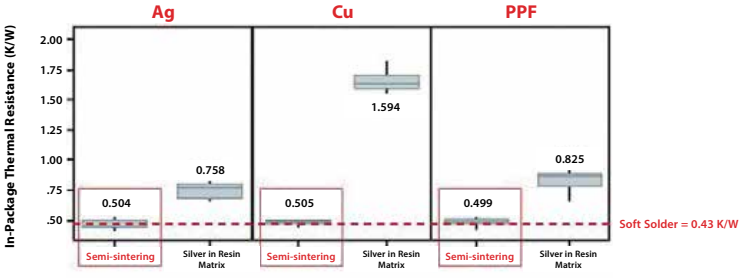
Reliability

As in-package thermal conductivity is a more accurate predictor of reliability performance than standard bulk thermal conductivity measurements, an in-package thermal test was conducted to evaluate LOCTITE ABLESTIK ABP 8068T within a functional QFN package. The semi-sintering material exhibited better in-package thermal performance than traditional Ag-filled die attach adhesives on all lead frame surfaces – even Cu, where conventional materials struggle to form an intermetallic layer and have high interfacial thermal resistance. Here, the semi-sintering die attach paste showed in-package thermal resistance similar to that of soft solder, indicating it is a viable replacement for solder materials.

Finally, because of LOCTITE ABLESTIK ABP 8068T's ability to bind the silver sintered structure in its unique resin matrix, the semi-sintering materials do not exhibit the brittleness of pure silver sintered materials. This makes Henkel's semi-sintering portfolio applicable to a wide die size range, providing high elongation (toughness) for better thermal cycling performance and, therefore, reliability.

For more information about Henkel's novel semi-sintering die attach pastes, download our recent webinar and/or visit Henkel's semi-sintering product page. ◆

LOCTITE® ABLESTIK Semi-Sintering System
In Package Thermal Resistance (Rth)



In-package thermal resistance comparable to soft solder on multiple lead frames

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OSRDA - Out-Sourced R&D and Assembly

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Even for low heat resistant devices and various materials that can not be mounted at high temperature mounting, all new construction MONSTERPAC® can be handled.

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Magazines and Carriers for Process Handling Solutions


Film Frames


Film Frame Magazines


Film Frame Shippers


Grip Rings


Grip Ring Magazines

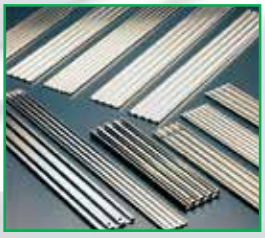

Grip Ring Shippers

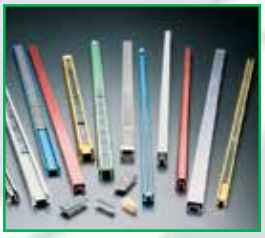

Lead Frame Magazines - F.O.L./E.O.L.


Stack Magazines - E.O.L.


Process Carriers (Boats)


Boat Magazines


I. C. Trays - Multi-Channel


I. C. Tubes and Rails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