SPRING 2020

MEPTEC Report

A Quarterly Publication of The Microelectronics Packaging & Test Engineering Council

Volume 24, Number 1

THE CONCEPT AND PRACTICE OF CONCURRENT ENGINEERING

Having a Complete Team Approach from the Very Beginning of the Product Design

page 20

+

Is the Heterogeneous Integration Roadmap the Best Path to Increased Revenues?

page 11

SIP-based RF Modules Squeeze More Functionality into Devices

page 16

Indoor Positioning Technology Takes Center Stage - Enabled by Systems-in-Package (SiP) Modules

page 18

INSIDE THIS ISSUE

INDUSTRY LEADING Packaging

Amkor Technology®

Enabling the Future

amkor.com ▶ sales@amkor.com

Amkor's Advanced System in Package solutions enable highly integrated products with performance advantages, smaller footprint, increased component density and superior system operation.

Changing Direction

Ira Feldman
Executive Director, MEPTEC

WELCOME! FROM LONG TIME MEPTEC members to recent subscribers to casual visitors, we are glad you are here.

Technology is a global business that changes rapidly. Companies and related organizations require the tenacity and the ability to adapt to survive over the 'long haul'. As the COVID-19 epidemic spreads, individuals and organizations worldwide will be challenged to adapt. MEPTEC is no exception and we will continue to change to not only survive but thrive as we have done over the past thirty years. At the same time, our hearts go out to everyone who has been directly impacted. We hope that the exposure can be minimized to reduce the case load globally.

Two immediate changes are being made to the upcoming **Known Good Die (KGD) Workshop** and our monthly **Semiconductor Industry Speaker Series luncheons** jointly hosted with IMAPS. First: KGD, was originally scheduled for April, has now been postponed to the September 16, 2020 as local health officials have banned large gatherings here in Silicon Valley. (An updated event schedule will be posted at www.kgdworkshop.org shortly.)

Secondly, the speaker series luncheons will be postponed until local gatherings are again considered safe. In the meantime, we are working with speakers to present via webcast in April and May. Yes, there is nothing that beats the in-person networking at one of our luncheons. However, if we cannot meet IRL (in real life), virtual meetings are the way to go. We are working to switch up our existing speaker lineup as we change the luncheons into webinars. The end result will be opportunities for speakers to share their knowledge and expertise across the entire MEPTEC and IMAPS communities here in Silicon Valley and beyond.

As always, we are looking for informative speakers to talk about challenges and solutions for packaging, test, design, outsourced assembly and test (OSAT) business models, etc. for the Speaker Series. If you would like to suggest a topic or know someone who would be a great speaker at a future webinar or luncheon, please let us know.

The Advisory Board (AB) is now working to "re-plan" our event calendar for 2020. We will be announcing via email and our website (www.meptec.org) the revised schedule including full day events and luncheons as details are known.

I look forward to hearing your suggestions and feedback as to how MEPTEC can best serve you. Please don't be shy!

Stay safe and healthy!

Ira Feldman
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Does the FPGA Industry Face Peril? *Pt. III*

Martin Hart
TopLine Corporation

PART II OF THE WINTER 2019 MEPTEC REPORT titled "Call to Action" urged stakeholders to create a shared vision to ensure a robust, resilient and sustainable supply chain for production of Field Programmable Gate Arrays (FPGA) devices.

Executive Order 13806 Assessment Report

The Department of Defense published an unclassified report titled, "Assessing and Strengthening the Manufacturing and Defense Industrial Base and Supply Chain Resiliency of the United States," in fulfillment of Executive Order (EO) 13806 which describes risks that threaten America's manufacturing and defense industrial base.

The ten "risk archetypes" described in the report are as follows: 1) Sole source; 2) Single source; 3) Fragile supplier; 4) Fragile market; 5) Capacity constrained supply market; 6) Foreign dependency; 7) Diminishing manufacturing sources & material shortages (DMSMS); 8) Gap in the U.S.-based human capital; 9) Erosion of U.S.-based infrastructure; and 10) Product security.

Most of the risk archetypes described in the EO 13806 assessment report apply to FPGA manufacturing. Risk archetypes lead to a variety of impacts upon America's industrial base. These include reduced investment in new capital and R&D; reductions in the rates of modernization and technological innovation; potential bottlenecks across the many tiers of the supply chain; lower quality and higher prices resulting from reduced competition.

Sole Source Versus Single Source

A sole source risk exists when only one supplier is able to provide the required capability. Fortunately, manufacturing capability for producing copper-wrapped solder columns (shown in Figure 1) exists today in the USA. Also, multiple subcontractors who are capable of providing column attachment services for FPGA packages currently exist in America.

A single source exists when only one supplier is qualified to provide a required capability. The EO 13806 report draws a key distinction between sole source and single source. Multiple suppliers may exist, but only a single source for copper-wrapped solder columns is qualified, according to the Qualified Manufacturing List (QML-38535) published by the Defense Logistics Agency (DLA). Companies that produce FPGA devices are not required to voluntarily qualify multiple subcontractors. It could take 24 months for an alternative candidate starting from scratch to attain QML status should a single source supplier unexpectedly shut down.

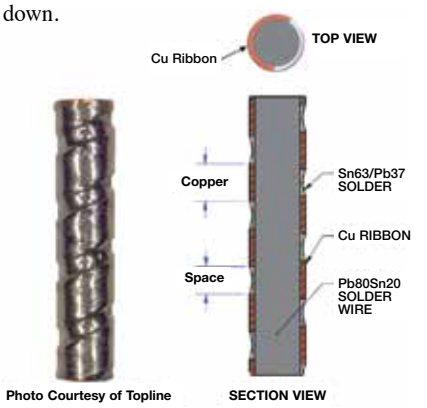

Figure 1. Construction of Copper Wrapped Solder Column.

Other Risks

A fragile supplier is an individual firm that is financially challenged or distressed, and this potentially includes most subcontractors in the U.S. microelectronics industry today.

A fragile market occurs when domestic markets have structurally challenging economics and face the potential to move toward foreign dependency.

Presently, a capacity-constrained supply market may not be thought of as problematic. However, a single source supplier may not be able to keep up with a sudden surge in market demand.

Foreign dependency on wafer foundries could become an elevated risk, especially when a domestic foundry does not produce a critical item.

Diminishing manufacturing sources and material shortages risk is often associated with obsolescence that might result when a relevant supplier issues end-of-life warnings.

Gaps in U.S.-based human capital is an ongoing concern. Think: the graying of "Silicon Valley". The industry needs to keep fresh science, technology engineering and math (STEM) talent in the pipeline especially within the microelectronics assembly base. Attaching copper wrapped solder columns to FPGA packages is fundamentally a non-automated, artisan process, which requires highly developed operator skills.

Erosion of U.S.-based infrastructure, including the loss of specialized capital equipment, is a risk since attachment of solder columns to FPGA packages requires precision tools and fixtures that are difficult to fabricate.

Lastly, product security could be of heightened concern under circumstances where FPGA packages require an assembly step overseas, opening the risk of reverse engineering or embedding trojans by hostile foreign actors.

Conclusion

Negative impacts can manifest as gaps in the industrial base, including single-points-of-failure, threatened capabilities and extinct capabilities. Fortunately, domestic manufacturing of copper wrapped solder columns is already available. Multiple American microelectronic subcontractors are ready to provide copper wrapped column attachment services for FPGA packages on the condition that funding is available to pay for QML qualification. An investment in such qualification today can mitigate that risk, rather than waiting for an unexpected disaster to strike. Such a disaster could result in diminished readiness, insecurity of supply, and program delays caused by the inability to deliver FPGA components in a timely manner. A production stoppage of critical FPGA components could possibly tip the balance of peace in the World Order. ◆

MEPTEC
THE NEXT GENERATION

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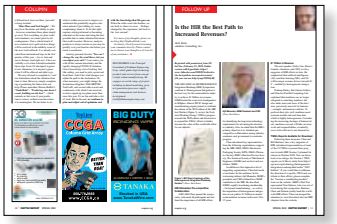
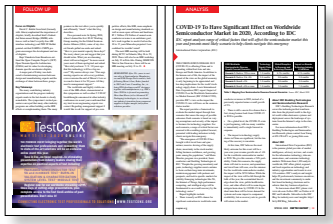


11 FOLLOW UP – The 3rd Annual Heterogeneous Integration Roadmap (HIR) Symposium confirms it: Heterogeneous Integration is the best way for the industry to achieve $1 Trillion in revenues. SEMI hosted the event in Milpitas, CA. Almost 200 IC design and manufacturing experts joined, to celebrate the release of the 2019 edition of the HIR last October.

HERB REITER
EDA2ASIC CONSULTING, INC.

13 ANALYSIS – The Coronavirus Disease 2019 (COVID-19) has affected China and has spread within East Asia and into Europe and North America. In addition to the human cost of life, the impact of the spread of the virus on the global economy is only beginning to be appreciated and has deep implications for the world's technology supply chain.

INTERNATIONAL DATA CORPORATION (IDC)



14 MARKET TRENDS – The recent U.S. - China trade war turmoil has made Western semiconductor manufacturers come to the realization that they should keep their fabs closer to home. U.S. companies with back-end facilities located in Asia are getting increasingly concerned because of the risk of overly centralizing production in just one location.

STEPHEN ROTHROCK
ATREG, INC.

16 PACKAGING – System-in-Package is a way of providing a complete system in what looks externally like a single component like a chip in a QFN package. Inside they are increasingly sophisticated systems, which can incorporate semiconductors, passives, and radio frequency (RF) components.

NICK WOOD
INSIGHT SIP

18 TECHNOLOGY – Recent corporate activity between major semiconductor vendors and startups has thrust Ultra-Wide Band (UWB) indoor positioning technology onto center stage. What events signaled this new trend? What indoor positioning technology is available to design engineers today? What do these recent moves mean for the technology?

NICK WOOD AND CHRIS BARRATT
INSIGHT SIP

DEPARTMENTS

Front Cover
Photo Courtesy of SMART Microsystems

CFIUS CONCLUDES REVIEW OF PLANNED ACQUISITION OF CYPRESS

On March 9, 2020, the Committee on Foreign Investment in the United States ("CFIUS") concluded its review under Section 721 of the Defense Production Act of 1950, of the planned acquisition of Cypress Semiconductor Corp. as announced by Infineon Technologies AG on June 3, 2019. CFIUS cleared the transaction. The closing of the Merger remains subject to approval from China's State Administration for Market Regulation (SAMR) and other customary closing conditions under the merger agreement.

www.infineon.com

AEHR RECEIVES OVER $2.9 MILLION IN ORDERS FOR WAFER-PAK CONTACTOR AND DIEPAK CARRIER

Aehr Test Systems has announced it has received orders totaling over $2.9 million from its installed base of FOX™ test and burn-in system customers for its proprietary WaferPak™ Contactors and DiePak® Carriers. Aehr's FOX wafer-level test and burn-in systems utilize its proprietary WaferPak Contactors, which provide cost-effective solutions for making electrical and thermal contact with a full wafer or substrate in a multi-wafer or multi-panel environment. Aehr's FOX-XP multi-wafer and singulated die/module test systems utilize its proprietary DiePak Carriers to enable burn-in of singulated die and multi-die modules to screen for defects in both the die and the module assembly processes.

www.aehr.com

Xilinx Launches Industry's First SmartNIC Platform Bringing Turnkey Network, Storage and Compute Acceleration to Cloud Data Centers

Also unveils OCP 3.0 form factor XtremeScale™ Ethernet adapter; proof of concept for world's first FPGA-based OCP Accelerator Module

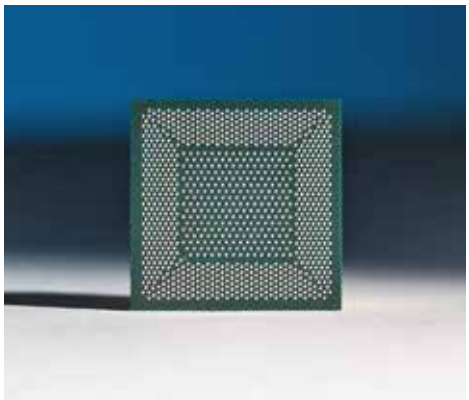
XILINX HAS ANNOUNCED the industry's first SmartNIC platform delivering true convergence of network, storage and compute acceleration functions on a single device. The Alveo™ U25 SmartNIC is designed to bring the greater efficiency and lower TCO benefits of SmartNICs to cloud service providers, telcos, and private cloud data center operators struggling with increasing networking demands and rising costs. The U25 combines a highly optimized SmartNIC platform with a powerful and flexible FPGA-based engine that supports full programmability and turnkey accelerated applications. The U25 delivers a comprehensive SmartNIC platform to address the industry's most challenging

demands and workloads such as SDN, virtual switching, NFV, NVMe-oF, electronic trading, AI inference, video transcoding, and data analytics.

Xilinx also unveiled the new XtremeScale X2562 10/25Gb Ethernet adapter card based on the OCP Spec 3.0 form factor. Designed for high-performance electronic trading environments and enterprise data centers, the X2562 features sub-microsecond latency and high throughput with ultra-scale connectivity for real-time packet and flow information to thousands of virtual NICs. The X2562 is currently sampling and will be generally available in the second calendar quarter of 2020.

For more information, visit www.xilinx.com. ◆

Computers That Smell: Intel's Neuromorphic Chip Can Sniff Out Hazardous Chemicals



IN A JOINT PAPER PUBLISHED IN NATURE Machine Intelligence, researchers from Intel Labs and Cornell University demonstrated the ability of Intel's neuromorphic research chip, Loihi, to learn and recognize hazardous chemicals in the presence of significant noise and occlusion. Loihi learned each odor with just a single sample, without disrupting its memory of previously learned scents. It demonstrated superior recognition accuracy compared with conventional state-of-the-art methods, including a deep learning solution that required 3,000 times more training samples per class to reach the same level of classification accuracy.

Using a neural algorithm derived from the architecture and dynamics of the brain's olfactory circuits, researchers from Intel and Cornell trained Intel's Loihi neuromorphic research chip to learn and recognize the scents of 10 hazardous chemicals. To do so, the team used a dataset consisting of the activity of 72 chemical sensors in response to these smells and configured the circuit diagram of biological olfaction on Loihi. The chip quickly learned the neural representation of each of the smells and recognized each odor, even when significantly occluded, demonstrating a promising future for the intersection of neuroscience and artificial intelligence.

To learn more about Intel's innovations, go to newsroom.intel.com and intel.com. ◆

JCET Enters Into Strategic Business Agreement with Analog Devices to Grow Singapore Test Business

JCET GROUP CO., LTD. has entered into a strategic business agreement with Analog Devices Inc. in which JCET will acquire ADI's test facility in Singapore. As part of this agreement, JCET will take on additional ADI test business in this newly acquired facility. Final transfer of ownership of the ADI Singapore facility to JCET will be completed May 2021.

"This agreement with our long time assembly and test partner JCET will allow ADI to take advantage of the operational and test engineering expertise we have experienced for many years as a customer in their Singapore plant" stated Steve Lattari, Senior Vice President of Global Operations and Technology at ADI. "ADI has been a highly valued and long standing customer of JCET. This opportunity to both grow our test floor footprint in Singapore and more importantly our business with ADI is a win-win for our companies," stated Li Zheng, CEO of JCET Group. "JCET's investment in this Singapore facility also shows that as a multinational semiconductor company, we will continue to steadily strengthen our global expansion and provide first-class integrated circuit products and advanced technical services to international and local customers," continued Mr. Zheng.

JCET Group has six factories located in China, Singapore and Korea. Its Singapore facility was established in 1994 as the first Outsourced Semiconductor Assembly and Test (OSAT) provider in Singapore.

Further information is available at www.jcetglobal.com. ◆

NAMICS Receives Intel's Preferred Quality Supplier Award

NAMICS CORPORATION has been recognized by Intel as a recipient of a 2019 Preferred Quality Supplier (PQS) Award. The PQS Award recognizes companies like NAMICS that Intel believes have relentlessly pursued excellence and conducted business with resolute professionalism.

"I am pleased to recognize the winners of Intel's Preferred Quality Supplier Award for 2019," said Dr. Randhir Thakur, head of Global Supply Chain at Intel. "The commitment to continuous improvement and the rich collaboration with these suppliers remain crucial factors in enabling Intel to bring exciting products to market and meet the needs of our customers."

To qualify for PQS status, suppliers must exceed high expectations and uncompromising performance goals while scoring at least 80 percent on an integrated report card that assesses performance throughout the year. Suppliers must also achieve 80 percent or greater on a challenging continuous improvement plan and demonstrate solid quality and business systems. ◆

DYCONEX AG STAFF CHANGES IN QUALITY MANAGEMENT

DYCONEX AG, an MST company and global leader for highly complex solutions in electronic interconnect technology, has announced the following staff changes in quality management: Dr. Hans-Peter Klein, who has headed up quality assurance at DYCONEX since 2009, retired at the end of February 2020. Effective March 1, 2020, Dr. Selcuk Mentese replaced him and became a member of the executive management. Dr. Mentese previously worked for DYCONEX as a process engineer and process quality manager from 2005 to 2011 and rejoined the company in early 2019.

www.dyconex.com

ENVIRONMENTAL CONTAINTMENT TAPE SUPPLIES DONATED BY ULTRATAPE TO HELP IN THE FIGHT AGAINST COVID-19

UltraTape Industries, a division of Delphon and leading supplier of cleanroom tape and custom label products announced the donation of environmental marking, sealing and containment tapes to the Oregon COVID-19 Response effort.

Environmental containment is essential to combat the spread of COVID-19. The donation of UltraTape's high-quality industrial tapes will assist in marking off quarantine areas, creating barriers, and the cuff-sealing tape can be used to seal the space between gloves and personal protective garments.

www.delphon.com ◆

Palomar Technologies Moves to New Global Headquarters

Expands Manufacturing Footprint to Meet Growth Goals and Customer Needs

PALOMAR TECHNOLOGIES has announced that to meet growing customer demand for its solutions around the world, it has moved to a new global headquarters and expanded its facilities to over 110,000 square feet.

"Since acquiring SST International (renamed to SST Vacuum Reflow Systems) in 2015, our global business has rapidly developed with a new customer base and these new facilities make it possible for Palomar to meet the growing global demand for our entire product line," said Bruce Hueners, CEO and President for Palomar Technologies and SST Vacuum Reflow Systems.

Palomar has its roots in the Aerospace & Defense industry with its origins as a technology division within Hughes Aircraft. Over the 40+ years of supporting the semiconductor and photonics industries, Palomar Technologies has expanded beyond its traditional segments across automotive (LiDAR & power modules), medical semiconductor/biophotonics, microwave, RF/wireless, 5G, Datacom, telecom, industrial and a few niche markets.

The new facilities complement Palomar's expansion in 2019 of its contract manufacturing facilities in Singapore, as well as collaborating with the Electronics and Photonics Innovation Center (EPIC) in Paignton (Torbay), in the United Kingdom to open a demonstration/prototyping laboratory to serve its growing European customer base. The new headquarters is located at 6305 El Camino Real, Carlsbad, California, 92009 USA.

SST Vacuum Reflow Systems has also expanded to over 24,000 square feet of precision manufacturing, machine shop, prototype/demonstration laboratory and office space. The expansion will enable the company to meet the growing needs for its new 8300 Series Automated Vacuum Pressure Soldering System specifically designed to deliver high-quality power modules for automotive and commercial applications. Their address remains the same at 9801 Everest St., Downey, California, 92042 USA.

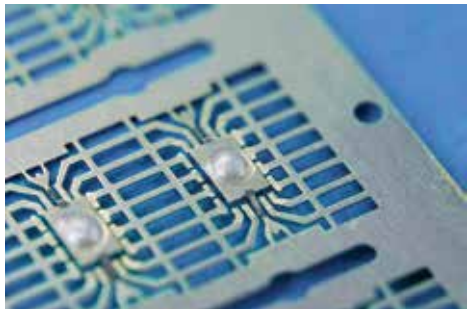
For more information, visit palomartechnologies.com. ◆

Electrically Conductive Die Attach Epoxy with High Glass Transition Temperature

MASTER BOND EP17HTS-DA IS A NEW one component, no mix, die attach epoxy that is electrically conductive and withstands high temperatures. It is a silver filled system. Typically, glass transition temperature (Tg) declines with the addition of a filler like silver. However, with this specialty formulation, a high Tg of 140-150°C is maintained and it passes MIL-STD-883J thermal stability requirements at 200°C.

Its strength profile is also notably robust with a die shear strength of 35-40 kg-f at room temperature. EP17HTS-DA meets NASA low outgassing specifications and its service temperature extends from -80°F to 550°F. It has a low volume resistivity of less than 0.005 ohm-cm and also performs well as a heat conductor.

EP17HTS-DA is a thixotropic paste and can be easily dispensed manually or via automated dispensing systems. This compound is not premixed and frozen and has an unlimited working life at room temperature. It requires a heat cure of 300°F for 2 to 3 hours, followed by post curing at 350°F for 1 to 2 hours.



This product bonds well to many substrates including metals, ceramics and plastics. It is recommended for applications where low volume resistivity and high temperature resistance is required. EP17HTS-DA is available for use in syringes and glass jars, in sizes ranging from 20 grams to several pounds.

Read more about Master Bond's adhesives for die attach as well as other demanding microelectronic applications at www.masterbond.com/industries/die-attach-epoxy-adhesives or contact Tech Support. Phone: +1-201-343-8983 Email: technical@masterbond.com. ◆

COUPLING & CROSSTALK

By Ira Feldman

Electronic coupling is the transfer of energy from one circuit or medium to another. Sometimes it is intentional and sometimes not (crosstalk). I hope that this column, by mixing technology and general observations, is thought-provoking and "couples" with your thinking. Most of the time I will stick to technology but occasional crosstalk diversions may deliver a message closer to home.

Roller Coasters & Proverbs

ARE YOU THE TYPE OF PERSON who flips to the end of the book to see how the story ends before starting it? Or one who reads the online reviews with the plot summary – including the spoilers – before watching the movie? If so, do you want to know how the coronavirus COVID-19 epidemic turns out? Well, I could tell you how it ends. But more important than the ending is in what genre will the story eventually fit? Horror? Science Fiction? Mystery and suspense? Humor? I suspect not… Love? Heroism? Leadership?

The story is like a roller coaster ride. It ends right where it starts. However, there is much fear, panic, and screaming enroute from the start to the finish. And right now - here in the United States as I write this - we are still on the "way up" the first hill just before the plunge. We can hear the screaming of those who have gone before us; we glimpse the twisted track ahead. China has led the way and they have already taken the first plunge in the group of cars ahead. But we are all wondering how many more ups, downs, twists, and turns remain? And there may be a dark tunnel ahead from which we think we will never emerge. In the moment we will be full of terror. But in the end, we will come to a full and complete stop after a very bumpy and terrifying ride. Will we fully recover from our fear, nausea, and excitement? And, more important will our outlook and capabilities change?

Until now "work" was a different amusement park ride – a delightful merry go round which we constantly rode to see if we could grab the brass ring of opportunity, fame, and fortune. Somehow, today we ended up on the wrong ride and now fear the future.

What is the author full of? Comparing a viral epidemic that will likely be a global pandemic to an amusement park roller coaster ride? Is Ira nuts?..... Yes, this analogy is appropriate and informative. **Human nature is full of optimism:** sometimes it is a function of ignorance and sometimes optimism alone enables us to function. I'm betting that many people will not want to go on this roller coaster ride again (or perhaps not on a cruise ship until their memory fades) and that a lot of thought will be given to changing corporate work environments.

> The story is like a roller coaster ride. It ends right where it starts. After a bumpy and terrifying ride, we continue to plan out of optimism with the knowledge that life goes on.

The value of remote/home offices will be proven conclusively to even the most 'unenlightened' management teams in this hopefully short-term crisis. You can assume that many companies that have previously rejected the concept will embrace it looking at the potential long-term savings. Everything thing from brick and mortar savings to the ability to add lower cost offshore staff while hoping existing employees will enjoy reduced commuting time and flexible hours.

However, full-time "hermit staffing" (isolation of employees) even though essential during this epidemic is short-sighted long term. Steve Jobs was an early opponent stating: *"Creativity comes from spontaneous meetings, from random discussions. You run into someone, you ask what they are doing, you say 'Wow', and soon you're cooking up all sorts of ideas."*

So how, when things return to normal, do we get the "best of all possible worlds"? We need a winning combination of corporate savings; live interfacing with coworkers, suppliers, and customers; and at the same time reducing unproductive daily commutes? Four workable elements to provide "human interaction":

- "Hoteling" at corporate headquarters: space where offsite workers can set up for an occasional visit or meeting.
- Part time telecommuting: for companies that can afford both home and traditional offices for each employee, Laszlo Bock (former head of Google Human Resources) reports research shows one and a half days per week is the ideal work-from-home arrangement.
- Co-work locations: where remote employees can simply get some social interaction and escape the confines of their home office. (As popularized by WeWork and others even if not the best business models.) These tend to be far more productive than working in a noisy coffee shop.
- Industry Events & Conferences: They combine exposure to new ideas with social interaction. (Okay, okay, this is a shameless plug for MEPTEC and other industry events we partner with.) As I have previously written and many industry friends confirm, often the networking and interaction at a conference is far more valuable than the technical content. This is saying a lot since our event technical content is excellent! This presenter and audience interaction provides necessary synergy to make cross-functional break throughs and create new concepts to move industry goal posts forward.

In the end, each person needs to achieve the right balance between remote and 'in office' work. And the good news is that **companies will increase their demand for telecommuting equipment and network bandwidth to support these new work arrangements. The promised connectivity of 5G mobile networks** will also power these remote, and sometimes mobile, workers. All of which will drive the need for faster and higher performance electronics using advanced packaging. So even though this year's growth forecasts have now been derailed, significant future growth is expected.

P.S. While we are busy screaming in terror and trying to guess where things

will head next, here are three 'proverbs' to keep in mind:

'Man Plans and God Laughs' – We may have the desire and ability to plan - however sometimes these plans simply go awry. Not everything we plan works and sometimes we cannot plan for all contingencies. I bet a whole bunch of new contracts now spell out how things will be resolved in the unlikely event of the next viral outbreak. I've already canceled three international trips in the first quarter of this year – two to Asia and one to Europe. And right now, I have no visibility as to when I should reschedule these trips. Even if I attempted to guess at new itineraries, it is anyone's guess when I will be allowed and able to go.

We may all need to complain to 'vent' our frustrations about the situation from time to time. However, simply complaining or predicting the future does not help. Please remember Warren Buffett's **"Noah Rule" - *"Predicting rain doesn't count, building an ark does"*** – which reminds us that even if your prediction is correct, without concrete action it is meaningless. We are better to do what is within our power to improve or ameliorate the potentially negative situation instead of just talking (or worse complaining) about it. To do this right requires staying informed or becoming educated on the issues and using the best possible data to make informed decisions that result in action. However, analysis-paralysis is always unwise as you may be quickly over your head in rain before you reach a conclusion.

And my personal favorite ***"You can't change the way the wind blows, but you can adjust your sails".*** I can assure you with all the current uncertainty and the rapidly changing COVID-19 situation, I have been doing a lot of tacking. Just like sailing, you need to pick a point and head there. And if the wind changes you adjust the path to the destination. Or, when necessary, you might change the destination altogether. With MEPTEC, TestConX, and several other events and conferences with which I am involved, we have ripped up our plans more than once this year. It's no fun and takes a lot of work. But in the end, **we continue to plan and adjust out of optimism and with the knowledge that life goes on.** When the roller coast ride finishes, we are back to where we were… Perhaps changed by the experience, but back to the 'new normal'.

For more of my thoughts, please see my blog http://hightechbizdev.com.

As always, I look forward to hearing your comments directly. Please contact me to discuss your thoughts or if I can be of any assistance. ◆

IRA FELDMAN is the Principal Consultant of Feldman Engineering Corp. which guides high technology products and services from concept to high volume manufacturing. He engages on a wide range of projects including technical marketing, product-generation processes, supply-chain management, and business development.
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Is the HIR the Best Path to Increased Revenues?

Herb Reiter
eda2asic Consulting, Inc.

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THE 3RD ANNUAL HETEROGENEOUS Integration Roadmap (HIR) Symposium confirms it: Heterogeneous Integration is the best way for the semiconductor industry to achieve $1 Trillion in revenues. SEMI hosted the event at its headquarters in Milpitas. Almost 200 IC design and manufacturing experts joined, to celebrate the release of the 2019 edition of the HIR last October (Figure 1), review the Technical Working Groups' (TWGs) progress towards the 2020 edition and discuss how to expand the TWGs' efforts to further increase the value of this worldwide effort for our industry.

Figure 1. Bill Chen's hardcopy of the Heterogeneous Integration Roadmap, Version 1 *(Photo: Herb Reiter)*

HIR Stimulates Pre-competitive Collaboration

ASE's Bill Chen opened the symposium, welcomed all participants and outlined the importance of all HIR efforts for identifying the long-term technology requirements for advancing the electronics industry. Also, he stated that the HIR's primary objective is to stimulate pre-competitive collaboration among industry, academia, and government to accelerate progress.

Ajit Manocha, SEMI President and CEO
(Photo: Herb Reiter)

Chen introduced key representatives from the following organizations, supporting the HIR: IEEE, IEEE's Electronics Packaging Society (EPS), IEEE's Photonics Society, IEEE's Electron Devices Society, The American Society of Mechanical Engineers (ASME) and our host and contributor, SEMI.

In addition to this impressive list of supporting organizations, Chen had another motivator for the audience: In his welcoming address Ajit Manocha, SEMI's president, and CEO outlined how SEMI contributes to the HIR. He described SEMI's rapidly broadening membership – far beyond manufacturing – as well as the importance of heterogeneous integration on our path to $1 Trillion in annual semiconductor revenues in the next 10 to 15 years.

$1 Trillion in Revenue

The next speaker, Nicky Luu, Etron's founder, chairman, and CEO, is a key supporter of HIR efforts in Asia. He emphasized that artificial intelligence (AI), machine learning (ML), and 5G will be major revenue drivers towards $1 T – enabled by heterogeneous integration.

Pradeep Dubey, Intel Senior Fellow, and Director Parallel Computing Lab explained that machines are no longer relegated to crunching numbers, but also make more and more of the decision, previously reserved for humans – example: autonomous vehicles. To perform their jobs well, machines need accurate models and real-time data, which is highly heterogeneous. Considering the increasing shortage of human talent, machines can and will take on more work and responsibilities, eventually, even write software to run themselves.

TWG's Reports Available for Download

Following these keynotes, Chen and Bill Bottoms, also a key supporter of HIR, introduced representatives of most of the 23 TWGs to present their progress towards HIR Version 2, planned for release in October 2020. You can download, at no charge, the Version 1 TWG reports you'd like to study from https://eps.ieee.org/technology/heterogeneous-integration-roadmap.html under "2019 Edition". If you would like to influence the direction of a specific TWG and contribute to their efforts, please complete the "become a contributing member" form on the website. SEMI's Paul Trio represented Tom Salmon, who was out of town during this symposium. Bottoms, Chen and Salmon jointly head the worldwide HIR efforts. Chen encouraged the attendees to view/download relevant HIR chapters from the website.

Focus on Chiplets

David C. Kehlet from Intel (formerly with Altera) emphasized the importance of chiplets, briefly described Intel's Embedded Interconnect Bridge (EMIB) solution as well as Intel's royalty-free AIB interface technology and PHY IP. Kehlet pointed out that DARPA's CHIPS program encourages the development and use of chiplets.

Bapi Vinnakota from Broadcom outlined the Open Compute Project's (OCP) Open Domain-Specific Architecture (OSDA) and its value for developing domain-specific accelerator chiplets.

A major part of Friday was dedicated to brainstorming sessions between design and manufacturing experts and the exchange of ideas between these groups.

Key Takeaways

The many contributing industry organizations and the progress industry experts made in the last decade is clearly remarkable. The symposium's invited presenters conveyed that many other industry programs are either building on the HIR efforts or complementing them. The many pointers in this text allow you to quickly and efficiently "check" what this blog describes.

On a personal note: In Spring 2008, when I chaired the first 3D-IC Working Group meeting for the Global Semiconductor Alliance (GSA), some of my closest friends pulled me aside and asked: "How is your mental capacity these days? We worry about you and suggest that you should retire. What you are dreaming about will never happen!" In more recent years most of them apologized and asked: "How did you know 5 / 8 / 10 years ago that this technology will be a big success?" My answer always was: "Our engineering experts can solve every problem, even overcome the end of Moore's Law as we used to know it for 50 years. All they need is management support."

The worldwide and highly visible success of the HIR efforts, demonstrated at this symposium as well as other 2.5/3D-IC breakthroughs announced at other industry conferences in recent years confirmed that my trust in our engineering experts was correct. Regarding management support I would like to ask for support of pre-competitive efforts, like HIR, more emphasis on design and manufacturing standards as well as more open software and hardware IP. 1 Trillion US Dollars of annual semiconductor revenue is an ambitious goal, let's work together to reach it before the 10 to 15 years Manocha projected. I am confident he wouldn't mind!

The next HIR meeting will be held during ECTC in Orlando, May 26 to 29, 2020. There will also be an HIR workshop on July 19 in Palo Alto. During SEMICON West in San Francisco, there will be an HIR meeting on July 21 to 23. ◆

HERB REITER After 20+ years in various roles at Semiconductor Manufacturers and EDA Design Tools vendors, both following Moore's Law, Reiter founded in 2002 eda 2 asic Consulting, Inc., to bring EDA developers and IC designers together with manufacturers, e.g. ASICs. Since 2008 he is focused on promoting More than Moore (a.k.a. Advanced IC Packaging) technologies, to accelerate our industry's transition from component supplier to higher margin (sub)system solutions provider.

COVID-19 To Have Significant Effect on Worldwide Semiconductor Market in 2020, According to IDC

IDC report analyzes range of critical factors that will affect the semiconductor market this year and presents most likely scenario to help clients navigate this emergency

International Data Corporation (IDC)

THE CORONAVIRUS DISEASE 2019 (COVID-19) is affecting China and is spreading within East Asia and into Europe and North America. In addition to the human cost of life, the impact of the spread of the virus on the global economy is only beginning to be appreciated and has deep implications for the world's technology supply chain. A new International Data Corporation (IDC) report, Impact of COVID-19 on the Worldwide Semiconductor Market Forecast (IDC #US46115520), provides IDC's view on the impact the COVID-19 virus will have on the semiconductor market.

The report provides a framework to evaluate the market impact through four scenarios that assess the range of possible outcomes. Each scenario is based on varying assumptions and severity of the impact to business for technology suppliers. For each scenario, a range of critical factors are assessed with a resulting updated forecast, presented with leading indicators to help clients navigate this emergency.

"The emergence of COVID-19 has brought with it travel bans and quarantines; massive slowing of the supply chain; uncertainty in the stock market; falling business confidence, and growing panic among the population," said Mario Morales, program vice president, Semiconductors and Enabling Technologies at IDC. "Despite the growing uncertainty and panic, technology suppliers must continue to focus on their long-term investments, maintain engagement with partners and prospects, and look to specific markets for stability. Emerging technologies like 5G, the Internet of Things, high-performance computing, and intelligent edge will be fundamental to an overall recovery by the technology sector."

Report highlights include:

- There is nearly an 80% chance for significant contraction in worldwide semiconductor revenues in 2020, instead of a previously expected minor overall growth of 2%.
- There is still a one-in-five chance that a fast, strong bounce back from COVID-19 in 2020 is possible.
- On a global level, the COVID-19 crisis is just beginning, with too many variables to immediately craft a single forecast in response.
- The impact to technology supply chains in China are significant, but the timing of the recovery is uncertain.

2020 Worldwide Semiconductor Revenue Growth Forecast Scenarios	Technology Supply Chain Recovery	Global Disruption to Economy and Technology Demand	Impact on Broader Technology Industry & Initiatives
Scenario 1: Decline -12% or more	1-3 months	9-12+ months	9-12+ months
Scenario 2: Decline -3 to -6%	3-9 months	3-9 months	3-9 months
Scenario 3: Growth +2%	1-3 months	3-9 months	3-9 months
Scenario 4: Growth +6% or more	1-3 months	1-3 months	1-3 months

Table 1. Mapping Four Semiconductor Revenue Forecast Scenarios *Source: IDC, March 2020*

At this time, IDC believes the most likely outcome for this event will be a year-over-year revenue growth rate of -6% for the worldwide semiconductor market in 2020. We give this scenario a 54% probability. Under this scenario, the supply chain will start to recover, and quarantines and travel bans will ease, over the summer. For the worldwide semiconductor market, the impact will be $25.8 billion. While the impact of the virus will be felt through the bulk of the year, the accumulated knowledge about the virus, public health initiatives, and other efforts will to some degree mitigate harm done by COVID-19. In the short term there will be lower demand for systems and some impact to component availability, but as recovery sets in, growth will return to the market.

About IDC Enabling Technologies and Semiconductors Research

IDC's Enabling Technologies Research covers the technologies that transform data from the physical world to the digital world within electronics systems and deployment across the landscape of systems from the Internet's edge to the datacenter.

For more information about IDC's Enabling Technologies and Semiconductors Research, please contact Joan Young at 650-350-6471 or jyoung@idc.com.

About IDC

International Data Corporation (IDC) is the premier global provider of market intelligence, advisory services, and events for the information technology, telecommunications, and consumer technology markets. With more than 1,100 analysts worldwide, IDC offers global, regional, and local expertise on technology and industry opportunities and trends in over 110 countries. IDC's analysis and insight helps IT professionals, business executives, and the investment community to make fact-based technology decisions and to achieve their key business objectives.

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U.S.-China Trade War: The Tariff Impact on the Global Semiconductor Market

Stephen Rothrock, Founder, President & CEO
ATREG, Inc.

THE ESCALATING TRADE WAR between the United States and China has left the global semiconductor industry in uncertainty over the past couple of years. The U.S. chip industry is one of the few sectors still generating a trade surplus, largely driven by sales growth in China. The Semiconductor Industry Association (SIA) estimated that in 2018, about 36% of U.S. semiconductor company revenues came from sales to China, representing approx. $75 billion. As estimated then and now, a strong semiconductor industry is critical to U.S. global economic competitiveness in today's digital transformation era involving bleeding-edge, components-hungry technologies such as 5G, artificial intelligence (AI), Internet of Things (IoT), and automotive sub-systems. To hold on to its 45% to 50% market share as the global semiconductor leader, the U.S. faces the challenge to safeguard the innovation cycle relying on access to global markets to achieve the scale needed to fund very large R&D investments that consistently maintain U.S. technology ahead of global competitors. The tariffs imposed by the U.S.-China trade threaten this delicate balance. We at ATREG have been observing these geo-political developments from the sidelines and seen first-hand their impacts on the manufacturing asset end of the semiconductor spectrum.

Western Semiconductor Companies Will Locate Their Manufacturing Closer to Home

For many years, Asia has been the undisputed cradle for semiconductor back-end manufacturing. More than 80% of OSAT facilities are currently located in the region, 50% of which in either China or Taiwan with the rest in a handful of countries including Thailand, Japan, Vietnam, Indonesia, or Malaysia. Annual revenue among the top 25 OSATs amounted to $27.9 billion in 2018 and 65% of the A&T market is controlled by three Asia-based companies – Amkor, ASE, and JCET. The top eight OSATs (33%) account for $21.2 billion or 76% of revenue alone.

The recent U.S. - China trade war turmoil has made Western semiconductor manufacturers come to the realization that they should keep their fabs closer to home. U.S. companies with back-end facilities located in Asia are getting increasingly concerned because of the risk of overly centralizing production in just one location. As a result, sell-side activity has been increasing in Southeast Asia alone over the past few months with several assembly and test facilities currently on the market, including the Allegro MicroSystems automotive-qualified facility located in Saraburi Province, north of Bangkok, Thailand that went up for sale in February 2020 and another two confidential back-end facilities, one in Indonesia and one in Malaysia.

But this trend is not new. A handful of major Western players who used to have manufacturing operations in China have already shifted their production out or are looking at alternative manufacturing locations:

- Cree expanding SiC manufacturing in the U.S. with a brand-new greenfield fab at the Marcy Nanocenter, NY.
- Texas Instruments spending $2.5 billion to expand its existing 300mm fab in Richardson, TX.
- ON Semiconductor acquired GLOBALFOUNDRIES' 300mm fab located in East Fishkill, NY.
- Infineon investing €1.6 billion in a new 300mm wafer factory in Graz, Austria.
- Bosch deciding to keep their investments in Dresden, Germany to build a brand-new 300mm fab.
- STMicroelectronics announcing an expansion of existing sites in Europe.
- Apple and Google moving some hardware production out of China.
- Micron moved some production to Taiwan and Japan, able to mitigate 90% of the tariff impact.

China Will Reduce its Heavy Reliance on U.S. Semiconductor Suppliers

On the other side of the world, China is slowly, but surely developing its very own domestic semiconductor supply chain. The objectives of the heavily government-subsidized "Made in China 2025" plan threaten to reduce U.S. semiconductor market share to as low as 43% from 48%. Further decoupling because of additional U.S. trade restrictions could lead U.S. market share to fall as low as 30% of global sales. For the past five years, China has embarked on a massive fab building plan, but it is struggling to complete all of them – eight facilities out of 30 are not yet fully built out. For China's semiconductor industry to get off the ground, it also needs more local design and engineering talent, but more restrictions have been put on that transfer of knowledge due to continuous technology intellectual property (IP) infringement.

According to an independent study published in March 2020 commissioned by the SIA and conducted by global management consulting firm Boston Consulting Group (BCG), broad unilateral restrictions on Chinese access to U.S. technology could significantly deepen and accelerate the share erosion for U.S. companies. Established alternative non-U.S. suppliers apparently exist already for over 70% of Chinese semiconductor demand. Chinese technology company Huawei has already successfully replaced Micron memory chips with Samsung's. It also claims it can now make 5G base stations, a crucial piece of equipment to

deploy the superfast cellular networks, entirely without U.S.-made parts. HiSilicon, Huawei's chip making subsidiary, is already the largest customer for TSMC's most advanced technology, even beating out Apple. If implemented, the regulations could cost U.S. chip makers about $36 billion in revenue.

Industry Consolidation Will Continue as New Technologies Drive Competitive Edge

As new innovative applications drive current market demand and accelerated time-to-market dictates shorter development cycles, it is safe to predict that industry consolidation is not going to slow down for the foreseeable future despite attempts from governments to block an increasing number of deals in regulatory reviews. In 2019, 44 semiconductor transactions were completed altogether, representing an amount of $27,828 million.

The OSAT sector's forecast CAGR of 6% between 2020 and 2025 alone is propelled by increased demand from automotive sub-systems and connected devices for IoT, thus overtaking the smartphones market that has been in decline due to market saturation. The introduction of 5G is going to bring a new lease of life to the global market. The widespread implementation of IoT devices and AI means that newer chips are being developed by smaller players in the market who lack testing and packaging infrastructure. Chip providers are forced to introduce new products with a short duration. Chip makers are also trying to integrate as many components as possible into a single chip which further drives complexity. These chipmakers are mostly dependent on the OSAT companies as they have limited technical expertise and infrastructure to meet current market demands.

So what should be our take-away from all this? It should be that the issue of the U.S.-China trade war goes beyond the usual "re-shoring, bring manufacturing back to the U.S." policy. It is about maintaining U.S. investments in technology innovation and stating how countries can leverage their expertise to neutralize China's supposed cost advantages. In fact, an entire industry of research, procurement, manufacturing, and logistics expertise has developed over the last 10 to 15 years to do just that – support companies either relocating facilities overseas or seeking ways to blunt the edge rivals have supposedly gained from moving to China.

The SIA/BCG report predicts that dramatic drops in U.S. semiconductor revenue would inevitably lead to severe cuts in R&D and capital expenditures as well as the loss of 15,000 to 40,000 highly skilled direct jobs in the U.S. semiconductor industry. If things comes to the worst, a complete severing of technological ties with China would eventually enable South Korea to overtake the U.S. as world semiconductor leader in just a few years, with China attaining leadership in the long term if it plays its cards right. Let that sink in for a moment. When the stakes are this high, every necessary measure needs to be taken at U.S. leadership level to protect our semiconductor industry. ◆

STEPHEN FOUNDED ATREG IN 2000 to help global advanced technology companies divest and acquire infrastructure-rich manufacturing assets, including wafer fabs (front- and back-end) as well as MEMS, solar, display, and R&D facilities. Over the last 20 years, his firm has completed close to 40% of all global operational wafer fab sales in the semiconductor industry. Recent global acquisitions and sales have involved Fujitsu, GLOBALFOUNDRIES, IBM, Infineon, Matsushita (Panasonic), Maxim, Micron, NXP, ON Semiconductor, Sony, Qualcomm, Renesas, and Texas Instruments to name just a few. Prior to founding ATREG, Stephen established Colliers International's Global Corporate Services initiative and headed the company's U.S. division based in Seattle, Wash.

Before that, he worked as Director for Savills International commercial real estate brokerage in London, UK, also serving on the UK-listed property company's international board. He also spent four years near Paris, France working for an international NGO. Stephen holds an MA degree in Political Theology from the University of Hull, UK and a BA degree in Business Commerce from the University of Washington in Seattle, USA.

SIP-based RF Modules Squeeze More Functionality into Devices

How SIP (System-in-Package) technology enables design engineers to squeeze ever more functionality into ever smaller spaces

Nick Wood, President
Insight SiP

SYSTEM- IN- PACKAGE IS A WAY OF providing a complete system in what looks externally like a single component like a chip in a QFN package. Inside they are increasingly sophisticated systems, which can incorporate semiconductors, passives, and radio frequency (RF) components.

The Evolution of SIP

System- in- package techniques are not new. Initially they were confined to specialist applications like military and aerospace. They first entered the mainstream in the memory market. Most "memory chips" are SIPs with a number of stacked semiconductors.

However, the technology has moved beyond SIPs for memory to far more complex solutions. The mobile phone is increasingly based on SIP technology, as the vendors struggle to meet the twin demands of slim elegant physical design and increasing technological sophistication.

Benefits

What are the advantages of this approach? In comparison with traditional PCB modules, the components are smaller in all dimensions, without compromising performance or adding to the price. And all the traditional advantages of the module approach remain equally true for a SIP module.

Module vs. Discreet Solution

What are the advantages – and disadvantages – of a module approach? Whether to take a discreet component or module approach is one of the key design decisions when including a RF function such as Bluetooth Low Energy (BLE) in a solution.

The disadvantage of the discreet component approach is simple. It comes down to one thing – the unit bill of material (BOM) cost which will inevitably be higher. However, the advantages of the module approach are considerable. Firstly, engineers can completely forget about the analog/RF parts of the design, making only a digital connection to the module. This lowers the time and cost of the design cycle. Perhaps more importantly it reduces risk, as RF is a complex area where it is easy to make mistakes.

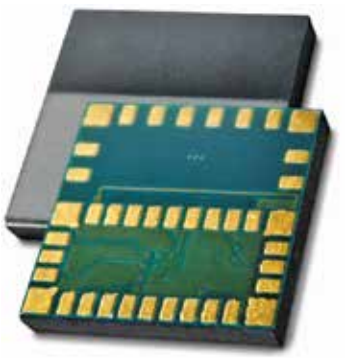


Figure 1. A typical RF module.

Second, the module will normally come pre-certified, removing another time consuming and costly step in the development process.

Lastly, the final procurement and assembly of the end-product is simpler with a pre-tested module replacing a large number of individual components.

In the case of standard SIP modules, it is also unlikely that the customer will be able to design a solution as small as achieving this level of miniaturization without significant research and development effort.

In the end, the choice depends on the particular circumstances of a project. Unless the volumes for a product are going to be very high, several hundred thousand pieces per year, it is unlikely a discreet design will make sense when all factors are taken into account.

Typical Applications

SIP based RF modules, for WiFi Global Positioning System (GPS) or cellular front ends can be found on today's smartphones. Bluetooth Smart modules have been designed into many applications such as temperature measurement (example: STEMP Smart Temperature Patch), gas measurement (example: Microtronics H2S sensor), industrial control (example: Teep-Trak), wearable fitness monitor (example: Arion), Vernier Caliper (example: Sylvac), car park barrier control (example: ComThings) plus many more.

DESIGN CONSIDERATIONS

RF and Antenna Issues

When using typical RF modules, there are very few special requirements apart from being careful to ensure that the antenna area is devoid of metal. As an example, the drawing below indicates the ideal antenna keep-out zone for Insight SiP Smart Bluetooth modules:

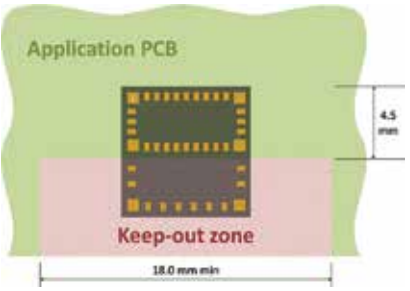


Figure 2. Ideal antenna keep-out zone for a Bluetooth RF module.

Following the above rule will ensure there is a good RF transmission from the PCB. Normally the application PCB will sit in a housing. One has to be careful that there is nothing in the complete solution that will adversely affect the radio connection. Whilst all engineers are aware that you cannot put an RF solution in a metal box, RF interference effects can be subtle.

Early testing of the complete solution is advised.

We are often asked what range can be achieved with our modules. However, most RF products specifications will quote a range under ideal conditions, typically 1m above ground with no obstructions. Most situations are nowhere near as straightforward. For example, any solution that is used close to the human body including a wearable or hand-held solution will significantly reduce the real range. Whilst we can confidently state that our modules and possibly those from others may achieve a range of over 50m in ideal circumstances, it is important to test an application under realistic conditions.

A further aspect of any antenna is the directional performance. If one cannot be sure of how the application device will be oriented, it is important that the antenna has an omnidirectional performance. This is a key design consideration for our Insight SiP RF modules to have a largely spherical radiation pattern. A more directional antenna would be fine if the orientation of the solution is fixed and known, but if not, one could find the solution stopped working under certain conditions. For example, if the system was radiating mainly into the human body instead of into air.

Power Consumption

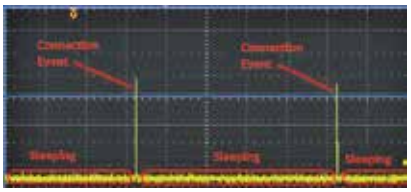
Power consumption for BLE based solutions is another area of concern, as often a key design aim is for the application to run for a long period – months, or maybe even years – off a small coin cell battery.

Unfortunately, it is very hard to give a simple answer to such questions. Vendors often focus on key performance numbers such as peak Rx/Tx current. The reality is that the issue of power consumption is much more complex.

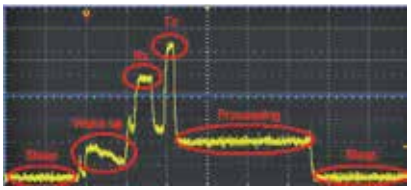
BLE achieves its low power performance by being in a deep sleep state most of the time. When it is a connection state, the transmit and receive cycle are quite short, although these require the highest current. There is also normally a processing cycle, where the radio transmission is off but the processor is active.

The overall power consumption of a solution depends on several factors:

- the frequency of connection required, the speed the chip can wake up,
- the quantity of data transmitted and the length of the transmission cycle, and
- the amount of processing required and the speed of the processor.



Separation of BLE connection events.



Detail within a BLE connection event.

Figure 3. Current power consumption over time.

By looking at the above figures, one can see that peak Rx/Tx current is only one factor in assessing the performance of different BLE solutions, and not necessarily the most important factor.

Optimizing the power consumption is largely a question of designing the application software appropriately. However, it is useful to understand the underlying process to come up with the best design.

A further element related to power consumption is the inclusion of the 32KHz crystal in the solution included in an RF module such as our ISP1507 module. This crystal is not essential for the solution to function correctly, but it does improve power consumption, by improving the timing of the wake-up cycle, and thus maximizing the "sleep" time.

Certification

Whilst certification is not strictly speaking a "design" activity, it is worth mentioning as it is a task that would typically be expected of the engineering department.

Requirements vary according to territory. Normally RF enabled solutions require certification by the relevant national or supra-national body. This involves engaging a third party accredited laboratory to carry out a series of tests to ensure that the RF application is "well-behaved" – i.e. it only radiated in the bands that it is meant to, and at the power levels expected. Of course, if any tests are failed, a re-design is required.

Each product has to be individually certified even if it shares some design aspects with a similar product.

As stated previously, this is an area where a module can save time and money, as modules need to be pre-certified for global markets by the FCC (USA), CE (Europe) and Telec (Japan). In this case, the test process is either not required or vastly simplified. All you need is a reference to the module certification number.

Case Study - ISP150 Module

Our ISP1507 module is an example of how SIP can add significant value to the design process for chipsets requiring RF technology. The ISP1507 is a high-performance multiprotocol module suitable for BLE, ANT+ and NFC-based applications and equipped with an integrated antenna and MCU.

This miniature BLE module by Insight SiP is deployed in two variants to support sophisticated or baseline applications requiring Bluetooth 5 without Long Range connectivity. At 8 mm x 8 mm x 1 mm, the ISP1507 series provide huge computing capability coupled with best-in-class battery life, with power consumption around 20-50% lower than previous generations of technology, making this Bluetooth Low Energy module a ready to use solution for most Internet of Things (IOT) applications.

Getting Started and Support

To accelerate product development and support product developers, your SiP provider should offer a complete development kit together with sample software. Those provided by Insight SIP include everything required out of the box to start developing a solution on day one. This enables the developers to build a complete breadboard using the kit together with external sensor development kits so that software development can proceed in parallel with hardware design.

Not only do SiP modules allow greater functionality using less overall space, they can significantly reduce the development time, cost, and risk of launching a new product. From "off the shelf" functional modules – such as RF modules suitable for BLE-based applications – to fully customized designs they are changing how products are designed and delivered. ◆

Indoor Positioning Technology Takes Center Stage

Enabled by Systems-in-Package (SiP) modules

Nick Wood, President and Chris Barratt, CTO
Insight SiP

RECENT CORPORATE ACTIVITY between major semiconductor vendors and startups has thrust Ultra-Wide Band (UWB) indoor positioning technology onto center stage. What events signaled this new trend? What indoor positioning technology is available to design engineers today? What do these recent moves mean for the technology?

Center Stage

For a long time, this technology had been the preserve of pioneering UWB-focused startups. However, recently the major semiconductor manufacturers have got into the act and highlighted their interest in UWB indoor positioning technology by acquiring or partnering with these startups.

Firstly, Qorvo announced they had purchased Decawave, the UWB chip vendor based in Ireland for $400M. A big success for the team from Ireland. Secondly, Renesas announced a licencing deal with 3db Technologies, the Swiss-based UWB startup. Added to NXP's announcement of a UWB chip and Apple's somewhat cryptic announcement of its "U1" chip, and the picture looks very different to twelve months ago.

Indoor Positioning Technology Today

There has been a long-standing interest in accurate indoor positioning technology, with a wide range of interesting use cases involving the tracking of either people or objects. These include locating assets in a warehouse or other facility, finding people or for sports related data-analysis.

However, the will has not always been matched by the means. The technology has been either too inaccurate to serve the intended purpose or too complex and proprietary to easily put in place. We assume Global Positioning System (GPS) is not feasible or accurate enough.

First, some terminology. It is common in positioning systems to use the term "Tag" to refer to the mobile device that is being tracked and "Anchor" to the fixed points used to form a reference point or grid within which the Tag can be tracked.

Two Technology Options

There are two indoor positioning technology options available today, namely using Bluetooth Beacons or UWB technology.

> Recently the major semiconductor manufacturers have got into the act and highlighted their interest in UWB indoor positioning technology

Simple Indoor Tracking with Bluetooth Beacons

The simplest indoor tracking method uses Bluetooth Beacons, a cheap and widely used technology. These work off simple received signal strength (RSSI) indicators, with position determined by the signal strength measured at one or more anchors.

Nearly everyone carries a Bluetooth device, namely their mobile phone. For objects, a dedicated tag can be easily and relatively cheaply created. Bluetooth has a simple standardised mechanism ("advertising") whereby a device can send out a short message to detect location without complex interaction with the rest of the system.

Lack of Accuracy

The major drawback of such a system is lack of accuracy. The signal strength (or RSSI) is hugely influenced by obstacles between the two points, the relative orientation of the transmitting and receiving antennas and other factors.

In looking at the potential accuracy of locating a Tag worn by a person using Bluetooth RSSI, then consider the effect the human body could have. If we imagine the Tag as a badge pinned to a lapel, the emitted advertising pulse traverses the body in one direction but is freely transmitted through air in the other. Thus, if we consider a person with such a Tag equidistant between two Anchors, the measurements at each anchor will be very different.

Direct transmission through the body might involve an antennation of up to -50 dB. There would probably be transmission round the body or reflection. However, 10 – 20 dB attenuation could be realistic, meaning the two equidistant anchors would infer distances different of up to an order of magnitude.

Even the direct measurement can only be assumed to be within a +/- 3 dB window resulting in an error in the distance estimation of a factor of 2 i.e. "somewhere between x m and 2 times x m".

Angle of Arrival Arrives

To improve accuracy, the Bluetooth Special Interest Group (SIG), has introduced new capabilities with Bluetooth 5.1 including the detection of the angle of arrival of a Bluetooth packet.

This works by having a multiple antenna array in the Anchor and measuring the phase difference of the same signal received at the different antennas, typically separated by a half wavelength i.e. ~ 6 cm.

Figure 1 shows a signal arriving at an angle to the antenna array, assumed to be

sufficiently far away that the paths to the different antenna elements can be parallel lines. Therefore, at right angles to the direction of travel, the signal is in phase.

The accuracy of the angle of arrival estimate is related to 2 fundamental parameters:

- The total width of the antenna array, typically (N-1) * λ/2 where N is the number of linearly spaced antennas
- The accuracy with which the phase of the received signal can be measured for each antenna

The accuracy with which the phase can be measured depends on the precision of the I-Q sampling carried out by the BLE device, which is affected by the internal precision of the I-Q demodulator and the short term frequency drift of the crystal oscillators used in both the tag and the anchor.

In this article we assume that the BLE device can resolve the electrical phase between bursts coming from different antennas with a tolerance of +/- 10° due to the combination of the different error inducing factors.

Geometric calculations indicate that for a 2 antenna array this results in an angular positioning error of +/- 3° close to the axis normal to the antenna plane and +/-5° at 45° relative to the axis.

Similar calculations show that for a 4 antenna array the accuracy of the angle estimation is improved respectively to +/-1° close to the axis and +/-1.5° at 45°.

Assuming a more realistic angle accuracy of +/- 5 degrees, then the accuracy of location is dependent on the distance * tan (5 degrees). So, at 25 m distance, one would have an error of 0.087*25 = +/- 2m. Thus, with multiple anchors, one could expect to localise an object to within a "zone" of 1-2 meters, depending on the distance from the anchor.

UWB-based Indoor Positioning

The other main method of indoor positioning is Ultra-Wide Band (UWB). This method uses a short sharp pulse in the 5-8 GHz range and detects the time of flight between two points, somewhat analogous to an "indoor GPS". In terms of accuracy, such a system is limited by the timing accuracy of the arrival of a pulse. Using the speed of light at 3 x 10**8 m/s, one can calculate that to achieve 1cm accuracy, a timing accuracy of 33 ps is required.

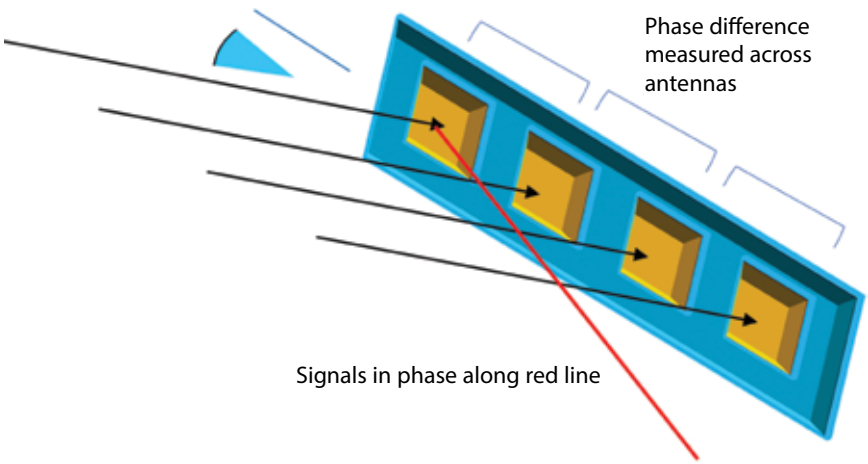


Figure 1. Antenna Array showing signal arriving at oblique angle.

Using only the detected amplitude of the received pulse implies that the accuracy is approximately equivalent to half the pulse width. Since pulse width is directly related to the inverse of bandwidth and UWB systems typically use a 500MHz bandwidth, this technique could achieve an accuracy of the order of 0.5/500 MHz =1ns or 30cm. However, UWB systems use very high frequency sampling of the incoming pulse train and correlation to a known reference train to improve accuracy. Assuming the high frequency sampling captures the phase of the pulse to within +/-45°, the accuracy would be related to ¼ of the carrier frequency period. In the case of 6.5 GHz UWB this implies an accuracy of 0.25/6.5 GHz or 38 ps, equivalent to 1cm positioning precision.

In real case examples the basic repeatability of the receiver is of the order of 130 ps (4 cm) and additional antenna environmental issues allow for an average achieved accuracy of around 10 cm. The disadvantage of such a method is that until now it has been based on closed proprietary technologies, and complex and expensive systems. Real installations require a system to synchronize and keep synchronized the Anchors at high precision. Such systems are not trivial to install.

Gentle Market Awakening

Last year, there were interesting developments in the Ultra-Wide Band ecosystem. The first is that Apple mysteriously announced that the recent iPhone 11 will have a "U1" chip in it with UWB capability. There are almost no details available, but if this was to presage the development of a de-facto standard and a movement to make UWB ubiquitous in the mobile phone, it would be a game changer for the technology. Also notable is NXP becoming the first large silicon player to announce a UWB chip.

There are also intriguing possibilities if, as seems likely with the next generation, UWB devices were to offer an Angle of Arrival capability. This, coupled with accurate distance measurement, would provide the capability to locate an object with reasonably high precision in 2-D from a single anchor. This would significantly simplify the installation of indoor location systems.

In conclusion, indoor positioning technology has a lot of value adding use cases. What has been lacking are solutions that are sufficiently cheap and, perhaps more importantly, easy to install.

Implications of Recent Corporate Moves

As a module vendor of SIP based UWB solutions, amongst other things, we have seen a lot of "slow burn" of interest in the technology, but caution about big deployment. However, announcements from major semiconductor companies such as Qorvo, Renesas, and NXP and electronics giants such as Apple signal a forthcoming acceleration in the development and adoption of UWB indoor positioning technology. Exciting times! ◆

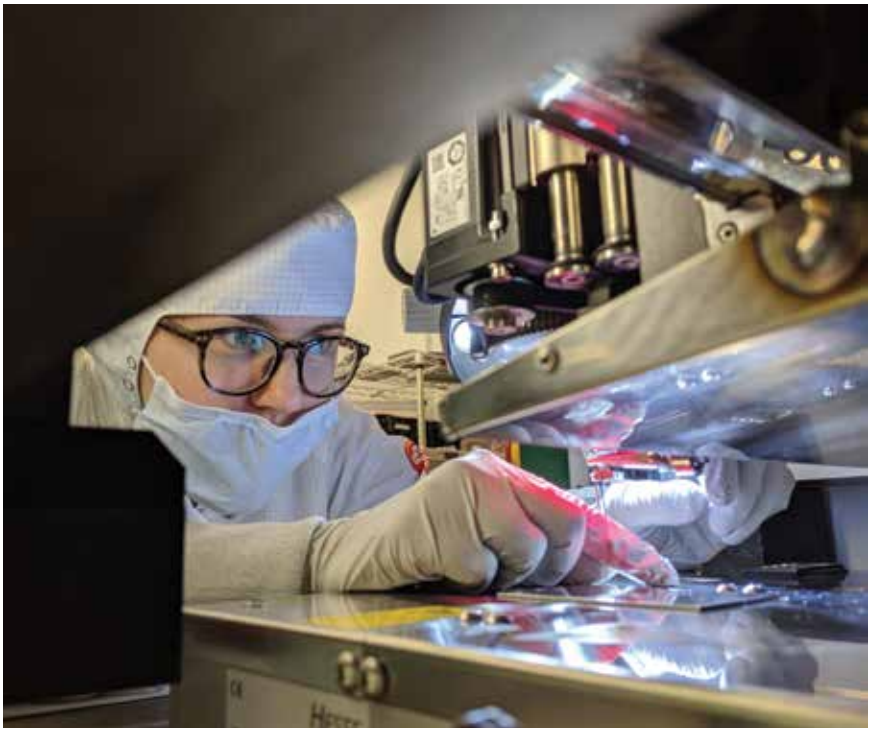
The Concept and Practice of "Concurrent Engineering"

William Boyce
SMART Microsystems Ltd.

A LOT HAS BEEN SAID OVER THE years of the concept of concurrent engineering. There are courses available at engineering colleges and universities that delve into the value of the practice of concurrent engineering. Sometimes it goes by "simultaneous engineering" or "integrated product development (IPD)", but they all refer to the same basic practice. To some, the concept of concurrent engineering implies that once the design is "frozen", the design engineers can engage with the process engineers to begin the task of designing the process to produce the product as designed. To others, it implies that the design engineers have gained input from other engineering groups. To us at SMART Microsystems, it means having a complete team approach from the very beginning of the product design until the product launches.

In a not uncommon organization process flow, the process engineering group will see the design for the first time when the design is "frozen" by the design engineering group. This is when the redesign iterations begin to make the part or assembly compatible with a cost-effective process, or perhaps an existing process. Then, when the process engineering group hands off the modified design to the manufacturing engineering group for review, it is discovered that more iterations are needed to make the design manufacturable. At this point, it is even possible that the design goes back to the initial design group only to discover that the part or assembly no longer meets the original design intent.

You have probably seen these scenarios play out first-hand. Just think of how many iterations you have seen in product concepts that make it out of the design engineering team but cannot be manufactured. Or, think of how many times a "completed" design was not able to be manufactured because the manufacturing folks only saw the design at the end and determined it wasn't able to meet the design-to-cost goal.



With this in mind, it is somewhat funny that when some people hear the words "concurrent engineering", they recoil and think of all the time it will take to get the different disciplines (and people) to agree on anything. They believe that the process will slow to a crawl, and deadlines will be missed. However, in actuality, just the opposite is the case. A fully integrated concurrent engineering development cycle saves time and cost by eliminating costly iterative cycles.

That said, concurrent engineering can be implemented incorrectly and make all the fear of organizational morass come true. Simply gaining random input from other groups is not typically sufficient. Nor is it typically sufficient to only implement concurrent engineering at the beginning or end of product development. Both of these approaches—random input and partial implementation—can lead to confusion, organizational morass, and missed deadlines.

An interactive collaborative approach from beginning to end is always preferable. One effective way to implement concurrent engineering is to take advantage of the very first "concept phase" design review process to integrate different groups and individual ideas. Gaining

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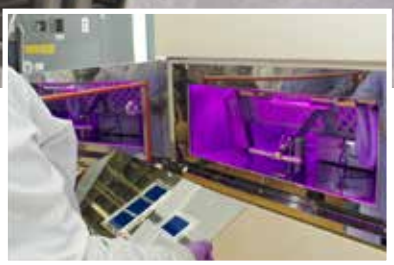

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continued from page 20

valuable insight from as many sources as possible at this early step will help the process get off on the right foot.

So who do we invite? Who are the interested parties? Here is the short list of those that should be considered:

- Design engineering team needs to be present to weigh in on the design intent or customer requirements.
- Program management folks need to be present to weigh in on program timing and design to cost requirements.
- Process engineering team needs to be present to make certain that the design is manufacturable.
- Manufacturing engineering team needs to be present to consider the manufacturing needs once the product is released.

And don't be afraid to invite participants from outside the product development responsibility. Machine operators, technicians, assembly people, even people outside the scope have all attended design reviews with my groups in the past. These team members are not simply placeholders to demonstrate compliance to a design philosophy of concurrent engineering, but need to be full participating members that have valued input and respected as full stakeholders in the outcome.

Very large multidiscipline design corporations have the advantage to implement concurrent engineering because all of the development disciplines are contained within the company. But what about the smaller organizations, ones that do not have the luxury of a design, process, and manufacturing groups within the same reporting structure? What about new product development groups that are start-ups without a formal organizational structure? These smaller groups need to get a little more creative in their design approach if they want to take advantage of the benefits of concurrent engineering. For smaller organizations one possibility is to take advantage of outside entities to take part in the review process.

At SMART Microsystems, we are a process and manufacturing engineering development firm that also performs contract manufacturing for a variety of different firms from the very large corporations to very small startup ventures. We help develop sub-assemblies and complete assemblies for medical, aerospace, and energy sectors to name a few. Sometimes we are asked to take part in the development cycle as a member of the concurrent engineering team during a design review. When the spirit and intent of this time-tested and valued process is recognized and respected by all the team members, the outcome can be very powerful.

For more information visit our website at www.smartmicrosystems.com. ◆

WILLIAM BOYCE is the Engineering Manager at SMART Microsystems. Mr. Boyce earned a Bachelor of Science in Engineering degree from the University of Rhode Island and has served in the field for over 20 years as a mechanical design engineer, process engineer, team leader, engineering Manager, and Global Engineering Director. In addition to his current role at SMART, he has held positions at General Dynamics, Texas Instruments, Sensata Technologies and TT Electronics. Mr. Boyce has also been a member of the IMAPS New England Chapter for over 10 years as a session chair. He is EIT certified, a Six Sigma Green Belt, and an industry recognized expert in Al wire bonding.

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With the demise of Moore's Law due to the economics of advanced semiconductor process nodes, the demand for greater cost performance and differentiation has fueled the development of advanced packaging. Having Known Good Die (KGD) is essential for many, if not all, of the current 'crop' of advanced packaging including 2.5/3D die stacking, Fan-out Wafer Level Packaging (FOWLP), System in Package (SiP), Heterogeneous Integration (HI), and Panel Level Processing (PLP). Not to mention bare die used in modules and on flex-circuits such as chip on board (CoB), chip on flex (CoF), and chip on glass (CoG).

It is clear that the various functional areas that necessary to have KGD have made progress since the first KGD conference in Napa in 1994. For example, electronic design automation (EDA) design for test (DFT) tools are generating much higher levels of test coverage that historically was the case.

However, these efforts in isolation may not be sufficient especially since issues may cross more than one functional area. Or worse changes in one area may exacerbate problems in another. What is missing is a forum that will take a higher level and cross-functional view of the challenges of producing KGD.

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An Industry Under Siege

Bumping elbows…where there are any.

Ed Sperling, Editor in Chief
Semiconductor Engineering

Reprinted with permission from Semiconductor Engineering, March 5, 2020

THE CORONAVIRUS IS TAKING A big toll on the semiconductor industry's unquenchable thirst for new information. The longer it lasts, the more the industry will have to resort to technology — some new, some old — to continue moving forward.

Over the past couple weeks, conferences and trade shows have been postponed or outright canceled. Synopsys, Cadence and Intel pulled out of DVCon at the last minute. And an increasing number of scheduled conferences, such as DATE, have announced they are going virtual.

For those conferences still being held, attendance has been eerily sparse over the past couple of weeks. At the recent SPIE conference in San Jose, the convention center parking lot was so empty it didn't look like a conference was in session. At other gatherings in Silicon Valley, the vast number of seats inside of large ballrooms were unoccupied. And if that wasn't enough to make one question the wisdom of attending, badges handed out at registration often were accompanied by a small bottle of hand sanitizer.

Long-time colleagues this week began greeting each other with an elbow bump rather than a handshake. And anyone coughing was eyed suspiciously and given wide berth.

Amid all of this, the U.S. Centers for Disease Control and Prevention (CDC) issued guidelines for mass gatherings. Some of those are useless. It recommends setting up an emergency operations plan, complete with disposable face masks if someone becomes sick. The only problem is those face masks are unavailable at the moment. The agency also recommends sending out messages discouraging anyone who is sick from attending events. Unfortunately, many sick people are symptomless and contagious, at least in the early stages of the virus.

How long this continues, and what comes next, is far from clear. But for the semiconductor industry, the potential toll is far greater than a short-term revenue loss.

How long this continues, and what comes next, is far from clear. But for the semiconductor industry, the potential toll is far greater than a short-term revenue loss.

Due to rapid changes in technology, keeping track of all of these shifts is essential to remain competitive. Moreover, those changes occur on a global scale, involving the latest process nodes, progress on different ISAs, new security threats, and market-specific changes in assisted driving or advanced packaging.

Obtaining that information electronically is slower, and it doesn't provide the insights that people frequently pick up at conferences. Questions asked at the end of a presentation often are far different from what the presenter has talked about. For the presenters, as well as other attendees, that opens up some interesting new avenues of thought and potentially additional exploration. With this conduit closed off, it certainly will be more difficult to obtain that kind of information, and people will have to work much harder to stay on top of the latest trends and developments.

But the tools do exist for at least keeping up with the basic trends. As long as the infrastructure holds up, and as long as everyone still has phone service, e-mail and Internet access, then sharing of information and across a company, an industry, and the globe is still very possible. And interacting with some remote offices that get very little attention when everyone is scrambling to catch a plane or attend the next conference may have long-term dividends that go well beyond an elbow bump.

So, in case you're wondering what to do while the coronavirus continues to spread, pick up the phone or set up a videoconference with some of your colleagues and customers and suppliers. It may not be as efficient as seeing everyone in one place, but it's a necessary interim step. The learning must still continue, even if it requires more effort. ◆

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ED SPERLING is the editor in chief of Semiconductor Engineering. He is a technology industry veteran and frequent moderator and speaker in Silicon Valley. Sperling is a former contributing editor at Forbes, where he wrote nearly 200 articles about business and technology issues affecting IT and CIOs. He was previously editor in chief of Electronic News and Electronic Business, and before that he held top editorial positions at Ziff-Davis and CMP Publications. Prior to that he was a daily newspaper investigative reporter covering crime and corruption.

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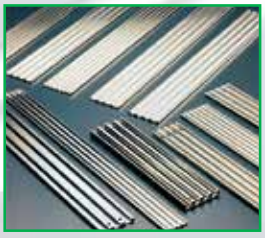
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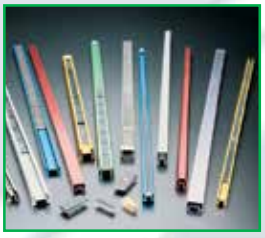
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