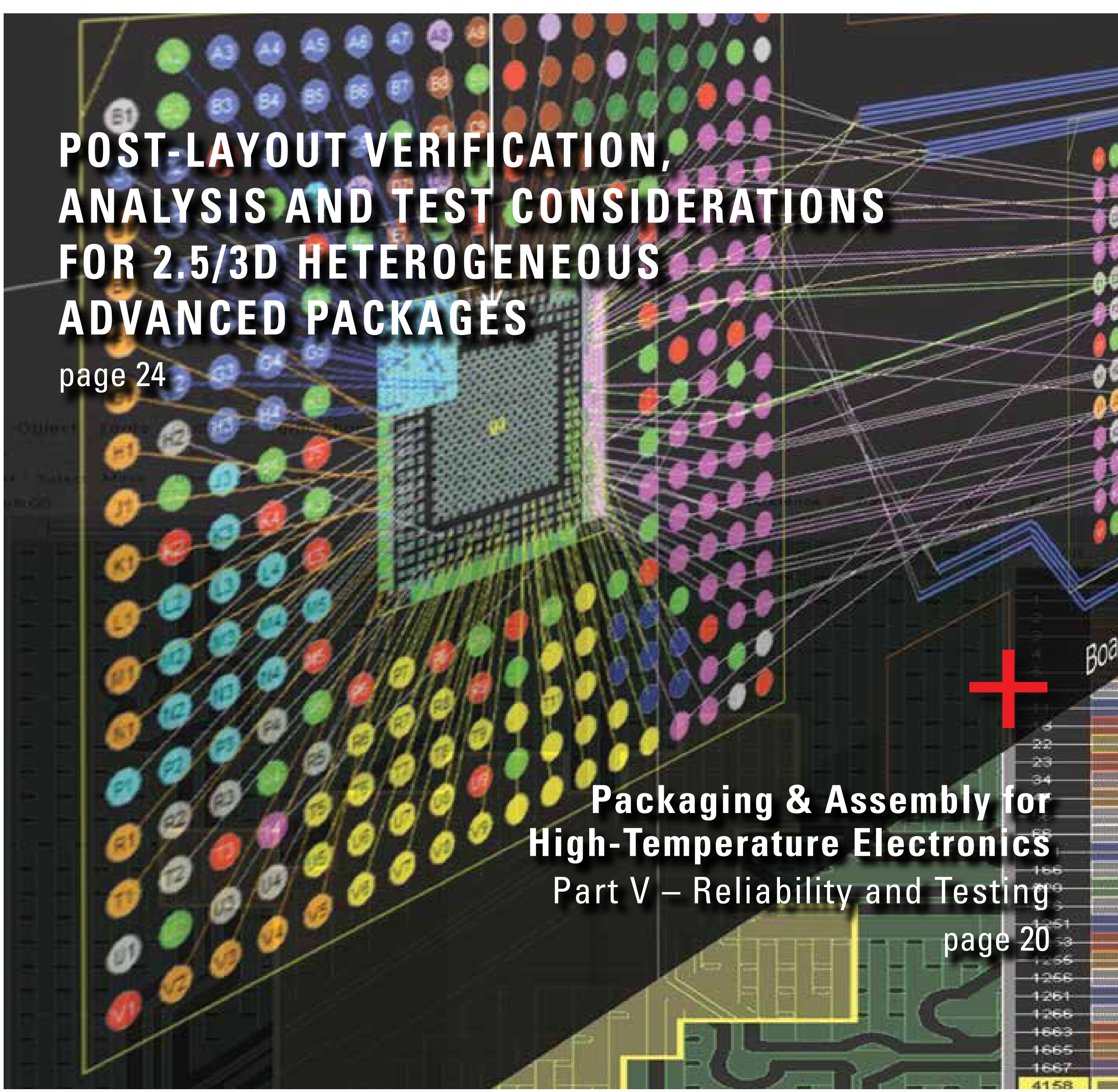
MEPTEC Report

A Quarterly Publication of The Microelectronics Packaging & Test Engineering Council

Volume 23, Number 4

WINTER 2019



POST-LAYOUT VERIFICATION, ANALYSIS AND TEST CONSIDERATIONS FOR 2.5/3D HETEROGENEOUS ADVANCED PACKAGES

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15 They won't replace silicon, but GaN and SiC are becoming much more attractive as prices drop.

28 Binghamton University Professor of Chemistry and Materials Science wins Nobel Prize in Chemistry.

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The MEPTEC Report is a Publication of the Microelectronics Packaging & Test Engineering Council

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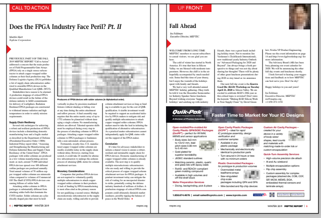
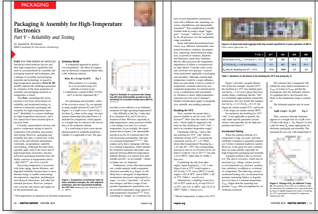


4 CALL TO ACTION – A prudent investment today can mitigate the risk of waiting for an unexpected disaster to strike, potentially costing the defense industry hundreds of millions of dollars. A production stoppage of critical FPGA components could ultimately diminish market readiness, possibly tipping the balance of peace in the World Order.

MARTIN HART
TOPLINE CORPORATION

15 MARKET TRENDS – They won't replace silicon, but GaN and SiC are becoming much more attractive as prices drop. Several vendors are rolling out the next wave of power semiconductors based on gallium nitride (GaN) and silicon carbide (SiC), setting the stage for a showdown against traditional silicon-based devices in the market.

MARK LAPEDUS
SEMICONDUCTOR ENGINEERING

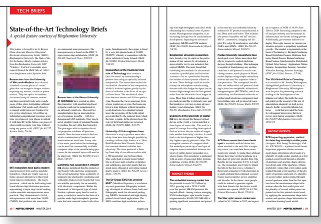


20 PACKAGING – Parts II, III and IV of this series explored the challenges presented by variations of the basic properties of assembly and packaging materials as temperature is raised. This concluding Part presents a few basic observations on reliability and accelerated testing, in relation to electronics packaging and assembly for high-temperature operation.

DR. RANDALL K. KIRSCHMAN
R&D CONSULTANT FOR ELECTRONICS TECHNOLOGY

24 PACKAGING – Heterogeneous packaging is a disruptive impact on traditional design and verification methods. The growth of these designs demands an efficient, proven automated sign-off for physical, electrical, thermal, and manufacturing performance. To ensure consistency and automation a single environment is essential to manage all of these processes.

KEVIN RINEBOLD
MENTOR®, A SIEMENS BUSINESS



28 TECH BRIEFS – The State-of-the-Art Technology Briefs contains articles from the Binghamton University S3IP "Flashes." Binghamton University currently has research thrusts in healthcare/medical electronics; 2.5D/3D packaging; power electronics; cybersecure hw/sw systems; photonics; MEMS; and next generation networks, computers and communications.

BENSON CHAN
BINGHAMPTON UNIVERSITY

DEPARTMENTS

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Does the FPGA Industry Face Peril? *Pt. II*

Martin Hart
TopLine Corporation

PREVIOUSLY, PART I OF THE FALL 2019 MEPTEC REPORT "Call to Action" addressed a concern that the main producers of Field Programmable Gate Arrays (FPGA) rely on a single source subcontractor to attach copper wrapped solder columns as their final production step. The Defense Logistics Agency (DLA) publishes a list of supply chain subcontractors authorized to assemble FPGA devices in the Qualified Manufacturer List (QML-38535).

Stakeholders have reason to be alarmed. A production stoppage of critical FPGA devices could result in the failure of the defense industry to fulfill commitments for delivery of warfighters. Radiation Hardened FPGA packages are constructed to withstand intense radiation and high temperatures in order to satisfy mission requirements.

	CAGE Code	Parent Company
1	1RU44	BAE Systems PLC
2	65342	Cobham plc
3	65786	Cypress Semiconductor, Inc Acquired by Infineon Technologies AG
4	34168	Honeywell International, Inc
5	0J4Z0	Microchip (Microsemi)
6	F7400	Microchip (Atmel)
7	OC7V7	Teledyne Technologies Incorporated
8	01295	Texas Instruments Incorporated
9	68994	Xilinx Incorporated

Producers of FPGA devices with solder columns (in Alphabetical order).

Supply Chain Resiliency

Several risk archetypes for achieving a robust and resilient production of FPGA devices include a diminishing domestic manufacturing base and a fragile market as described in the Department of Defense (Presidential Executive Order 13806) Industrial Policy report titled, "Assessing and Strengthening the Manufacturing and Defense Industrial Base and Supply Chain Resiliency of the United States". FPGA packages with solder columns are produced in a low-volume manufacturing environment; as such, around 75,000 individual FPGA devices spread over 100 different outline packages are produced annually. Total annual volumes of 70 million copper wrapped solder columns are minuscule when compared to volumes of Commercial Off-The-Shelf (COTS) FPGA devices consuming billions of solder balls.

Attaching solder columns to FPGA packages is substantially different from attaching solder balls that dominate the COTS market. Solder columns are cylindrically shaped pins that must be held vertically in place by precision machined fixtures without slanting or falling over at any time during the entire attachment and reflow process. A final assembly step requires that the entire matrix array of up to 1752 columns be planarized without damaging a single column. No manufacturing defects are allowed. Talented operator skills must be employed during every step in the process of attaching columns to FPGA packages. Attaching copper wrapped solder columns to FPGA packages is fundamentally a non-automated, artisan process.

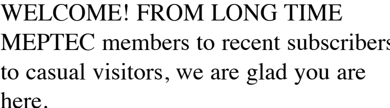
Fortunately, royalty-free, U.S. manufactured copper wrapped solder columns are readily available today in the supply chain without delay. However, starting from scratch, it could take 24 months for alternative subcontractors to undergo the arduous process of attaining QML status for column attachment services.

Monetary Considerations

Companies that produce FPGA devices are not required to voluntarily qualify multiple subcontractors to attach copper-wrapped solder columns to their products. A lack of funding by FPGA manufacturing is most often cited as the primary reason for not qualifying a second source. Multiple microelectronic subcontractors in the supply chain are ready, willing and able to provide column attachment services as long as funding is available to pay for the cost of QML qualification. A sizable investment would be required to support an accelerated initiative by FPGA makers to mitigate risk and qualify multiple subcontractors to attach copper wrapped solder columns. FPGA makers need to take the lead in initiating the qualification of alternative subcontractors. As a practical matter subcontractors cannot independently apply for QML status without the support of the FPGA maker.

Conclusion

It's time for advocacy stakeholders to initiate a shared vision to ensure a robust, resilient and sustainable supply chain for FPGA devices. Domestic manufacturing of copper wrapped solder columns is already available. The next step is to qualify multiple microelectronic subcontractors who are ready and willing to provide the critical process of copper wrapped column attachment services for FPGA packages. A prudent investment today can mitigate the risk of waiting for an unexpected disaster to strike, potentially costing the defense industry hundreds of millions of dollars. A production stoppage of critical FPGA components could ultimately diminish market readiness, possibly tipping the balance of peace in the World Order. ◆



Warming Up to 2020

Ira Feldman
Executive Director, MEPTEC

WELCOME! FROM LONG TIME MEPTEC members to recent subscribers to casual visitors, we are glad you are here.

The cold of winter has started in North America. It's true that here in Silicon Valley we are blessed with moderate temperatures. However, the chill is in the air hopefully accompanied by much needed rain. Some find this time of year dreary, but I enjoy the warmth of the holidays spent with family and friends.

We had a very well attended annual MEPTEC holiday gathering. Okay truth be told it was the December Semiconductor Industry Speaker Series luncheon. Beyond wishing everyone 'happy holidays' and catching up with industry friends, there was a great lunch including holiday treats. Not to mention Jan Vardaman's (TechSearch International), now traditional yearly Industry Outlook on "Advanced Packaging for 2020 and Beyond". Jan always brings a fresh perspective to things and was not shy about sharing her thoughts! There will be plenty of other great luncheon presentations during 2020 so stay tuned as we announce them.

Our next full day event is the **Known Good Die (KGD) Workshop on Tuesday April 21, 2020** in Silicon Valley. We are excited to celebrate KGD's 20th year as this critical topic is revisited! Don't miss the keynote "Making KGD Silicon Work in Your Supply Chain" by David Greenlaw, Nvidia VP Product Engineering. Please see the event information on page 14 and http://www.kgdworkshop.org/ for more information.

The Advisory Board (AB) has been busy planning our event calendar for 2020. We will be announcing the other full day events and luncheons shortly.

I look forward to hearing your suggestions and feedback as to how MEPTEC can best serve you. Don't be shy!

Happy holidays to you and yours!

Ira Feldman
Executive Director, MEPTEC
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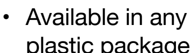

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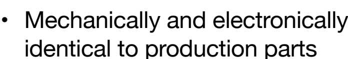

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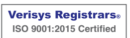


HENKEL APPOINTS NEW CFO

Effective January 1, 2020, Marco Swoboda, Corporate Senior Vice President Finance, will become new Chief Financial Officer of Henkel. He will succeed Carsten Knobel who will take over the position as CEO effective January 1, 2020. “We are pleased to name Marco Swoboda as a highly qualified successor to our Chief Financial Officer from within our organization. He has strong financial expertise with many years of international experience,” said Dr. Simone Bagel-Trah, Chairwoman of the Shareholders’ Committee and the Supervisory Board.

www.henkel.com

MITSUNOBU KOSHIBA OF JSR TO RECEIVE SEMI SALES AND MARKETING EXCELLENCE AWARD

SEMI has announced that Mitsunobu (Nobu) Koshiba of JSR Corporation has won the SEMI Sales and Marketing Excellence Award, inspired by Bob Graham, for 2019. The 22nd recipient of the award, Koshiba was honored for his role in developing and bringing to market multiple photoresist generations that have been critical to the semiconductor industry. He will be recognized during ceremonies at SEMICON Japan 2019, December 11-13, in Tokyo.

www.semi.org

ANALOG APPOINTS DR. SUSIE WEE TO BOARD OF DIRECTORS

Analog Devices, Inc. has announced the appointment of Dr. Susie Wee to the Board of Directors as an independent director, effective November 29, 2019.

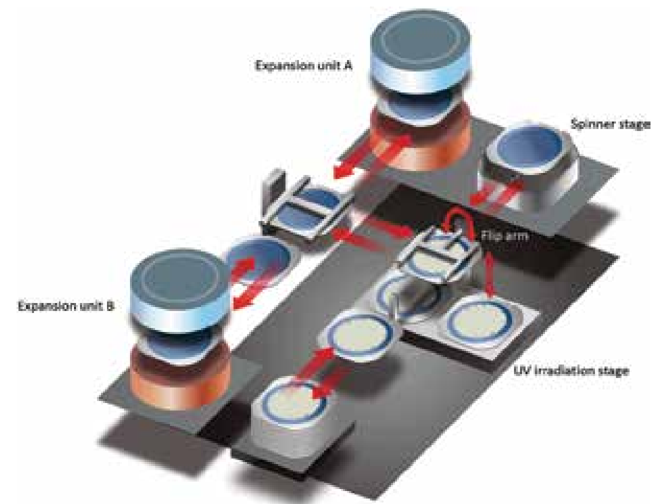
Improved Productivity and Reliability for Thin Memory Chips

Development of DDS2320, Die Separator with Dual Processing Stage

DISCO CORPORATION), A semiconductor manufacturing equipment manufacturer, has developed DDS2320, a fully automatic die separator capable of processing 300 mm wafers that contributes to improved throughput and reliability in memory production. This equipment was exhibited at SEMICON Japan 2019.

Memory demand is expected to increase with the development of IoT, AI, and ADT. As a result, productivity improvement in memory chip manufacturing and improvement of post-processing device reliability will be required more than in the past.

While DISCO had previously introduced the die separator DDS2300 to the market, DD2320 has been newly developed to meet these emergent needs.



Improved Productivity

Efficient production of thin die is now possible due to the adoption of a newly developed expansion unit.

- Cool expansion and heat shrinking in one unit
- Parallel processing with dual expansion unit

Improved Device Reliability Post-Processing

Particle adhesion is reduced by performing processing and transfer after reversing the workpiece, leading to improved device reliability and yield.

- Reverse-side cool expansion / heat shrinking
- Reverse-side spinner cleaning/transfer

Approximately 40% FootPrint Reduction

In previous models, auxiliary equipment was installed in the area around the main equipment. DDS2320 achieves a smaller footprint by having the auxiliary equipment installed internally.

For more information, visit www.discousa.com. ◆

SEMI and VLSI Research Unveil End-to-End Semiconductor Manufacturing Industry Report

SEMI AND VLSI RESEARCH HAVE unveiled the *Semiconductor Manufacturing Monitor*, a report covering the semiconductor manufacturing industry from materials to electronic systems. The inaugural report includes comprehensive 2018 and 2019 quarterly data for the semiconductor manufacturing supply chain, a one-quarter outlook, and semiconductor equipment forecast scenarios to 2020.

“The *Semiconductor Manufacturing Monitor* sets a new standard for semiconductor manufacturing by offering critical insights for making strategic business decisions and investments in our highly dynamic industry,” said Ajit Manocha, SEMI president and CEO. “The combination of SEMI’s leading benchmark data and VLSI Research’s semiconductor manufacturing expertise delivers an unparalleled breadth of market research spanning the entire semiconductor manufacturing supply chain.”

Published four times each year, the annual subscription provides information on:

- Electronic systems sales
- IC sales by logic and memory
- Semiconductor manufacturing CapEx
- Foundry, fabless, OSAT and semiconductor equipment company revenues
- Silicon shipments
- Global wafer fab capacity
- IC inventory

This *Semiconductor Manufacturing Monitor* is ideal for companies requiring cost-effective, comprehensive industry data from trusted sources. Visit www.semi.org to learn more. ◆

nepes Corporation to Acquire Deca Technologies Manufacturing Operations

DECA TECHNOLOGIES IS pleased to announce that it has reached an agreement with nepes Corporation whereby nepes will expand its geographic footprint and manufacturing capabilities by taking over the operations of Deca Technologies Philippines manufacturing facility. The investment will permit the expansion of the WLCSP capacity already in mass production and now offer up to 100,000 wafers per month with a dual site capability courtesy of the Korea site in addition to the Philippines facility.

As part of the agreement, nepes has licensed Deca's M-Series technology to further enable the rapid industry adoption of advanced fan-out technology. Deca's revolutionary M-Series with Adaptive Patterning combined with nepes strong experience in fan-out and large panel manufacturing creates a powerful combination for future growth.

Multiple industry research firms have identified M-Series designed into several Tier One handsets in support of a leader in PMIC applications, further announcements are expected to follow as more customers adopt the technology. Integration of nepes' large panel and SIP capabilities with M-Series and Adaptive Patterning will create multiple exciting customer module solution possibilities including advanced heterogeneous integration.

nepes has manufacturing sites in South Korea and China and international sales offices in San Diego, CA and Shanghai, China. Visit www.nepes.co.kr for more. ◆

NXP Increases Performance and Expands LPC5500 Arm® Cortex®-M33 Microcontroller Series

NXP SEMICONDUCTORS has announced the availability of its LPC552x/S2x Microcontroller (MCU) family – further extending its performance efficient LPC5500 MCU series with the second of seven families planned for the series. The LPC552x/S2x MCU family offers significant advantages for developers, including pin-, software- and peripheral-compatibility to accelerate time to market, while leveraging 40-nm NVM process technology to deliver a cost- and power-efficient microcontroller platform. The LPC552x/S2x is a mainstream family in LPC5500 series, providing a perfect balance between security, performance efficiency and system integration for general embedded and industrial IoT markets. It combines the high-performance efficiency of the Cortex-M33 core with multiple high-speed interfaces, an integrated power management IC, and rich analog integration.

Key features include:

To learn more about the LPC552x/S2x MCU family, visit: www.nxp.com/LPC552x. ◆

Spectrum offers:

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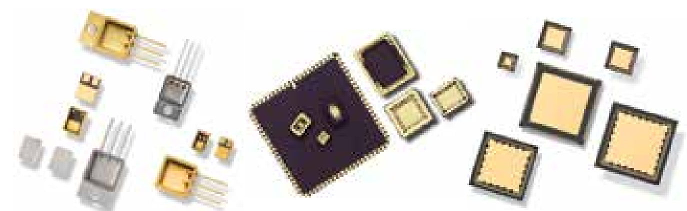

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30 YEARS

Dr. Wee is the Senior Vice President and General Manager of DevNet and CX Ecosystem Success at Cisco Systems and will serve on the Board's Compensation Committee.

"We are pleased to welcome Susie to the ADI Board. Her extensive experience in information technology and application development, together with her established track record of driving software innovation at global technology companies, will be of great value to ADI and our customers," said Ray Stata, ADI Chairman of the Board.

www.analog.com

NORDSON MOVES TO NEW OFFICE AND DEMONSTRATION CENTER IN TOKYO

Nordson Corporation announces that **Nordson Advanced Technology K.K. Japan** has relocated to new, larger office and demonstration facilities in central Tokyo to deliver superior sales, service, technical training, and support to its customers and sales network in Japan. The Nordson Advanced Technology group sells and supports the products from several Nordson divisions (Nordson ASYMTEK, Nordson SELECT, Nordson DAGE, Nordson MARCH, Nordson MATRIX, Nordson SONOSCAN, and Nordson YESTECH) under a unified, in-country team. With the expanded facility, Nordson Advanced Technology K.K. consolidated its fluid dispensing and conformal coating, test and inspection, and plasma treatment equipment into one location. The move was completed in the summer and an opening event was held in October 2019.

www.sonoscan.com

With Sub Micron Accuracy from Lab to Fab

FINETECH'S HIGH-PRECISION placement and assembly systems support customers from the photonics and optoelectronics industry in cost-efficient product development and transfer to automated manufacturing. With the newly introduced FINEPLACER® lambda 2 and the high-yield production platform FINEPLACER® femto 2, the Berlin-based precision machine manufacturer offers integrated equipment and process solutions for all product stages from a single source.

As a manufacturer of micro assembly equipment and process technology, Finetech has been supporting start-ups, as well as global technology leaders, for almost three decades in the development of innovative semiconductor products.

They are the first choice for complex multi-stage assemblies with extremely high accuracy requirements, as well as diverse and very demanding bonding technologies. Applications include the development and production of optical transceivers up to 400 G for data communication, environmental sensors for autonomous driving, or power laser modules for use in industrial and medical applications.

The FINEPLACER® lambda 2 is used to place and connect components with an accuracy of better than 0.5 microns - ideal for the high requirements, e.g. in the development of opto-electronic products such as transceivers (TOSA/ROSA) or laser diode modules.

Thanks to the proven FINEPLACER® alignment and placement principle with only one moving axis, the system combines highest process quality, stability and accuracy. In conjunction with specially developed optical systems with an optical resolutions down to 0.7 μm, it enables superimposed images of the highest optical quality for the reliable detection and alignment of finest structures in the micron range.

For more information, visit www.finetechusa.com. ◆

Mobileye and NIO Partner to Bring Level 4 Autonomous Vehicles to Consumers in China and Beyond

MOBILEYE, AN INTEL COMPANY, AND NIO, a pioneer in China's premium electric vehicle market, are engaging in a strategic collaboration on the development of highly automated and autonomous vehicles (AV) for consumer markets in China and other major territories. As part of the planned cooperation, NIO will engineer and manufacture a self-driving system designed by Mobileye, building on its Level 4 (L4) AV kit. This self-driving system would be the first of its kind, targeting consumer autonomy and engineered for automotive qualification standards, quality, cost and scale. NIO will mass-produce the system for Mobileye and also integrate the technology into its electric vehicle lines for consumer markets and for Mobileye's driverless ride-hailing services. NIO's variants will target initial release in China, with plans to subsequently expand into other global markets.

Under the planned collaboration, Mobileye will provide NIO with the design of the self-driving system building on the Mobileye AV Series, a L4 AV kit comprised of the Mobileye EyeQ® system-on-chip, hardware, driving policy, safety software and mapping solution. NIO will take on the automotive-grade engineering, integration and mass-production of Mobileye's system for both consumer automotive markets and for Mobileye's mobility-as-a-service (MaaS) applications. In addition to integrating the self-driving system into its vehicle lines, NIO will develop a specially configured variant of electric AVs that Mobileye will use as robotaxis, deployed for ride-hailing services in global markets.

Visit www.intel.com for more info. ◆

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MEMBER NEWS

BERND HOPS TO HEAD CORPORATE COMMUNICATIONS AT INFINEON

Infineon Technologies AG has announced that effective January 2020 Bernd Hops, currently Head of External Communications, will take over as Head of Communications and Public Authorities & Associations at Infineon Technologies AG. He will succeed Klaus Walther, who held this position from 2013. In this capacity, Mr. Hops will report to Chief Executive Officer Dr. Reinhard Ploss and have global responsibility for internal, external and political communication.

www.infineon.com

INTEL ACQUIRES ARTIFICIAL INTELLIGENCE CHIPMAKER HABANA LABS

Intel Corporation has announced that it has acquired Habana Labs, an Israel-based developer of programmable deep learning accelerators for the data center for approximately $2 billion. The combination strengthens Intel's artificial intelligence (AI) portfolio and accelerates its efforts in the nascent, fast-growing AI silicon market, which Intel expects to be greater than $25 billion by 2024. Intel's AI strategy is grounded in the belief that harnessing the power of AI to improve business outcomes requires a broad mix of technology – hardware and software – and full ecosystem support. Today, Intel AI solutions are helping customers turn data into business value and driving meaningful revenue for the company. In 2019, Intel expects to generate over $3.5 billion in AI-driven revenue, up more than 20 percent year-over-year.

www.intel.com ◆

Henkel Celebrates Groundbreaking of New Plant in Korea

New High-tech Facility as Global Hub for the Electronics Business

HENKEL HAS HELD THE groundbreaking ceremony for a new production facility in the high-tech industrial cluster in Songdo, Korea. With an investment of more than 30 million euros, the new plant will become a global production hub for the electronics business of Henkel Adhesive Technologies.

The Songdo Plant will have a gross area of 10,144m^2 in a two-story building and will commence full production in Q1 of 2022. The new facility will be designed as a high-tech smart factory including a comprehensive building management system (BMS). In addition, the production facilities will fulfill high sustainability standards and be equipped with the state-of-the-art technologies such as solar energy panels, high-efficiency equipment for energy conservation and securing of green land.

For more information, visit www.henkel.com. ◆

Intel Research Identifies Digital Skills Gap Slowing Industry 4.0

INTEL HAS RELEASED THE RESULTS OF a new study, "Accelerate Industrial," that represents the most comprehensive view of Industry 4.0, the digital transformation of the manufacturing sector. The research uncovered a serious skills gap that most Western industrial production training programs and government investment initiatives fail to address.

The study found that today's leaders need to create tomorrow's future-ready workforce. This requires the collaboration of universities, government and industry – including initiatives that focus on worker training for the transforming manufacturing sector.

A recent Deloitte/Manufacturing Institute study suggests that industries are entering a period of acute long-term labor shortages, with a shortfall in manufacturing expected to be 2.4 million job openings unfilled by 2028, resulting in a $2.5 trillion negative impact on the U.S. economy.

The study uncovered the top five challenges cited by respondents that have the potential to derail investments in smart solutions in the future:

- 36% cite "technical skill gaps" that prevent them from benefiting from their investment.
- 27% cite "data sensitivity" from increasing concerns over data and IP privacy, ownership and management.
- 23% say they lack interoperability between protocols, components, products and systems.
- 22% cite security threats, both in terms of current and emerging vulnerabilities in the factory.
- 18% reference handling data growth in amount and velocity, as well as sense-making.

"Accelerate Industrial" was conducted and authored by Dr. Faith McCreary, a principal engineer, experience architect and researcher at Intel, in tandem with Dr. Irene Petrick, senior director of Industrial Innovation for Intel's Industrial Solutions Division. For more information visit www.intel.com. ◆

COUPLING & CROSSTALK

By Ira Feldman

Electronic coupling is the transfer of energy from one circuit or medium to another. Sometimes it is intentional and sometimes not (crosstalk). I hope that this column, by mixing technology and general observations, is thought-provoking and "couples" with your thinking. Most of the time I will stick to technology but occasional crosstalk diversions may deliver a message closer to home.

Trust Your Paranoia!

PRESIDENT RONALD REAGAN'S use of the Russian proverb "*Doveryai, no proveryai*" was the perfect soundbite to describe the 1987 Intermediate-Range Nuclear Forces Treaty. What does this and Andy Grove's ***"only the paranoid survive"*** have to do with semiconductors?

"Trust, but verify" appears to be a nonsensical phrase since verification implies a lack of trust. However, it accurately describes how models of trust work. The extensive process of verification built into the treaty basically meant there was no trust between the United States and the former Soviet Union. But, as each side performed their commitments in a verifiable manner the treaty worked.

Most people trust something until it no longer works. We hop in our car trusting that the brakes will stop the vehicle when needed. Did you take a moment to inspect the brake pads before driving off? Of course not, unless you already suspected a problem. Did you tell a colleague or friend a 'secret'? Will you continue to share with them? Yes, until that trust is broken and something untoward happens. Cases of "blind trust" rarely end well…

A good engineer, by nature and practice, tends to be skeptical. Usually a project needs to be successful the first time or the cost of failure will be too high. We double-check, we cross-check, and sometimes triple-check our process assumptions as well as the calculations and data. The cost of correcting a small error on a semiconductor mask set can run into the millions of dollars. Some endeavors, like space flight, combine the need for first time success without any failures due to the lives at stake and enormous cost.

My son does not fully comprehend why I insist on checking his math homework with him before he is 'done'. Like most high school students, he thinks he is done after he quickly writes out the answers in his notebook but before we go through to check… He hasn't grasped the value in reinforcing his mastery of the material as he attempts to explain his steps (especially those he failed to write out) nor finding simple calculation errors before turning in his homework. Asking him to detail out all the steps of his calculations is our family's current "trust but verify".

> "Trust, but verify" appears to be a nonsensical phrase since verification implies a lack of trust. However, it accurately describes how models of trust work.

Semiconductor design using modern electronic design automation (EDA) software has extensive process checks to make sure the design is correct. As the process nodes have shrunk to ever smaller sizes, not only has the non-recurring engineering (NRE) costs increased, but the complexity of the physical process also has increased, resulting in more opportunities for design errors and fabrication yield loss. Most modern integrated circuits (ICs) are designed using a high-level description (HDL), examples include VHDL and Verilog, which provides a 'logical' language (think software code) to describe the desired functionality. The design in HDL can be simulated and analyzed to verify the desired operation. At some point the HDL is expressed as an electrical circuit schematic which is also checked and simulated. This circuit schematic is then translated into a physical layout, i.e. the patterns and shapes of the traces to be processed on the IC.

One of the last checks performed before the patterns are written on the masks is "physical verification". At this stage the mask patterns are checked against design rules (minimum feature size, minimum clearances, etc.), electrical checks are performed, and layout versus schematic (LVS) is run. LVS calculates the schematic of the patterns – as generated – and compares them against the input schematics. This makes sure the EDA tools did not create an error by adding extra circuitry, neglecting part of the circuitry, or misinterpreting the circuitry. Yes, ***we trust the tools to operate correctly but it is essential to verify the output to make sure there are no errors.*** Each and every discrepancy needs to be checked carefully to make sure there are no systemic errors or fatal mistakes. Only after the design team is fully satisfied that everything is correct, does the mask data get sent off to generate the physical glass masks.

At the moment the EDA data becomes physical masks is where nature intrudes and physical variations become the difference between failure and success. Just like a film negative, an error in generating the mask or contamination on the mask will cause defects in every IC patterned. Needless to say, mask fabricators very carefully measure and inspect the masks to insure they match the submitted data.

In the actual IC fabrication process itself there are systemic (process "bias") and random defects that will impact the yield of the individual devices. Hence the need for extensive quality control including "metrology" (measurement) and testing to separate the defective devices from those presumed good. I've previously discussed the need for Known Good Die (KGD) and I hope you will join us as MEPTEC discusses the need and ever present challenges at the upcoming KGD Workshop on April 21, 2020.

In addition to a method for finding the good die, what is needed in terms of trust? Beyond the random variations that cause die to fail, how does one ensure there are no 'bad actors' in one's supply chain? Jeff Demmin (Booz Allen Hamilton and MEPTEC Advisory Board member), touched upon this in his MEPTEC-IMAPS Semiconductor Industry Speaker Series luncheon presentation on September 11, 2019.

Today's distributed global supply chain typically has over a dozen entities 'touching' an IC between fabrication and

assembly into an electronic sub-system. Most of these companies are located outside of the US. And there are increasing cases of counterfeit ICs being found due to the economic incentives. With the IC itself it is very difficult and costly to confirm that the actual circuits match those of the design and do not contain changes or extraneous circuitry. Unfortunately, reverse engineering an IC is a destructive process. So, one can never say with 100% certainty that a specific IC being used has not been tampered with.

Combined with no longer having domestic companies that are 'trusted' semiconductor foundries available to build complete devices (especially at advanced process nodes) this creates a challenge for defense related applications. In addition to developing methods for detecting the counterfeiting of or tampering with packaged devices, the Defense Advanced Research Projects Agency (DARPA) is driving the development of Heterogenous Integration (HI) based solutions. Their approach is to use HI 'chiplets' developed and fabricated in secure and trusted facilities for the most 'sensitive' functions. These chiplets can then be integrated with more common building blocks available from the commercial market with less concern as to the level of trust.

So, regardless of one's level of paranoia, processes (as always) need to be established to ensure one's supply chain's quality and security. And the roots of the paranoia expressed by former CEO and Intel co-founder Andy Grove? His biggest concern was that of missing strategic inflection points (SIP) where the fundamentals of the business or available technology have shifted. If a company did not see and respond to these SIP, they may be passed by competitors or left out of a market entirely. Thus, his focus on manufacturing and quality (product and process).

Mr. Grove realized that existing teams have a very large bias towards the status quo. He often used outsiders (other divisions / business units, consultants, etc.) to review things from a fresh perspective. This is similar to having a separate team do the design verification and physical verification of a chip design. Like most audit processes, an outsider may find details overlooked by the those involved in the day-to-day activities.

Bottom line? For any important process, ***even though you may trust that it is being done 'correctly', you must establish an independent 'audit' or checking process.*** Be paranoid and trust, but verify. And do not hesitate to ask for 'outside' help!

For more of my thoughts, please see my blog http://hightechbizdev.com.

As always, I look forward to hearing your comments directly. Please contact me to discuss your thoughts or if I can be of any assistance. ◆

IRA FELDMAN is the Principal Consultant of Feldman Engineering Corp. which guides high technology products and services from concept to high volume manufacturing. He engages on a wide range of projects including technical marketing, product-generation processes, supply-chain management, and business development. (ira@feldmanengineering.com)

COLUMN

INDUSTRY INSIGHTS

By Ron Jones

Changes

I'M A SEMICONDUCTOR GUY, through and through. Always have been, always will be.

I started at Signetics R&D in January 1967 and have been in the industry ever since. To put a finer point on it, I am mostly an assembly/test semiconductor guy. If you scratch me, what will flow out is a mixture of die attach epoxy compound and under fill resin.

My first assembly position was at Texas Instruments in 1970 as a die attach and wire bond engineer on TI's first automated assembly line. A couple of years later I was the first engineering manager on the ABACUS automated assembly line building 14/16 plastic DIPs. I was also the manager for the consolidated military high-rel assembly/test operation in TI's Sherman plant.

I joined Amkor in 1985 and shortly after moved to live in Korea as Corporate VP of Worldwide Operations. I next joined Indy Electronics/Olin Interconnect Technologies in Manteca as president. When that facility was sold, I moved to Thailand as CEO of Thai Microsystems.

When Thai Microsystems was sold, I formed N-Able Group International in 1996 – half of our business has been in consulting or recruiting for the semiconductor assembly test arena.

I began my association with MEPTEC in 1990. That is when I first met Bette Cooper and later Gary Brown. We have worked on a number of things together over the years:

- I have attended many, many MEPTEC meetings.
- I joined the advisory board in 1997 and transitioned off in 2010 when the board was scaled down.
- I began writing a column for the MEPTEC Report in 1998 and continue to do so today.

During those many years I've gotten to know Bette and Gary very well. They epitomize semiconductor assembly and test as much as anybody I know. They are knowledgeable, honest and ethical and would do anything in the world for you.

They have provided a real service to the semiconductor assembly and test segment of our industry. The MEPTEC luncheons are a great opportunity for members of our segment to get together, talk shop, and just catch up on being friends. The MEPTEC symposiums are a great way to stay up on industry trends that are taking place in our market.

> Technology has certainly changed during my 53 years in the industry. When I began, we were on one-inch wafers and now twelve-inch wafers are typical.

One thing about the semiconductor industry is that there is always change. For Bette and Gary, they moved from Silicon Valley to Medicine Park, OK, then to the Charleston, South Carolina area.

Technology has certainly changed during my 53 years in the industry. When I began, we were on one-inch wafers and now twelve-inch wafers are typical. Then geometries are measured with a yardstick and they are now down in the deep submicron range. A typical device used to be seven masking levels and now it's not unusual to have devices with 50 levels. For all these changes, the typical process steps are spin, expose, develop, etch, deposit/implant, oxidize… Rinse and repeat.

On the other hand, some things never change. Bette and Gary are the same responsible, conscientious, ethical people they have been over the decades that I have known them. In my opinion, the MEPTEC Report is one of the most professionally done industry magazines I have run across, and Gary is one of the most talented graphic artists I know of.

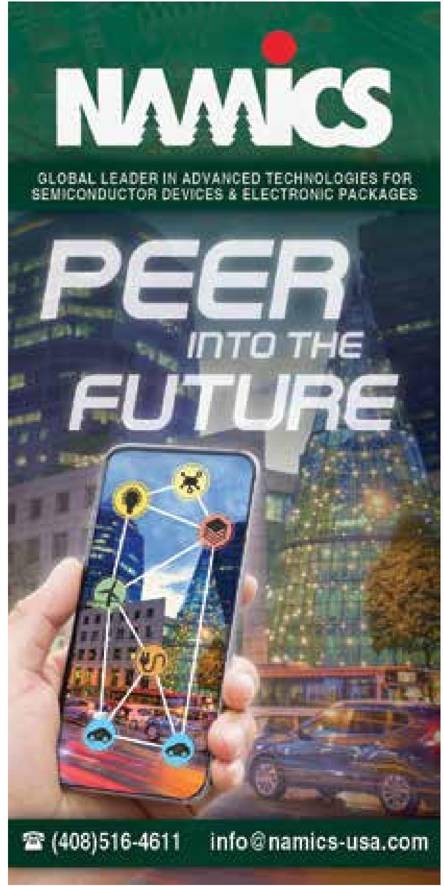
Working with them is a combination of collaboration and Saturday Night Live. Every e-mail contains a zinger of some sort in both directions. You can say whatever you want without fear that it will be taken the wrong way. They are both witty and more than willing to fire salvos but at the same time more than willing to take incoming fire. When I see an incoming email from either of them, I know there'll be something in it to laugh about and the opportunity to fire back.

For many years they have offered a real and valuable service to our industry and have always done it with integrity, honesty and openness.

Some things never change.

This article is not about me, but merely to establish my bona fides as somebody that understands the assembly, packaging and test arena and who has dealt with Bette and Gary for many years. We are lucky to have them providing this service for us and I don't think it would be out of line to say thank you next time you communicate with them. ◆

RON JONES is CEO of N-Able Group International (NGi); a semiconductor focused consulting and recruiting company. N-Able Group serves clients in the Americas, Asia and Europe. NGi supports the semiconductor supply chain including fabless and IDM semiconductor device companies, wafer foundry and OSAT providers, materials and equipment suppliers, software companies and investors. Email ron.jones@n-ablegroup.com for more info.



KNOWN GOOD DIE WORKSHOP 2020

Tuesday, April 21, 2020

SEMI Global Headquarters, Milpitas, California

With the demise of Moore's Law due to the economics of advanced semiconductor process nodes, the demand for greater cost performance and differentiation has fueled the development of advanced packaging. Having Known Good Die (KGD) is essential for many, if not all, of the current 'crop' of advanced packaging including 2.5/3D die stacking, Fan-out Wafer Level Packaging (FOWLP), System in Package (SiP), Heterogeneous Integration (HI), and Panel Level Processing (PLP). Not to mention bare die used in modules and on flex-circuits such as chip on board (CoB), chip on flex (CoF), and chip on glass (CoG).

It is clear that the various functional areas that necessary to have KGD have made progress since the first KGD conference in Napa in 1994. For example, electronic design automation (EDA) design for test (DFT) tools are generating much higher levels of test coverage that historically was the case.

However, these efforts in isolation may not be sufficient especially since issues may cross more than one functional area. Or worse changes in one area may exacerbate problems in another. What is missing is a forum that will take a higher level and cross-functional view of the challenges of producing KGD.

This event will bring together experts to cover topics such as:

- Metrology and Inspection
- Test and Handling
- Big Data and Analytics
- Business Model
- EDA and CAD Tools

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For questions about event attendance, sponsorships, or exhibiting, please email Susan Kinne **susan@meptec.org**.

FOR MORE INFORMATION AND TO REGISTER ONLINE TODAY GO TO KGDWORKSHOP.ORG

Power Semi Wars Begin

They won't replace silicon, but GaN and SiC are becoming much more attractive as prices drop

Mark LaPedus, Executive Editor for Manufacturing
SEMICONDUCTOR ENGINEERING

Reprinted with permission from SEMICONDUCTOR ENGINEERING, October, 23, 2019

SEVERAL VENDORS ARE ROLLING out the next wave of power semiconductors based on gallium nitride (GaN) and silicon carbide (SiC), setting the stage for a showdown against traditional silicon-based devices in the market.

Power semiconductors are specialized transistors that incorporate different and competitive technologies like GaN, SiC and silicon. Power semis operate as a switch in high-voltage applications such as automotive, power supplies, solar and trains. The devices allow the electricity to flow in the "on" state and stop it in the "off" state. They boost the efficiencies and minimize the energy losses in systems.

For years, the power semi market has been dominated by silicon-based devices, namely power MOSFETs and insulated-gate bipolar transistors (IGBTs). Both are mature and inexpensive, but they are also reaching their theoretical limits in several respects.

That's where GaN and SiC fit in. In the market for years, GaN and SiC devices compete against IGBTs and MOSFETs in various segments. Both GaN and SiC are wide-bandgap technologies, meaning they are faster and more efficient than silicon-based devices.

Still, GaN and SiC devices have relatively low adoption rates and won't displace their silicon rivals anytime soon. Today, silicon-based devices have more than 90% market share in the overall power semi market, according to Yole Développement. Generally, GaN and SiC devices are expensive technologies with various challenges.

That's beginning to change because new GaN and SiC devices are making a bigger dent in the market. SiC, for example, is growing at a double-digit pace, compared to single digits for silicon-based devices, according to Yole. "The silicon carbide power device market is expected to grow very fast, driven mainly by the automotive market," said Hong Lin, an analyst at Yole. "The market potential is huge and is attracting a lot of players. We expect the competition to be very strong in the coming years."

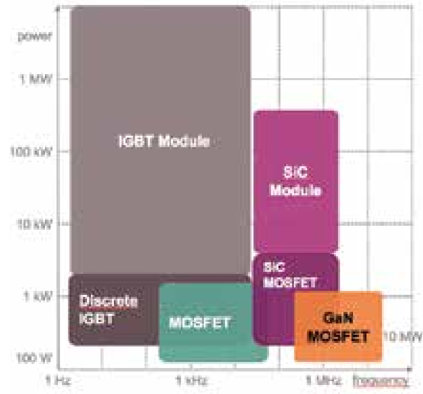

Figure 1. How power switches are categorized. *Source: Infineon*

GaN is a tiny market today. "When we calculate the growth rate in five years, GaN could be really much bigger than silicon carbide and IGBTs. The market could grow very fast," Lin said.

As it turns out, though, there is no one power semi that fits all needs. There is a place for all technologies. "The total market is growing very quickly. Every device can still have their place, at least for the foreseeable future," Lin said.

Nonetheless, there are a number of events taking place in this market. Among them:

- Cree, Rohm and others are increasing their capital spending and building new SiC fabs. Vendors are preparing for huge demand in the battery-electric car market.
- Automotive OEMs are securing supply deals with SiC device makers to meet demand.
- Efficient Power Conversion (EPC), a supplier of GaN power semis, is making what it calls a "frontal assault" against power MOSFETs. GaN is making inroads in various systems.
- Equipment vendors are seeing an uptick in demand in compound semi fabs.

In total, the power device market is expected to grow from $17.5 billion in 2018 to more than $21 billion by 2024, according to Yole. Of that, the SiC device market will grow from $420 million in 2018 to $564 million in 2019, according to Yole. In 2018, the GaN device market was less than a $10 million business, according to the firm.

The End of Silicon?

In total, the world generates 12 billion kilowatts of power every hour, according to North Carolina State University. More than 80% of the world's electricity is transported through a power electronic system, according to the school.

Power electronics make use of various devices that control and convert electric power in systems, such as cars, motor drives, power supplies, solar and wind turbines.

Generally, power is wasted during the conversion process in systems. In one example, the power wasted in desktop PCs sold in 1 year is equivalent to 17 500MW power plants, according to NC State.

Therefore, the industry requires more efficient devices, such as power semis and other chips. Each power semi is denoted by a numerical figure with a "V" or volt-

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age. "The 'V' as in VDSS is the maximum allowed operating voltage, or drain-source voltage specification," explained Alex Lidow, chief executive of EPC. "The terminology 'DSS' means drain-to-source with the gate shorted."

Nonetheless, there are several power semis to choose from. On the silicon front, the choices include power MOSFETs, super-junction power MOSFETs and IGBTs.

Considered the least expensive and most popular device, power MOSFETs are used in adapters, power supplies and other products. They are used in lower-voltage 10- to 500-volt applications.

Super-junction power MOSFETs, which are souped-up MOSFETs, are used in 500- to 900-volt systems. Meanwhile, the leading midrange power semiconductor device is the IGBT, which is used for 1,200-volt to 6.6-kilovolt applications.

MOSFETs compete against GaN devices in the lower voltage segments, while IGBTs and SiC go head-to-head at the high end. All devices compete with one other in the 600- to 900-volt range.

Regardless, IGBTs and power MOSFETs will remain the mainstream technologies for the foreseeable future. "Silicon is a very mature technology, leading to better cost positions in many aspects, including from a supply chain and internal production processes to existing designs and processes at the customer side," said Gerald Deboy, a senior principal at Infineon. "This is why for many applications silicon-based power switches will continue as the preferred technology for many years."

Silicon-based devices, however, have several limitations, such as high conduction losses and low switching frequencies. Conduction loss is due to the resistance in the device.

That's why OEMs are interested in two wide-bandgap technologies—GaN and SiC. Silicon has a bandgap of 1.1 eV. In comparison, SiC has a bandgap of 3.3 eV, while GaN is 3.4 eV.

"GaN and SiC are wide-bandgap materials, which means higher bonding energy of the atoms in the crystal," said Steven Liu, vice president of corporate marketing at UMC. "SiC and GaN are promising components for the power semiconductor market due to the higher efficiency and smaller form-factor characteristics, compared to their silicon-based peers. The devices can be made much smaller in size for the same relative voltage and current handling capability."

GaN and SiC power semis have been shipping for some time, but they are still expensive. "The manufacturing cost is the main obstacle to market growth, since today both are mainly still using 6-inch and below wafers for production. Once the cost can be improved to a certain threshold, the market size could explode," Liu said.

SiC and GaN are promising components for the power semiconductor market due to the higher efficiency and smaller form-factor characteristics.

Still, there is a place for all power semi types, according to Infineon. Infineon has a unique perspective, given that it sells IGBTs, MOSFETs, GaN and SiC.

"Criteria for selection of a wide-bandgap device instead of traditional silicon depends on balancing system cost and performance requirements for particular applications," Infineon's Deboy said. "There are various applications where a tipping point in cost and performance goals has been reached for systems based on wide bandgap material. Depending on the specific application, GaN or SiC devices have a better cost position at the system level, even while the GaN or SiC device itself is more expensive than the silicon alternative."

What is SiC?

The SiC market is heating up. Suppliers of SiC devices include Cree/Wolfspeed, Infineon, Mitsubishi, On Semiconductor, STMicroelectronics, Rohm and Toshiba.

SiC is a compound semiconductor material based on silicon and carbon. It has 10 times the breakdown field strength and 3 times better thermal conductivity than silicon.

There are two SiC device types—SiC power MOSFETs and diodes. SiC power MOSFETs are power switching transistors. A diode passes electricity in one direction and blocks it in the opposite direction.

SiC devices are produced in 150mm fabs today, although 200mm is in R&D. In the production flow, a SiC substrate is developed. An epitaxial layer is grown on the substrate. It is then processed into a device.

Making the substrate is the biggest challenge. "This wider bandgap gives the materials interesting qualities such as faster switching and higher power density," said Llewellyn Vaughan-Edmunds, director of strategic marketing at Applied Materials, in a blog. "A major challenge is substrate defects. Basal plane dislocations and screw dislocations can create 'killer defects' that must be reduced for SiC devices to achieve the high yields required for commercial success."

The issues with the SiC substrate translates into higher costs and potential supply constraints during boom cycles. "Cost is a challenge versus silicon or even GaN-on-silicon approaches. There are two main reasons—the cost of the SiC substrate and the material yield. Given the tight supply conditions, those prices are unlikely to start dropping soon, but the situation will improve," said Kevin Crofton, president of SPTS Technologies and senior vice president at KLA.

To address the cost issues, some vendors are working on 200mm SiC fabs. This will increase the die per wafer, thereby reducing the cost.

Meanwhile, SiC MOSFETs are based on two structure types—planar and trench. Planar incorporates a traditional source-gate-drain structure. Trench forms a "U shape" vertical gate channel.

"At the device level, first and second silicon carbide MOSFET generations based upon planar technologies are now well established, but scaling of these technologies to reduce cost and improve performance is technically challenging," said David Haynes, senior director of strategic marketing at Lam Research. "Trench-based silicon carbide MOSFETs offer the potential to overcome this scaling barrier

for key applications in electric vehicles and hybrid electric vehicles, but the performance and reliability of these devices still must improve to address a broader range of automotive applications."

In both cases, suppliers are striving to make good parts with a low on-resistance. This involves unwanted resistance between the source and drain. "My goal is to make every generation with a lower specific on-resistance," said John Palmour, CTO of power and RF at Cree. "It also has to be reliable."

SiC-based devices, meanwhile, are used in 600-volt to 10-kilovolt applications. At the high end, some sell 3.3- to 10-kilovolt devices, which are used for power grids, trains and wind power.

The big market for SiC falls in the 600- to 1,200-volt range. For this, battery-electric cars are the biggest market, followed by power supplies and solar.

For years, electric-vehicle OEMs used IGBTs and MOSFETs in many parts of the vehicle. Then, instead of using IGBTs, Tesla began using STMicroelectronics' SiC power devices for the traction inverter within its Model 3 car. The traction inverter provides traction to the motor to propel a vehicle. SiC devices also are used for the DC-to-DC converter and on-board charger in electric cars.

Other OEMs are also evaluating or using SiC. "The performance of silicon carbide provides higher efficiencies. That allows you to go further on a battery charge or reduce the battery, which is the most expensive part of the vehicle," Palmour said.

Each electric car vendor has different requirements. "We refer to it by bus voltage. A standard bus voltage would be 450 volts. If you have a 450-volt bus, you would use a 650-volt power transistor. Some people are also looking at using an 800- or 850-volt bus. There, you would use a 1,200-volt transistor," Palmour said. "Some people are looking in between. We are having discussions with people about 650, 900 and 1,200 volts."

Some OEMs will use SiC. Others may stick with IGBTs due to cost. "The cost is still a challenge and competition from proven silicon-based IGBT solutions will be a reality for some time to come," Lam's Haynes said. "At the integrated power module (IPM) level, SiC can win out. Indeed, a SiC power module can deliver significant cost benefits versus all silicon-based IPMs or indeed hybrid IPMs in a smaller form factor. However, at the device level, IGBTs are still substantially cheaper than SiC MOSFETs and have proven performance and reliability, as well as being established in the automotive supply chain. As a result, it is likely that IGBT and SiC technologies will coexist for many years."

One expert summarized the situation with SiC. "If you look at Japan, they are making 3.3-kV SiC MOSFETs. They have a massive rail infrastructure there," said Victor Veliadis, executive director and CTO at PowerAmerica, a Manufacturing USA institute that is accelerating the development of wide bandgap semiconductor technology.

> GaN and SiC are taking off. These devices give engineers some new and different options. But they won't displace silicon.

"1,200 and 900 volts are automotive. That's the biggest application for SiC," Veliadis said. "If you look where silicon carbide is going, it started at 1,200 volts, which is far from where silicon is competitive. Now, it's trying to work it's way down and trying to get market share in the 900- and 600-volt range.

"If you go to 600 volts, and you look at everything silicon does, SiC will likely do it more efficiently. There are obstacles when you go to a lower voltage. At 600 volts, silicon is still relatively efficient because of the infrastructure. It's very cheap. When you go to 1,200, it's very expensive to do it with silicon," he said.

Going, Going GaN

Meanwhile, GaN, a binary III-V material, has 10 times the breakdown field strength with double the electron mobility than silicon.

GaN is used for LEDs, power electronics and RF. The RF version of GaN is used in 5G, radar and other applications. GaN power devices, which are different, are used in power switching apps. EPC, GaN Systems, Navitas, Panasonic, Transphorm and others sell GaN power devices.

These devices are made on 150mm wafers. Many suppliers have their devices produced on a foundry basis by Episil and TSMC.

In EPC's GaN flow, a thin layer of aluminum nitride (AlN) is deposited on a silicon substrate. A GaN layer is grown on the AlN layer. A source, gate and drain are formed on the GaN layer.

"From a technical perspective, GaN remains less mature than SiC," Lam's Haynes said. "If one considers GaN-on-silicon HEMT (high electron mobility transistor) technologies, yield remains a concern because of the quality of GaN MOCVD growth on silicon. There are also still challenges associated with device performance and reliability."

That's not the only issue. "Wafer breakage caused by wafer bow is still an issue for this technology," KLA's Crofton said. "The plasma processes are also required to be very low energy because of concerns about plasma-induced device damage. Equipment makers are striving to make their reactors sufficiently benign to the device."

On the device front, meanwhile, GaN semis are targeted for different markets. EPC and others compete in the lower voltage segments from 15 to 200 volts. In these segments, GaN competes against power MOSFETs.

Others compete in the 600-, 650-, and 900-volt markets. These devices compete against IGBTs, MOSFETs and SiC.

One company, EPC, is expanding its efforts in the low-voltage GaN arena. "It was only about a year ago that EPC did what I call a frontal assault on silicon MOSFETs —and we did that at the 48-volt node," EPC's Lidow said. "GaN, at least from EPC, is not only higher performance than MOSFETs, but we also priced it right at MOSFET prices."

Indeed, there are some changes taking place in the 48-volt market in automotive, data centers and other segments.

For example, data centers consist of a multitude of servers, each of which are housed in a cabinet or rack. The power is distributed in the backplane of the rack

using rack-mounted power supplies.

In the data center, AC voltage is generated and fed into the server racks. The power is then converted into a lower voltage. At one time, the racks used 12-volt power supplies. Over time it became inefficient to distribute the power at 12 volts because it caused an increase in power consumption and losses for servers in the data center.

So in 2011, Facebook and others formed the Open Compute Project (OCP). As part of its efforts, OCP pushed for a 48-volt power rack distribution spec, which is more efficient and also reduces power.

"In the past, you would have 12 volts coming onto the board. It would go to a point-of-load converter, and that would convert from 12 volts down to the voltage needed by the microprocessor. But it took a lot of real estate, and it wasn't efficient," Lidow said. "Now, they're bringing the 48 volts onto the server board. And in one big step, they are going all the way down to like 5, 4 or 3 volts. They are using GaN to do that."

In 12-volt backplanes, some OEMs used 40-volt power MOSFETs, according to a blog from GaN Systems. At 48 volts, OEMs are forced to use 100-volt MOSFETs, but these are less efficient, according to the company.

OEMs also have the option to use 48-volt DC-DC converters based on GaN devices. "They are smaller, cheaper and more efficient. And the dominant topology is something called an LLC topology. And these things are tiny and 98% to 99% efficient," Lidow said.

Besides servers, GaN is targeted for other 48-volt apps. "It's coming in on automotive. Instead of having a kilowatt of electrical load, they're going up to 6 and 8 kilowatts. So they're going to 48-volt systems. And they're going to GaN," he said. "Robots are going to 48 volts for similar reasons. So there are different marketplaces feeding off each other in the advances in GaN."

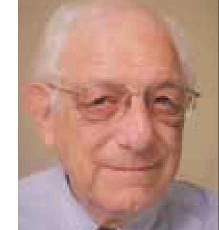
GaN, meanwhile, is gaining traction at the 600-, 650- and 900-volt markets, especially the consumer adapter market and other systems. "GaN is making inroads into areas where silicon performance is simply not acceptable," said Primit Parkih, chief operating officer at Transphorm. "As GaN prices decrease, GaN will continue to chip away at the current market."

For 600 and 650 volts, GaN is targeted for adapters, automotive and power supplies. At 900 volts, GaN is targeted for automotive, battery chargers, power supplies and solar. Like SiC, GaN is trying to get more traction in electric vehicles, especially for on-board chargers and DC-to-DC converters.

Conclusion

Clearly, GaN and SiC are taking off. These devices give engineers some new and different options.

But they won't displace silicon. It's difficult to replace a familiar technology in mission-critical products. ◆



Packaging & Assembly for High-Temperature Electronics

Part V – Reliability and Testing

Dr. Randall K. Kirschman
R&D Consultant for Electronics Technology

PART I OF THIS SERIES OF ARTICLES introduced semiconductor devices and their high-temperature capabilities that must be accommodated by assembly and packaging materials and techniques, plus a glimpse of assembly and packaging materials and technology in regard to high-temperature operation. **Parts II, III** and **IV** explored the challenges presented by variations of the basic properties of assembly and packaging materials as temperature is raised.

This **Part**, concluding this series, presents a few basic observations on reliability and accelerated testing, in relation to electronics packaging and assembly for high-temperature operation[1]. Reliability is a serious challenge for high-temperature electronics, and a few aspects have been touched upon in previous Parts.

Certainly, semiconductor devices and passive components spring to mind in connection with reliability and accelerated testing. However, packaging and assembly also play a critical role, in the form of die and substrate attachments, wirebonds, encapsulation, underfill, and molding. (Although the latter three typically apply only to the lower end of high-temperature electronics, because polymeric packaging materials raise reliability concerns at temperatures above ≈200–250°C[2]. *(See Parts I and II)*

Increasing temperature is associated with faster aging, shorter lifetimes, and degraded reliability because there is more thermal energy to enable restructuring, decomposition, migration, metallurgical and chemical interactions, and other detrimental processes. However, temperature is not the only factor, and might not be the predominant one.

Arrhenius Model

A widespread approach to predict—via extrapolation—the effect of temperature on electronic component failure rates is the Arrhenius relation:

$$\textbf{Rate, } R = A\cdot\exp(-E_a/kT) \qquad \textbf{Eq. 1}$$

Where prefactor A is a constant,
E_a is an associated energy (eV) called the *activation energy*,
k is Boltzmann's constant (0.862e–4 eV/K),
and T is *absolute* temperature (K).*

For packaging and assembly, values of the *activation energy*, E_a, are reported to range roughly between 0.5 and 2 eV[3][4]. Figure 1 is a *logR-versus-T* plot of Eq. 1 for three E_a values in this range. An exponential relationship (described below) is included for comparison, which appears as a straight line in contrast to the curved lines of the Arrhenius relation.

It is comforting to have some uncomplicated guide for reliability prediction—whether it is applicable or not. The question then is how effective is an Arrhenius treatment for high operating temperatures?

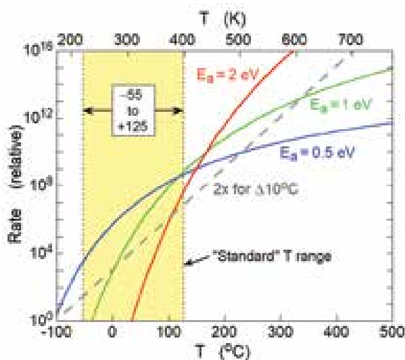


Figure 1. Comparison of Arrhenius rates for three activation energies, E_a, with adjusted prefactors, plus the exponential *doubling-for-10°C* line (dashed gray line, arbitrarily set to 1 at –100°C).

Figure 2. Example of a process rate changing with time (intermetallic growth in Au-Al wirebond) at a constant temperature (200°C) Data from [5].

One difficulty is that Eq. 1 states that R is a function of E_a and T; but not a function of time. However, especially at high temperatures, many processes exhibit a *rate* change over time at a *constant* temperature. As an example, the experimental data in Figure 2 for intermetallic growth in an Au-Al wirebond show the rate decreasing considerably with time at a constant temperature Data from [5]. This implies an E_a that is changing with time at a constant temperature, which muddies the Arrhenius treatment and makes comparisons between different temperatures difficult. Besides, it is unclear how intermetallic growth—as an example—relates to failure rate via Arrhenius.

Furthermore, as has often been pointed out, a multi-material, multi-component electronic assembly (e.g. Figure 3) will likely have a menagerie of degradation mechanisms (processes) represented by a range—or even a "spectrum"—of activation energies, and thus a range of temperature dependencies, particularly over an extended temperature range typical of high-temperature electronics[6][7][8]. Even something as "simple" as a wirebond can

*All temperatures in equations are absolute temperatures.

have several degradation mechanisms, each with a different rate: annealing, corrosion, interdiffusion, and intermetallic formation[9]. This complication is usually brushed aside by using a single "aggregate," "average," "effective" or "global" E_a for all processes over the temperature range considered.

Some individual physiochemical processes, (e.g. diffusion, intermetallic compound formation, oxidation, decomposition, outgassing, electrochemical migration, or growth of whiskers, dendrites and filaments), *might* obey Arrhenius. But for other processes the temperature dependence of failure is overshadowed by other factors. Consider *solder joints* and *wirebonds* (two primary "wearout" items particularly applicable to packaging and assembly). Although constant high temperature would be a major influence, these are more likely to fail as a result of temperature variations (driven by environmental temperature, by internal power, or by a combination) and exacerbated by vibration or shock. High temperature exposure can even *remove* damage[9]. Similar considerations apply to encapsulation, underfill, and molding materials.

Doubling-for-10°C

Next, consider the mantra that a process doubles in rate for every 10°C increase[10]. How does this relate to Arrhenius—which might be supposed is the basis for this *doubling-for-10°C* "rule"—and to an extended temperature range?

Calculating with Eq. 1 shows that the *doubling-for-10°C* "rule" follows Arrhenius around 125°C, *assuming* the commonly used E_a of ≈ 1 eV. What about other temperatures? Keeping $E_a \approx$ 1 eV and ΔT = 10°C, the corresponding increase in rate (or *acceleration factor* see below) would be 3.6x at 22°C**, but only 1.2x at 500°C, rather than 2x (Table 1, first row).

Considering the rule from other angles: Again keeping $E_a \approx 1$ eV, a doubling of rate at 22°C would require a ΔT of only 5.3°C, but at 300°C it would require a ΔT of 20°C, and at 500°C a ΔT of 37°C (Table 1, second row).

Alternatively, a doubling of rate for a ΔT of 10°C needs an E_a of only 0.54 eV at 22°C, but 2 eV at 300°C, and 3.6 eV at 500°C (Table 1, bottom row).

**Room temperature is taken to be 22°C.

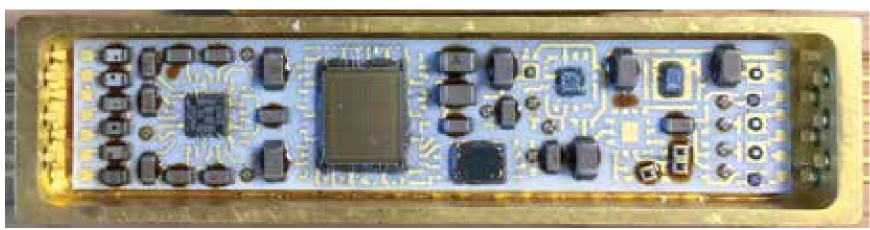


Figure 3. A down-hole (well-logging) multi-chip module specified for 2 years operation at 260°C. *Photo courtesy Quartzdyne, Inc.*

T (°C) →	22**	125	300	500
Accel factor for E_a = 1 eV and ΔT = 10°C	3.6	**2.0**	1.4	1.2
ΔT (°C) for E_a = 1 eV and doubling	5.3	**9.7**	20.0	37.0
E_a (eV) for doubling and ΔT = 10°C	0.54	**0.97**	2.0	3.6

Table 1. Variations on the theme of the *doubling-for-10°C* rule (using Eq. 1).

Figure 1 provides a graphic illustration of the last example: Around 125°C the *doubling-for-10°C* line (dashed gray) and the E_a = 1 eV curve (green line) have similar slopes, confirming that the "rule" is a reasonable approximation around this temperature, but *only* around this temperature for $E_a \approx 1$ eV. For E_a = 0.5 eV, the slopes are similar around 22°C, and for E_a = 2 the slopes are similar around 300°C.

In conclusion, the *doubling-for-10°C* "rule" is not applicable in general, but only under specific parameter circumstances, and especially not for high-temperature electronics[10].

Accelerated Testing

When the required lifetime of a component is long, say years, real-time reliability evaluation is generally impractical. A faster evaluation method is needed. However, in the quest for such a method, there are many pitfalls, especially for high-temperature packaging and assembly.

A popular method is the *accelerated test*. The idea is overstress, which may be electrical (e.g. voltage, current, power), or environmental (e.g. moisture, acceleration, radiation), in addition to, or instead of, temperature. The following concerns accelerated testing *only* via increased temperature: measuring failures or degradation over time at a constant temperature, T_{TEST}, higher than the operating temperature, T_{OPER}, often accompanied by an Arrhenius treatment.

This assumes that a component will exhibit the same failure mechanisms at T_{TEST} as it does at T_{OPER} and that the mechanisms obey the Arrhenius relation. As explained above, this becomes less likely as the temperature range is expanded.

The Arrhenius equation may be recast as

$$\log R = \log A - E_a/kT \qquad \text{Eq. 2}$$

Thus, a process obeying Arrhenius appears as a straight line on a *logR-verus-1/T* plot with slope = $-E_a$. Figure 4 is such a plot for three E_a values appropriate for electronic packaging and assembly. The measured E_a can vary with temperature if

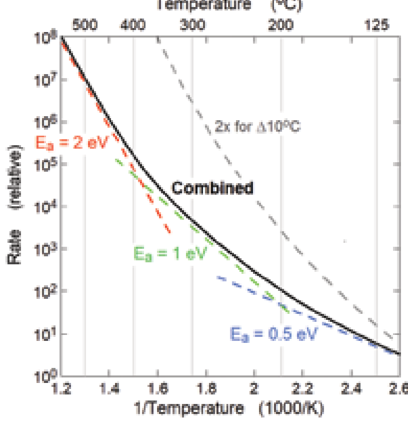


Figure 4. Change of E_a for different T ranges. The prefactors have been set at arbitrary values for illustration; the combined curve (sum of the three E_a lines) is slightly displaced for clarity. A *doubling-for-10°C* exponential is included for comparison (dashed gray line).

T_{TEST} → vs T_{OPER} (°C)		300 vs 200	400 vs 200	500 vs 200	400 vs 300	500 vs 300	600 vs 500
ΔT (°C) →		100	200	300	100	200	100
E_a (eV)	0.3	3.6	8.9	17	2.5	4.8	1.7
	0.5	8.5	38	120	4.5	14	2.4
	1.0	**72**	**1,500**	**1.4e+4**	**20**	**190**	**5.6**
	2.0	5,200	2.1e+6	1.8e+8	410	3.5e+4	31

Table 2. Acceleration factors, F, for high-temperature accelerated testing (Eq. 3)
Shading indicates low acceleration factor, F < 10.

there are different mechanisms dominant at different temperatures, each having a different E_a. As shown by Figure 4 as well as Figure 1, as temperature increases, a process with lower E_a can be overshadowed by a process having a higher E_a. Indeed, it is observed experimentally that activation energies tend to increase with increasing temperature. Thus, trying to curve-fit a single E_a is unreasonable, as illustrated by the combined (black) curve in Figure 4.

For high-temperature electronics, with a typically wider temperature range, or as $T_{TEST} - T_{OPER}$ widens, encountering shifting E_a values is more likely. Consequently, prediction based on extrapolation via Arrhenius is simplistic and suspect and likely to be optimistic[3][11].

Proceeding further, a reshuffle of the Arrhenius formula provides an *acceleration factor*, F, comparing the rate, R, between T_{TEST} versus T_{OPER}:

$$\textit{Acceleration factor}, F \equiv R_{TEST}/R_{OPER} = \exp[(E_a/k)(1/T_{OPER} - 1/T_{TEST})] \quad \textbf{Eq. 3}$$

Considering *only* temperature as a stress, Table 2 presents acceleration factors calculated from Eq 3. Lower E_a or higher temperature means a lower F for the same T_{TEST} versus T_{OPER} and a "flatter" curve (Figure 1). Consequently, a useful acceleration factor, say > 10, may be impractical. For example, for T_{OPER} = 200°C or 300°C, if there is an $E_a \approx 0.5$ eV mechanism, then T_{TEST} must be at least 200°C higher than T_{OPER} for F > 10 (bold red numbers). If $E_a \approx 0.3$ eV the situation is even worse.

Even assuming that accelerated testing is practical, its temperature range of applicability must have limits. As T_{TEST} is increased, it becomes increasingly likely that it will exceed one or more "trigger" temperatures: e.g. polymer glass-transition temperature (T_g) or decomposition temperature, solder melting temperature (MP†), phase change, or ductile-brittle transition[6]. Failure would be immediate or the failure rate could be greatly accelerated out of proportion and meaningless for prediction at T_{OPER}. Individual parts might not even survive the high T_{TEST}.

Thus, acceleration via temperature (as well as burn-in) may be impractical for high-temperature electronics, as this could bring about a failure mechanism that differs from the relevant ones.

Field Environment

For real-life applications constant temperature operation is rare. Consider vehicles, aircraft engines, down-hole probes, spacecraft, and industrial processes—where high-temperature electronics would be applied. Especially for high-temperature electronics, the particular *temperature-vs-time*, T(t), probably irregular, will likely have much greater relevance to reliability "in the field" than constant (time-independent) temperatures.

Moreover, mechanical stresses from nonuniform temperature are more likely as temperature increases, because of generally decreasing thermal conductivity, or from high-power devices, which are often associated with high-temperature electronics.

Besides temperature, additional stresses are typical. Reliability will be strongly influenced by diverse environmental and operational conditions: electrical stress and transients, static discharge, magnetic fields, hostile atmospheres, chemicals, contaminants, pressure, radiation, mechanical vibration and shock, mishandling, and others. Furthermore, these stresses can interact in complex ways with temperature and with each other.

Alternatives?

Considering the pitfalls indicated in the preceding, what are possible alternatives methods to assess and work toward reliability for high-temperature electronics? Without going into detail, here are a few[11]:

Real-time testing may be an expedient option for applications where limited operating lifetime (e.g. ≈ 100–1000 hours) or frequent maintenance can be accepted as a tradeoff against development time and cost. Possible examples include well-logging instrumentation, jet-engine development instrumentation, and data tracers.

Step-stress testing applies increasing overstress to identify weak points of a package or assembly. Typically, temperature is increased incrementally at time intervals until something fails, followed by analysis and resolution[12]. Preferably, testing would include other stresses that will be experienced in use; also, the difference between testing while unpowered, powered but not operating, and fully operating needs consideration.

Physics-of-failure *(PoF)* should be well-suited to high-temperature electronics when thermal energy becomes a major stimulus and physiochemical processes become more active. A package or assembly could be conceptually "taken apart" to test, analyze, and simulate individual structures (e.g. a single joint) independently, and whose "failure" mechanisms *might* be amenable to accelerated testing and Arrhenius treatment[3].

If PoF characterizes a "wearout" ("fail ure") mechanism (e.g. metal fatigue in a joint) and related consequences (e.g. high thermal and electrical resistance and detachment of the joint), can this be called a *reliability* problem, or is it rather a question of inadequacy of design? This facet of PoF mostly indicates what *not* to do and might be better termed "Physics of Wearout."

Sound design and fabrication for high-temperature operation should be foremost, addressing possible degradation mechanisms, in concert with PoF, since the objective is *reliability* rather than testing *per se*. Reliability depends on a component's design, materials, geometry, structure, and fabrication conditions.

Since many of the "failure" (i.e. wearout) mechanisms are known (e.g. metallic interdiffusion, migration, fatigue), avoidance solutions could be applied for high-temperature packaging and assembly. In other words, don't design in a mechanism that is known to cause failure, bearing in mind the component's temperature, lifetime, and other conditions of the application. Design-in and build-in reliability rather than attempt to test-in reliability[12].

Conclusion

In regard to reliability and testing for high-temperature electronics there is no simple, universal answer. High-temperature operation of packaging and assembly enters new and mostly uncharted territory. Reliability and testing methods for "standard" temperature-range (–55°C to +125°C) electronics will need reassessment and revision[1].

Series Wrap-up

This is the final article in this series of five. Certainly, a great deal more could be (and has been) said about high-temperature electronics, but hopefully these brief articles have provided a sense of the issues involved in seriously extending the operating temperature capability of electronics. Electrical performance is paramount but packaging and assembly underlie electrical performance and play a vital role.

Applications are waiting for electronics with high-end temperature capabilities, beyond the present +125–200°C. And as the market for high-temperature applications steadily increases, so does the economic incentive to develop and qualify new assembly and packaging materials and technologies. ◆

Acknowledgements

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Notes

†Melting point (MP) as used here means the temperature above which the material is no longer solid, and thus can be the material's melting-point temperature (for elements or compounds), or eutectic or solidus temperature (for alloys). Higher temperature (≈ > 300–400°C, although definitions differ) joining materials are usually referred to as *brazes*. As used in this article, "solder" may include both solders and brazes.

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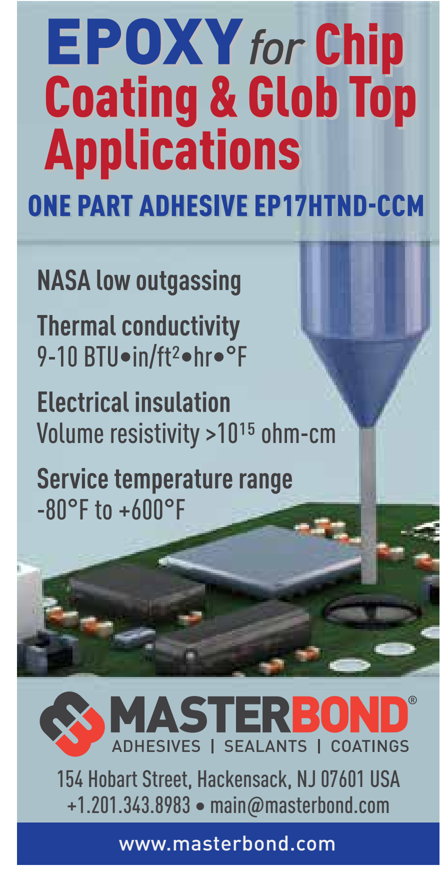

Post-Layout Verification, Analysis and Test Considerations for 2.5/3D Heterogeneous Advanced Packages

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Mentor®, A Siemens Business

MEMORY ACCESS FOR SOC/ASIC devices historically has been facilitated by mounting and connecting these devices on a printed circuit board (PCB). Today's signal speeds and data rates coupled with the need to use less power and generate less heat is changing that paradigm for these devices. Increasingly SoC/ASIC devices are co-located with memory in the same package to support the needed bandwidth and performance. The current trend of integrating a SoC/ASIC with high-bandwidth memory (HBM) on an interposer is a good example. The interposer provides the needed density and performance requirements while providing an overall smaller form-factor.

This approach can also be applied to bring devices of disparate technologies and processes together onto a single substrate, otherwise known as heterogeneous integration. These heterogeneous packages utilize manufacturing techniques, materials, and processes that increasingly are more silicon-like thus creating unique challenges to traditional design tools and methodologies.

Heterogeneous packaging relies on a diverse eco-system to supply the die, substrates, and services to design, assemble, and test these package. Given the multiple data sources and formats it is clear that a comprehensive verification flow is required—one that accounts for assembly-level physical verification, as well as more in-depth, system-level electrical, stress and testability verification. At the same time, expanded EDA tool support is required to ensure fast, accurate, automated flows that ensure package designers can meet their market schedules and performance expectations. Ideally these flows provide a single integrated process for electrical, stress, and test analysis built around a 3D digital model, or twin, of the entire heterogeneous package assembly.

Heterogeneous Assembly Level Verification

2.5/3D Heterogeneous packages typically incorporate multiple devices and multiple substrates to deliver the needed solution for system scaling and performance. With decreasing delineation between die and substrate the close proximity of these elements greatly enhances chip-package interactions (CPI) neces-

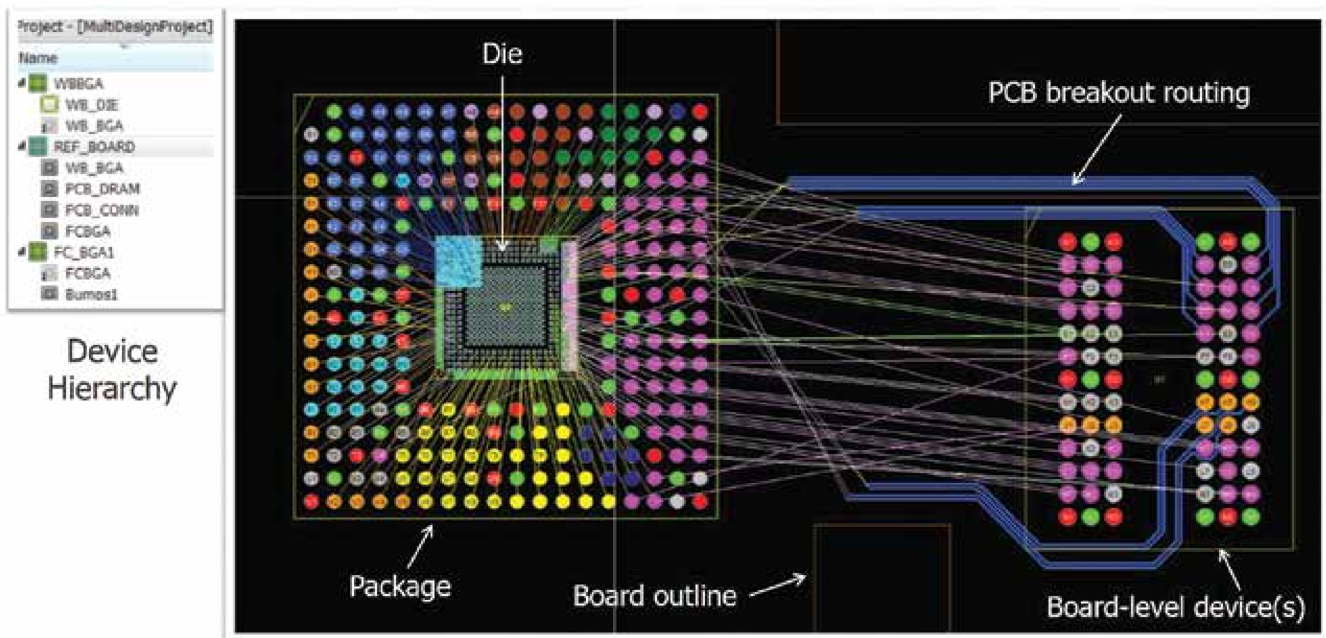

Figure 1. Single Environment for Cross-Substrate Connectivity Planning and Optimization.

sitating a unified co-design flow. With critical elements like high-speed interfaces or power delivery, a decision on one substrate can have a ripple effect on adjacent substrates, or impact the entire system. Designers must find ways to manage multiple substrates in one environment, often while collaborating across geographies and departments, using rapid prototyping and co-design to evaluate substrate routability, electrical and thermal performance, and testing. Finding the right balance and optimal solution can be an endless cycle of iterations.

Physical verification of heterogeneous assemblies has been extensively discussed, and automated solutions introduced [1][2]. There have been analyses of the need for assembly-level layout vs. schematic (LVS) verification. Best practices for an assembly-level LVS process have been explored, including the required inputs (data, formats, etc.), and likely hurdles. There has even been discussion of how parasitic extraction could be achieved for these assemblies [3][4].

As methodologies and flows mature, system-level designers also need to know if package design rule checking (DRC), layout vs. layout (LVL) verification (die-to-package alignment, scaling, orientation, etc.), and assembly-level LVS are sufficient to guarantee correct functionality and successful manufacturing of the heterogeneous assembly. What has not been addressed is the need for a single environment that enables designers to manage all of these processes in an efficient, repeatable, and automated flow.

In heterogeneous design and verification, designers must be able to coordinate and manage multiple substrates (design databases) in one environment. With the ability to see the complete picture (die, interposer, package, PCB) in one environment, designers can better anticipate and eliminate potential downstream issues, efficiently perform and evaluate trade-offs and design scenarios, and clearly communicate decisions to stakeholders.

Digital Twin

Building a digital twin (virtual model) of the 2.5D/3D heterogeneous assembly provides designers a comprehensive representation of the full system comprised of multiple devices and substrates. Model construction requires ability to aggregate data from different sources and in different formats into a cohesive system representation suitable to drive verification and analysis. Tools like Mentor's Xpedition™ Substrate Integrator can import and manage the multiple databases comprising the heterogeneous assembly. Ideally this is done using industry standard formats like LEF/DEF, AIF, GDS, or CSV/TXT files. Functionality should also exist that automatically recognizes device/substrate interfaces without having to instantiate pseudo components.

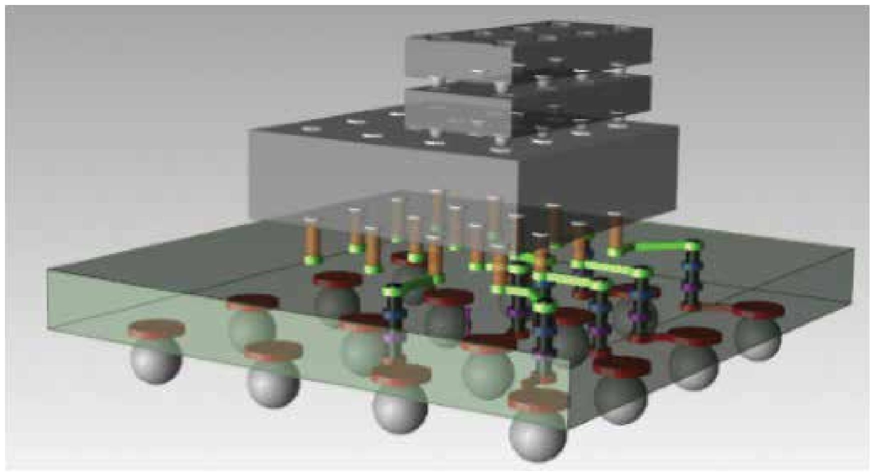

Figure 2. 2.5D/3D Digital Twin (Virtual Model) of Heterogeneous Assembly.

One of the primary benefits of the digital twin approach is that it serves as the golden reference to drive verification and analysis operations. This eliminates need to use multiple static spreadsheets to represent pin and connectivity information replaced by a full system level netlist in Verilog format. This netlist serves as the golden reference for complete physical and electrical verification of every level of the design hierarchy (die, interposers, embedded bridges, and package substrate).

The digital twin enables automated verification of heterogeneous assemblies beginning with substrate level DRC expanding into LVS, LVL, parasitic extraction (PEX), stress and thermal analysis, and finally, test.

Combining the digital twin with industry standardization and EDA tool automation has led to the beginning of a unified approach to providing proven, qualified signoff flows for automated heterogeneous verification.

Physical Verification

One hallmark of IC verification has been the use of multiple specialized EDA tools within a single framework to enable designers to perform a wide variety of verification processes. The goal is the same when automating heterogeneous package assembly verification. Heterogeneous verification is significantly simplified based on the premise each individual die has already been checked to their target foundry rules. It's also critical to maintain independence between the design and verification environments to ensure the veracity of verification results.

Verification is comprised of DRC, which checks the interactions between die (spacing, features sizes, etc.) which may require extracting several layers within each die to see these impacts. It also includes LVL checks for alignment between substrates, scaling or compensation factors, and pad centers or overlap checks. The EDA tool must understand how to differentiate the layering per die and per placement. Using virtual model (digital twin) data, Mentor's Calibre™ 3DSTACK automatically extracts the correct assembly representation to perform DRC/LVL checks ensuring the design meets all physical requirements.

Connectivity Checking (LVS)

LVS checking in an IC looks at the connected shapes and pin locations derived from physical layout data to produce the physical netlist which is compared against the golden schematic netlist to verify connectivity. An automated

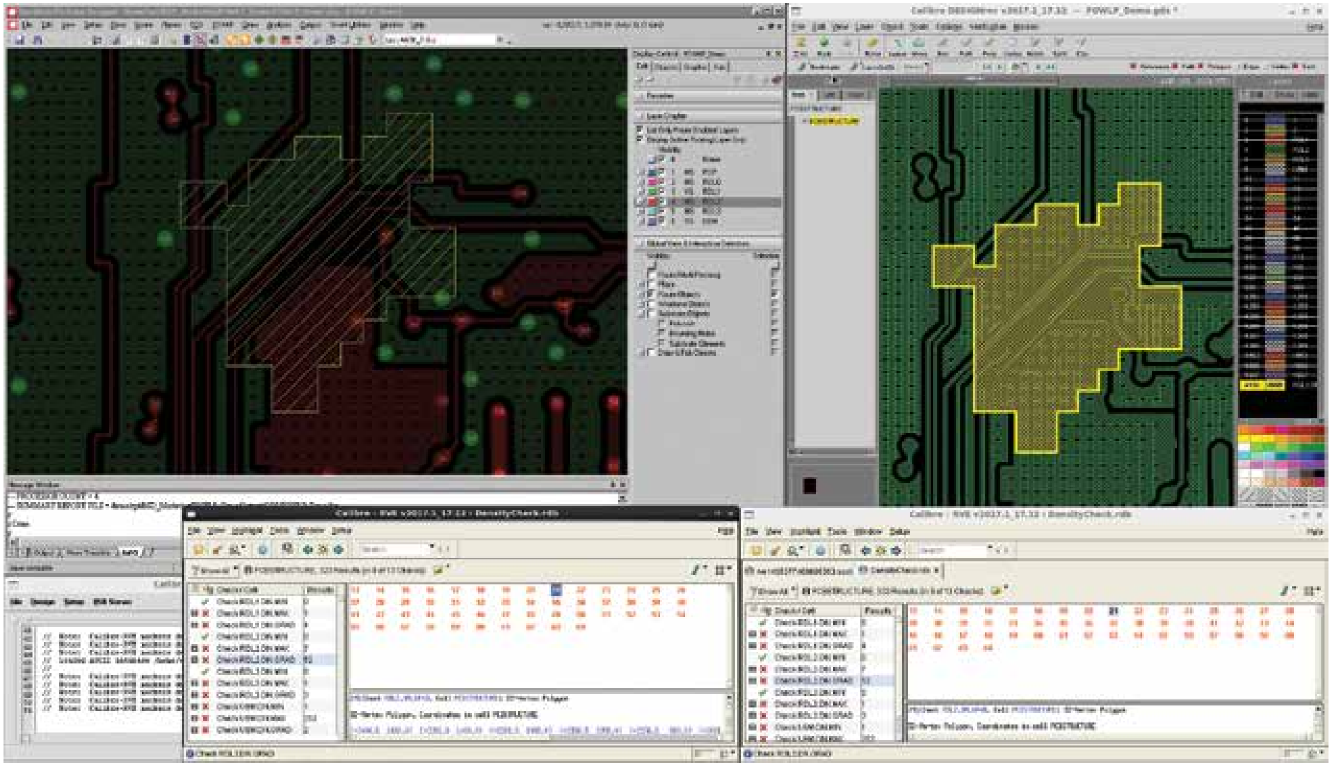

Figure 3. Integration of Verification and Layout Tools Enables Efficient Identification and Resolution of DRC Issues.

package LVS flow in its simplest form must ensure that the interposer/package GDS correctly connects die to die (for multi-die systems) and die to C4/BGA bumps (for both single die and multi-die systems) as intended by the designer [3].

In heterogeneous package assemblies this connectivity may be the die/interposer, die/interposer/package, or die/interposer/package/pcb. Regardless of the configuration it all starts with the ability to generate and manage a system netlist. The system netlist is compiled from the virtual model (digital twin) of the overall assembly as discussed earlier. This system or golden net list is then compared against physical design connectivity derived from the manufacturing data like GDS in Calibre 3DSTACK. Warnings or violations can be highlighted in the virtual model where Xpedition Substrate Integrator functionality can be used to trace and debug errors.

Parasitic Extraction

2.5D/3D heterogeneous designs typically use through-silicon via (TSV), which are long vias extending through the die or substrate to connect the front and back side. These TSVs allow die and substrates to be stacked and directly interconnected. However, in addition to their own significant electrical characteristics, TSVs also have an indirect effect on the electrical behavior of devices and interconnects in their vicinity. To accurately model a 2.5D/3D heterogeneous system, a designer needs tools that extract precise electrical parameters from the physical structure of these 2.5D/3D elements, which can then be fed into behavioral simulators [4]. Utilizing data from the virtual model (digital twin) tools like Calibre 3DSTACK used in concert with Calibre xACT™ can be used to extract parasitics of these 2.5D/3D elements.

Thermal Analysis

2.5D/3D heterogeneous assemblies bring active die into closer proximity, making thermal interaction within the assembly an area of concern. Given this proximity and higher power densities, heat dissipation becomes one of the main challenges that affects the performance and reliability of 2.5/3D heterogeneous assemblies. Using Mentor's FloTHERM™ product in conjunction with a Calibre thermal analysis, designers can reference a system-level model for in-context die level simulation, and create a die level thermal model that can be imported into a larger system for thermal simulation. While boundary conditions can be imported for more accurate modeling at the die level this solution also exports detailed thermal models of the heterogeneous assembly for accurate system level modeling. This provides designers the ability to accurately model from the die level to the system level (e.g. inside the die, inside the package, and package to system).

Mechanical Stress Analysis

2.5D/3D stacking can create a variety of unintentional physical stresses, such as substrate warpage during mounting as well as bump-induced stress. Designers must be able to analyze a layout for stresses caused by such chip-package interactions and their impact on device performance. By combining Calibre layout processing with proprietary modeling techniques, designers can analyze MOSFET channel mechanical stress, as well as stress-induced variation of transistor

electrical parameters (such as mobility and current).

It's also important to recognize thermal and mechanical stress do not happen in isolation but are closely intertwined. Heating effects can impact mobilities, i.e. impact stress. Similarly stresses (die/substrate stacking and TSVs) can also have a significant impact on the thermal conductivity.

Testing

Known good die (KGD) are key to effective testing prior to stacking in 2.D/3D heterogeneous assemblies. Package-level test generation is also important—test teams should reuse die-level built-in self-test (BIST) and scan patterns by mapping them up to package level. Boundary scan testing of the package interconnect structures ensures the IO are actually connected, and can identify any substrate fabrication or assembly issues. Partial stack testing is usually only done on new processes or those known or expected to have poor yield.

However, even with high-quality wafer testing and KGD, assembly can still produce failures from ESD damage or from pins missed during wafer testing. With multi-die packaging, the quality and depth of wafer testing is critical if the target yield of assembled parts is to be maintained. Mentor's Tessent™ logic test tools provide a variety of "best practice" test capabilities for heterogeneous package testing, including:

- Re-use of die-level test patterns
- Use of a common test access port (TAP) interface for all levels of substrate
- Use of IJTAG to enable flexibility by controlling the modes of test patterns
- Remapping of die level test patterns to the other levels of package substrate

Summary

Heterogeneous packaging is a disruptive impact on traditional design and verification methods. The growth of these designs demands an efficient, proven automated sign-off for physical, electrical, thermal, and manufacturing performance. To ensure consistency and automation of these processes, a single environment that enables designers to manage all of these processes in an efficient, repeatable, and automated flow is essential. ◆

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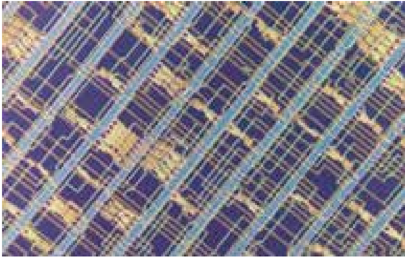
State-of-the-Art Technology Briefs

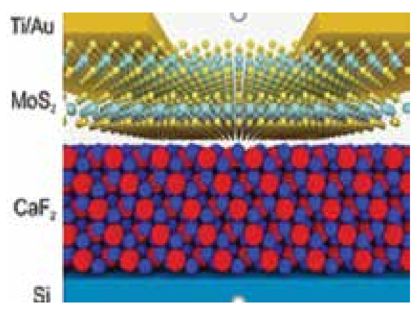
A special feature courtesy of Binghamton University

This feature is brought to us by Benson Chan, Associate Director, Integrated Electronics Engineering Center (IEEC), Binghampton University. The State-of-the-Art Technology Briefs contains articles from the Binghamton University S3IP "Flashes". Full text is available upon request through the IEEC Site at: http://www.binghamton.edu/s3ip/index.html.

Researchers from the University of Wisconsin-Madison have devised a method to create pieces of "smart" glass that can recognize images without requiring any sensors, circuits or power sources. They use optics to condense the normal setup of cameras, sensors and deep neural networks into a single piece of thin glass. Embedding artificial intelligence (AI) inside inert objects is a concept could open new frontiers for low-power electronics. AI gobbles up substantial computational resources every time you glance at your phone to unlock it with face ID. In the future, one piece of glass could recognize your face without using any power at all. *(IEEC file #11257, Science Daily, 7/8/19)*



MIT researchers have built a modern microprocessor from carbon nanotube transistors, which are widely seen as a faster, greener alternative to their traditional silicon counterparts. The microprocessor, which can be built using traditional silicon-chip fabrication processes, representing a major step toward making carbon nanotube microprocessors more practical. They demonstrated a 16-bit microprocessor with more than 14,000 CNFETs that performs the same tasks as commercial microprocessors. The microprocessor is based on the RISC-V open-source chip architecture. *(IEEC file #11328, Nanowerk News, 8/29/19)*



Researchers at the Vienna University of Technology have created an ultra-thin transistor, with excellent electrical properties and can be miniaturized to an extremely small size. This next big miniaturization step in microelectronics is becoming possible – with two-dimensional (2D) materials. They used a novel insulator made of calcium fluoride, to produce the new ultra-thin transistor. The prototype with its superior electrical properties outshines all previous models. Now the team wants to find out which combinations of insulators and semiconductors work best. It may take a few more years before the technology can be used for commercially available computer chips as the manufacturing processes for the material layers still need to be improved. *(IEEC file #11280, Science Daily,7/24/19)*

Lumitronix has succeeded in integrating plasma-metallized flexible printed circuit boards with electronic components. The novel technology turns a plurality of materials into electrically conducting and solderable printed circuit boards that were not suitable previously for an assembly with electronic components. Within the framework of this special type of metallization, a plasma spray head is used to spray a conductive metal in the form of a powder under high atmospheric pressure onto the basic material coated with silver paste. Simultaneously, the copper is fused by a very hot plasma beam of 10,000-50,000°C whereby a connection with the silver substrate is being formed. *(IEEC file #11260, Printed Electronics World, 7/12/19)*

Researchers at the Rochester Institute of Technology have created a laser for sound. by demonstrating a phonon laser using an optically levitated nanoparticle. The researchers studied the mechanical vibrations of the nanoparticle, which is levitated against gravity by the force of radiation at the focus of an optical laser beam. The mechanical vibrations become intense and fell into perfect sync. Because the waves emerging from a laser pointer are in sync, the beam can travel a long distance without spreading in all directions. In a standard optical laser, the properties of the light output are controlled by the material from which the laser is made. In the phonon laser the roles of light and matter are reversed. *(IEEC file #11148, R&D, 4/15/19)*

University of Utah engineers have discovered a way to produce more electricity from heat than thought possible by creating a silicon chip, known as a 'Near-Field Radiative Heat Transfer Device,' that converts thermal radiation into electricity. The team produced a 5mm-by-5mm chip of two silicon wafers with a 100 nanometers gap between them. This could lead to much longer battery life in devices such as laptop computers and cellphones, and solar panels that are much more efficient at converting radiant heat to energy. *(IEEC file #11258, Science Daily, 7/10/19)*

The EV Group (EVG) has unveiled MLE™ (Maskless Exposure), a revolutionary next-generation lithography technology developed to address future back-end lithography needs for advanced packaging, MEMS, biomedical and high-density printed circuit board applications. The MLE combines high-resolution pattern-

ing with high throughput and yield, while eliminating the overhead costs of photomasks. Heterogeneous integration is an increasing driving force in semiconductor development, impacting the advanced packaging, MEMS and PCB markets. *(IEEC file #11240, Semiconductor Digest, 7/2/19)*

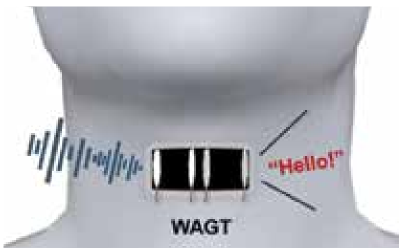
Binghamton University researchers have found a way to improve the performance of tiny sensors by developing a more reliable way to use actuators that control MEMS. The team found that combining two methods for electrostatic actuation – parallel-plate and levitation actuators – led to a predictable linearity that neither of those systems offered on its own. These findings could be revolutionary for microphone manufacturing, because with this design the signal can be boosted high enough that the background noise from the electronics is no longer an issue. More than 2 billion microphones are made around the world each year, and that number is growing as more devices feature vocal interaction. *(IEEC file #11303, Binghamton University, 8/15/19)*

Engineers at the University of California have developed the thinnest optical device in the world–a waveguide that is three layers of atoms thin. The work is a proof of concept for scaling down optical devices to sizes that are orders of magnitude smaller than today's devices. It could lead to the development of higher density, higher capacity photonic chips. The waveguide consists of a tungsten disulfide monolayer (made up of one layer of tungsten atoms sandwiched between two layers of sulfur atoms) suspended on a silicon frame. The monolayer is patterned with an array of nanosized holes forming a photonic crystal. *(IEEC file #11300, Semiconductor Digest, 8/12/19)*

MARKET TRENDS

The embedded memory market has the potential to reach $1.2 billion by 2024, growing with a 295% CAGR over this period. MRAM promises life beyond eFlash. Among various emerging NVM technologies, spin transfer torque magnetoresistive RAM (STT-MRAM) is gaining significant momentum and poised to become the next embedded memory solution for IC products manufactured at the 28nm node and below. That includes low-power wearables and IoT devices, MCUs, automotive, imaging and display ICs, edge AI accelerators, and other ASICs and ASSPs. *(IEEC file #11315, Semiconductor Digest, 8/12/19)*

Purdue University researchers have developed a new fabric innovation that allows wearers to control electronic devices through clothing. This technique is capable of transforming any existing cloth into a self-powered e-textile containing sensors, music players or illumination displays using simple embroidery without the need for expensive fabrication processes. The waterproof, breathable and antibacterial self-powered clothing is based on omniphobic triboelectric nanogeneragtors (RF-TENGs), which use embroidery and fluorinated molecules to embed small electronic components and turn clothing into self-powered devices. *(IEEC file #11310, Science Daily, 8/8/19)*



ACS Nano researchers have developed a wearable artificial throat that, when attached to the neck like a temporary tattoo, can transform throat movements into sounds. To make their artificial throat, they laser-scribed graphene on a thin sheet of polyvinyl alcohol film. The flexible device measures 0.6 by 1.2 inches. The researchers used water to attach the film to the skin over a volunteer's throat and connected it with electrodes to a small armband that contained a circuit board, microcomputer, power amplifier and decoder. In the future, mute people could be trained to generate signals with their throats that the device would translate into speech. *(IEEC file #11293, Printed Electronics World, 7/29/19)*

The fiber optic sensor market was valued at $1.1 billion in 2015 and expected to register a CAGR of 10.4% from 2016 to 2026. Increasing adoption in the oil and gas industry and investments in infrastructure are factors driving growth. Additionally, government initiatives to deploy fiber optic sensors in various construction projects is propelling significant growth. The market is segmented on the basis of Technology; Rayleigh Scattering Based Distributed Sensor, Brillouin Scattering Based Sensor, Raman Scattering Based Sensor, Interferometric Distributed Optical-Fiber Sensor, Application (Strain Sensing, Temperature Sensing, Acoustic/Vibration Sensing, Pressure Sensing). *(IEEC file #11186, Sensors, 5/7/19)*

The 2019 Nobel Prize in Chemistry was awarded to M. Stanley Whittingham, distinguished professor of chemistry at Binghamton University. Whittingham won the prize for pioneering research leading to the development of the lithium-ion battery. He holds the original patent on the concept of the use of intercalation chemistry in high-power density, highly reversible lithium batteries — work that provided the basis for subsequent discoveries that now power most laptop computers. *(IEEC file #11369? ,Binghamton University, 10/11/19)*

RECENT PATENTS

PCB inspecting apparatus, method for detecting anomaly in solder paste *(Assignee: Koh Young Technology)- Pub. No- EP3501828* – A printed circuit board inspection apparatus obtains measurement shape information about each of a plurality of solder pastes printed on a first printed circuit board through a plurality of apertures and aperture shape information about each of the apertures, obtains probability values that a first solder paste printed through a first aperture of the plurality of apertures and each of a plurality of second solder pastes printed through second apertures other than the first aperture have the measurement shape information when the first solder paste and the plurality of second solder pastes are printed on the first printed circuit board, by applying the measurement shape information and aperture shape information to a machine-learning based model.

Multi-layer circuit board using interposer layer and conductive paste.- *(Assignee: Sierra Circuits, Inc.)- Patent No- 10,349,520*– A multi-layer circuit board is formed by positioning a top sub having traces on at least one side to one or more pairs of composite layers, each composite layer comprising an interposer layer and a sub layer. Each sub layer is adjacent to an interposer layer having an interconnection aperture, the interconnection aperture positioned adjacent to interconnections having a plated through via or pad on each corresponding sub layer. Each interposer aperture is filled with a conductive paste, and the stack of top sub pairs of composite layers are placed into a lamination press,

Staged via formation from both sides of chip. - *(Assignee: Tessera Inc.) Patent No- 10,354,942*– A method of fabricating a semiconductor assembly can include providing a semiconductor element having a front surface, a rear surface, and a plurality of conductive pads, forming at least one hole extending at least through a respective one of the conductive pads by processing applied to the respective conductive pad from above the front surface, forming an opening extending from the rear surface at least partially through a thickness of the semiconductor element, such that the at least one hole and the opening meet at a location between the front and rear surfaces, and forming at least one conductive element exposed at the rear surface for electrical connection to an external device.

PCB with substrate integrated waveguide transition. *(Assignee: Texas Instruments)- Patent No- 20190207286*– In described examples, an integrated waveguide transition includes a substrate with a waveguide side and an opposing waveguide termination side. A first layer of metal covers a portion of the waveguide side, a second layer of metal is separated from the first layer of metal by a first layer of dielectric, and a third layer of metal covers a portion of the waveguide termination side and is separated from the second layer of metal by a second layer of dielectric. A substrate waveguide perpendicular to a plane of the substrate extends from the waveguide side to the waveguide termination side; and a length and a width of the substrate waveguide is defined by a fence of ground-stitching vias that short the first layer of metal and the second layer of metal to a plate of the third layer of metal that forms a back short.

Deterioration detection sensor of printed wiring board.- *(Assignee: FANUC)-Patent No- 16/234111*–An object is to provide a deterioration detection sensor of a printed wiring board in which the accuracy of detection is enhanced. A deterioration detection sensor of a printed wiring board is a circuit board which is vertically provided on a printed wiring board and is soldered to the printed wiring board with a soldering portion at a lower end. The deterioration detection sensor includes a detection surface for detecting a foreign material. The detection surface forms an intersection surface which intersects the planar direction of the printed wiring board. In the deterioration detection sensor as described above, a wiring in the detection surface is broken, and thus the foreign material is detected.

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BINGHAMTON UNIVERSITY *currently has research thrusts in healthcare / medical electronics; 2.5D/3D packaging; power electronics; cybersecure hw/sw systems; photonics; MEMS; and next generation networks, computers and communications. The S3IP Center of Excellence is an umbrella organization comprising five constituent research centers. More information is available at* ***www.binghamton.edu/s3ip.***

Center for Autonomous Solar Power (CASP) - The CASP center focusses on thin film solar cells and supercapacitors. The recent progress incudes 7.5% efficiency pure sulfide CZTS solar cell without an antireflection coating, and nano-structured transition metal oxide supercapacitor with specific capacitance of 760 F/g, maximum energy density of 8 Wh/kg, and a power density of 13 KW/kg. The CASP team has been invited to take part in the Cohort 5 NEXUS-NY program to explore market opportunity of a dielectric capacitor technology (patent currently drafted) that recently came out of CASP center. More information is available at ***www.binghamton.edu/casp.***

Integrated Electronics Engineering Center (IEEC) - The IEEC is a New York Center of Advanced Technology (CAT) responsible for the advancement of electronics packaging. Its mission is to provide research into electronics packaging to enhance our partner's products, improve reliability and understand why parts fail. More information is available at ***www.binghamton.edu/ieec***

NorthEast Center for Chemical Energy Storage (NECCES) - NECCES Director and Distinguished Professor of Chemistry and Materials Science M. Stanley Whittingham was recognized with the Nobel Prize in Chemistry for development of lithium-ion batteries, which "have revolutionized our lives" and "laid the foundation of a wireless, fossil fuel-free society." Whittingham won the prize for pioneering research leading to the development of the lithium-ion battery along with John B. Goodenough, Virginia H. Cockrell Centennial Chair in Engineering at the University of Texas at Austin and Akira Yoshino of Meijo University in Japan. "I am overcome with gratitude at receiving this award, and I honestly have so many people to thank I don't know where to begin," said Whittingham. "The research I have been involved with for over 30 years has helped advance how we store and use energy at a foundational level, and it is my hope that this recognition will help to shine a much-needed light on the nation's energy future." More information is available at ***www.binghamton.edu/neccess.***

Analytical and Diagnostic Laboratory (ADL) - The ADL provides an array of analytical and diagnostic tools located in a single facility to address the needs of faculty and industry in understanding materials, structures and failures that are found in electronics packaging. The ADL supports the 5 research centers previously mentioned. The facilities of the ADL are available to our industry partners. More information is available at ***www.binghamton.edu/adl*** ◆

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