MEPTEC Report

FALL 2019

A Quarterly Publication of The Microelectronics Packaging & Test Engineering Council

Volume 23, Number 3

KNOWN GOOD DIE WORKSHOP 2019

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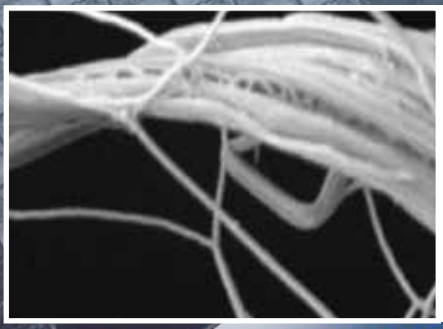

MIT engineers have fabricated polythene films that conduct heat at 62W/mK, which is as good as steel, better than alumina, and much better than normal polythene which is an insulator. These properties of polymers can create new applications and new industries and may replace metals as heat exchangers.

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INSIDE THIS ISSUE

Amkor Technology®

Cutting-edge solutions for 5G applications

Amkor is the first OSAT to deliver high volume manufacturing of products using Antenna in Package (AiP)/ Antenna on Package (AoP) technology. Our fully-integrated 5G NR millimeter wave (mmWave) and sub-6 GHz RF modules deliver capabilities across several spectrum bands utilizing a compact footprint.

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Fall Ahead

Ira Feldman
Executive Director, MEPTEC

WELCOME! FROM LONG TIME MEPTEC members to recent subscribers to casual visitors, we are glad you are here.

Summer is drawing to a close here in Silicon Valley as I write: children are returning to school, vacations are winding down, and monthly industry events are increasing in number.

MEPTEC took only a one-month summer break in our monthly Semiconductor Industry Speaker Series. We had an excellent presentation on System-in-Package (SiP) by Eelco Bergman of ASE Group in June. And we resumed in August with presentations by Stephen Rothrock of ATREG on the importance of facility locations to one's manufacturing strategy and David Adler of SVXR on x-ray inline process control. We have a very strong list of presentations scheduled for the rest of 2019. We hope to see you and welcome your suggestions on topics and/or presenters for 2020.

The MEPTEC staff and I have also been focused on our next full day event: the ***Known Good Die (KGD) Workshop on Thursday December 12, 2019*** in Silicon Valley. We are excited to celebrate KGD's 20th year as this critical topic is revisited! Please see the event information on page 27 and kgdworkshop.org for more information.

The Advisory Board (AB) has been busy planning our event calendar for 2020. We are looking forward to announcing several relevant and exciting full day events and luncheons before the year is out. We are happy to have Calvin Cheung, VP Engineering at ASE join the Advisory Board! Rich Rice will be stepping down, but we look forward to continuing to see him at future MEPTEC events. Thank you Rich for all of your support of MEPTEC!

I look forward to hearing your suggestions and feedback as to how MEPTEC can best serve you. Don't be shy!

Kind regards,

Ira Feldman
Executive Director, MEPTEC
ira@meptec.org
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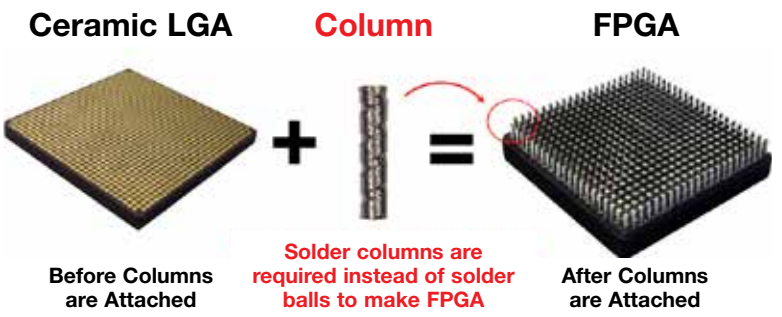
Does the FPGA Industry Face Peril? *Pt. I*

Martin Hart
TopLine Corporation



A SUDDEN SHORTAGE OF MISSION critical Field Programmable Gate Array (FPGA) devices could cause market distortions that are not in the defense industry's best interest, resulting in warfighters not flying and rockets not launching. Proactive steps taken now to close the gaps by identifying and monitoring the risks can mitigate such a threat.

Documentation published by the Defense Logistics Agency (DLA) shows that makers of FPGA devices depend upon a single subcontractor to provide services to attach copper wrapped solder columns. Columns, rather than solder balls, are a critical subcomponent in the final assembly of FPGA packages. An FPGA is an integrated circuit configurable by customers in the field, making such devices desirable for space and military applications, providing reduced cost and improved design cycle time. Radiation Hardened FPGA devices can withstand attacks from electromagnetic and particle radiation in outer space and high-altitude flight missions.

Past production shortages in the semiconductor industry have been short-lived because multiple vendors have been able to quickly step in to fill voids in the supply chain. Today, only a single subcontractor is designated on the Qualified Manufacturer List (QML-38535) as a provider of copper wrapped solder column attachment services for the entire FPGA industry. The supply-chain is vulnerable if a single supplier of critical components, such as copper wrapped solder columns, were suddenly unable to continue operations.

Business continuation is often an issue for any number of reasons, including natural disasters (fire, flood, earthquake) or the loss of a key manager due to death or retirement. An existential threat could materialize if a hostile foreign actor acquires said single-source supplier and moves production off-shore as a stratagem to lower production costs. A facility relocation typically results in the loss of QML status, pending requalification.

It could take 24-months for a new candidate to undergo an arduous process prior to attaining QML status for column attachment services. A prolonged production shut down of FPGA devices is relevant to National Security, affecting thousands of downstream customers who would be unable to complete systems and black box builds.

Industry veterans undoubtedly recall the impact in the FPGA supply chain in 2013 when IBM announced their intention to exit the ceramic column grid array (CCGA) FPGA business. IBM's entire column attachment production line was boxed up and sat in storage for years before being put back into service by a licensee.

Concerns over a diminishing supplier base is an on-going issue in the semiconductor industry. The U.S. Department of Defense (DoD) provides guidelines to assist the industry to identify and mitigate dependency on services from single-source subcontractors. The Defense Standardization Program Office publishes a helpful document SD-22, titled, "Diminishing Manufacturing Sources and Material Shortages (DMSMS), a Guidebook of Best Practices for Implementing a Robust DMSMS Management Program." It is a useful resource to aid FPGA device makers seeking to broaden their supplier base for components that are critical to the welfare of national security. The DMSMS guidebook presents the concerns and recommended remedies to mitigate the risk of loss, or impending loss, of manufacturers or suppliers of items, software, and raw materials.

The Under Secretary of Defense for Acquisition and Sustainment delivers an annual report to Congress titled "Industrial Capabilities" stating the mission of the Office of Industrial Policy (INDPOL) is to ensure a robust, secure, resilient, and innovative industrial capabilities upon which the DoD can rely.

Eight public companies making the majority of the world's FPGA devices may consider issuing forward-looking cautionary statements to shareholders according to guidelines of the Exchange Commission (SEC) citing their reliance on a single QML vendor to attach copper wrapped columns. These statements disclose potential risks from the perspective of management's reasoning or beliefs.

Fabrication of copper wrapped solder columns is not trivial, and requires the correct know-how, manufacturing equipment and proficient operator skills to properly attach columns to FPGA packages. You can't buy solder column attachment services from your friendly catalog distributor. Part 2 of Call to Action will describe a path to mitigate risk by encouraging the supply-chain to develop multiple suppliers for attaching copper wrapped solder columns to FPGA devices.

Conclusion

Risk of a FPGA production shut down is preventable by taking prudent action now. The most direct solution is to qualify multiple vendors for critical processes including column attachment services. This remedy requires a relatively low investment by FPGA device makers. The alternative is to wait for an unexpected disaster to strike, potentially costing the defense industry hundreds of millions of dollars. ◆

MEPTEC
THE NEXT GENERATION

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315 Savannah River Dr., Summerville, SC 29485
Tel: (650) 714-1570 Email: bcooper@meptec.org

Publisher MEPCOM LLC
Editor Bette Cooper
Art Director/Designer Gary Brown
Sales Manager Gina Edwards

MEPTEC Executive Director

Ira Feldman

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In Memoriam

Bance Hom

Contributors

David L. Adler, Ph.D. SVXR Inc.
William Boyce SMART Microsystems Ltd.
Ira Feldman Feldman Engineering Corp.
Thom Gregorich ZEISS Process Control Solutions
Allen Gu ZEISS Process Control Solutions
Martin Hart TopLine Corporation
Ron Jones N-Able Group International
Sam Karikalan Broadcom, Inc.
Dr. Randall K. Kirschman R&D Consultant
Dr. Gamal Rafai-Ahmed Xilinx

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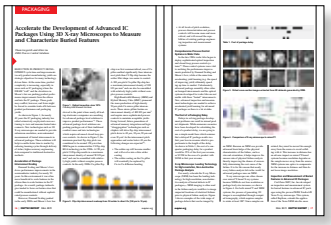
ON THE COVER

The Known Good Die (KGD) Workshop returns to Silicon Valley on Thursday December 12, 2019 at the SEMI Global Headquarters in Milpitas, California. We are excited to celebrate KGD's 20th year as this critical topic is revisited! This event will bring together experts to cover topics such as: Metrology and Inspection, Test and Handling, Big Data and Analytics, Business Model, and EDA and CAD Tools. Please see the event information on page 27 and visit kgdworkshop.org for more information.



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MICHAEL R. LOPEZ JOINS PROMEX AS NEW COO

Promex Industries has named Michael Lopez as their new Chief Operating Officer. Michael will be responsible for growing Promex while ensuring operational excellence. His considerable experience as a COO of companies producing Class II and Class III medical devices will come in handy, as many medical device OEMs come to Promex early in the development cycle to take advantage of their design for manufacturability and process validation expertise.

www.promex-ind.com

ASE RECEIVES A 2018 TOP SUPPLIER AWARD FROM ADI

Advanced Semiconductor Engineering, Inc. (ASE) is pleased to announce that it has received a top award at the Analog Devices Inc. (ADI) inaugural Supplier Day that brought together 100 of the semiconductor company's top suppliers for a day of recognition, celebration and relationship building. Testament to outstanding performance and contributions, ASE was one of 18 award recipients at the ceremony.

The award, Top Performer Contracted Manufacturing – Back End, was presented to ASE by John Hassett, Senior Vice President Global Operations and Technology, who paid tribute to the critical role ASE plays in ADI's overall strategy. The awards recognized excellence across five categories, including Quality, Delivery, Service/Responsiveness, New Product Time to Revenue, and Corporate Social Responsibility.

www.asegroup.com

Xilinx Announces the World's Largest FPGA Featuring 9 Million System Logic Cells

New Virtex UltraScale+ Device Enables the Creation of Tomorrow's Most Complex Technologies

XILINX, INC., THE LEADER in adaptive and intelligent computing, has announced the expansion of its 16 nanometer (nm) Virtex® UltraScale+™ family to now include the world's largest FPGA — the Virtex UltraScale+ VU19P. With 35 billion transistors, the VU19P provides the highest logic density and I/O count on a single device ever built, enabling emulation and prototyping of tomorrow's most advanced ASIC and SoC technologies, as well as test, measurement, compute, networking, aerospace and defense-related applications.

The VU19P sets a new standard in FPGAs, featuring 9 million system logic cells, up to 1.5 terabits per-second of DDR4 memory bandwidth and up to 4.5 terabits per-second of transceiver bandwidth, and over 2,000 user I/Os. It enables the prototyping and emulation of today's most

complex SoCs as well as the development of emerging, complex algorithms such as those used for artificial intelligence, machine learning, video processing and sensor fusion. The VU19P is 1.6X larger than its predecessor and what was previously the industry's largest FPGA — the 20 nm Virtex UltraScale 440 FPGA.

The VU19P is supported by an extensive set of debug, visibility tools, and IP, providing customers with a comprehensive development platform to quickly design and validate next-generation applications and technologies. Hardware and software co-validation allows for developers to bring up software and implement custom features before physical parts are available. Moreover, the design flow can be co-optimized by using the Xilinx Vivado® Design Suite, which reduces cost and tape-out risk, and improves efficiency and time-to-market.

For more information, visit www.xilinx.com. ◆

Intel Pushes 'AI Everywhere'

INTEL HAS REVEALED NEW DETAILS OF upcoming high-performance artificial intelligence (AI) accelerators: Intel® Nervana™ neural network processors, with the NNP-T for training and the NNP-I for inference. Intel engineers also released technical details on hybrid chip packaging technology, Intel® Optane™ DC persistent memory and chiplet technology for optical I/O.

"To get to a future state of 'AI everywhere,' we'll need to address the crush of data being generated and ensure enterprises are empowered to make efficient use of their data, processing it where it's collected when it makes sense and making smarter use of their upstream resources. Data centers and the cloud need to have access to performant and scalable general purpose computing and specialized acceleration for complex AI applications. In this future vision of AI everywhere, a holistic approach is needed—from hardware to software to applications," said Naveen Rao, Intel vice president and general manager, Artificial Intelligence Products Group.

Turning data into information and then into knowledge requires hardware architectures and complementary packaging, memory, storage and interconnect technologies that can evolve and support emerging and increasingly complex use cases and AI techniques. Dedicated accelerators like the Intel Nervana NNPs are built from the ground up, with a focus on AI to provide customers the right intelligence at the right time. ◆

TSMC to Boost Recruitment by More Than 3,000 New Hires

Personnel Expansion to Support Business Growth and Technology Development

TSMC HAS ANNOUNCED a large-scale hiring plan to support the Company's business growth and technology development, aiming to recruit more than 3,000 new employees in Hsinchu, Taichung, and Tainan. Job vacancies include semiconductor equipment engineers, R&D engineers, process engineers, process integration engineers, and production line operators.

After successfully bringing its industry-leading 7-nanometer logic technology to volume production, TSMC is ceaselessly advancing with development of 5-nanometer and 3-nanometer logic technology. This year, the Company continues to develop new technologies and build capacity to help customers unleash innovation and create maximum value with a comprehensive portfolio of advanced logic and specialty technologies. Accordingly, TSMC is recruiting broadly from both experienced professionals and first-time job seekers with backgrounds in electronics, electrical engineering, optoelectronics, mechanical engineering, physics, chemistry, chemical engineering, industrial engineering, and related fields to come on board and keep moving semiconductor technology forward.

Interested applicants are welcome to browse job openings on the TSMC website at https://www.tsmc.com/english/careers/index.htm and upload a resume with personal information now. ◆

UV Curing Adhesive Passes NASA Low Outgassing Specifications

MASTER BOND UV10TK40M is a one part UV curable system, which is not oxygen inhibited, and can be used for bonding, sealing and coating applications. UV10TK40M is optically clear, with a refractive index of 1.55. It has a high glass transition temperature (Tg) of 135-140°C and is serviceable from -60°F to +450°F. Its hardness upon curing is 75-85 Shore D.

"Not only does it meet NASA low outgassing specifications, but this system also withstands 1,000 hours at 85°C/85% RH. Its Shore D hardness was not adversely affected even after exposure to elevated temperatures and high relative humidity", says Rohit Ramnath, Senior Product Engineer. UV10TK40M cures in 20-30 seconds when exposed to a UV light source emitting at a wavelength of 320-365 nm with 20-40 milliwatts per cm^2.

UV10TK40M bonds well to glass, surface treated metals and plastics such as polycarbonates and acrylics. UV10TK40M is recommended in fiber-optic, optical, opto-electronic and electronic applications where heat resistance and a moderate viscosity are needed. The product is available in 1/2 pints, pints, quarts, gallons and syringes.

For more information visit www.masterbond.com. ◆

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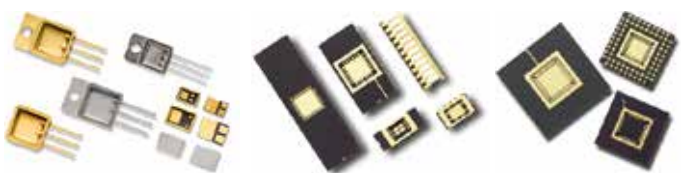

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KEN MOLITOR JOINS QUIK-PAK AS COO

Quick-Pak's new Chief Operating Officer Ken Molitor understands that new products are the lifeblood of the semiconductor industry. "Being first to market is important. That's where Quik-Pak can help. Our cross-functional teams give us the horsepower to turn jobs quickly. Combined with the engineering support and manufacturing knowledge we provide to our customers, we can significantly shorten time to market for their new product designs," he said.

In his previous COO positions, Ken was involved in relocating two semiconductor manufacturing facilities — experience that will come in handy this winter as he guides Quik-Pak through its own facilities relocation.

www.icproto.com ◆

ATREG Successfully Assists ON Semiconductor in Phased Acquisition of GLOBALFOUNDRIES' 300mm East Fishkill Facility

ATREG, INC., WHICH specializes in helping global companies divest and acquire infrastructure-rich advanced technology cleanroom assets, has announced that it has successfully represented and assisted ON Semiconductor Corporation with the structure of a transaction to acquire GLOBALFOUNDRIES' 300mm fab located in East Fishkill, New York for an amount of $430 million. Under the terms of this phased purchase agreement, $100 million was paid at signing and $330 million will be paid at the end of 2022, at which point ON Semiconductor will gain full operational control of the fab and the site's workforce will fully transition to ON Semiconductor. GLOBALFOUNDRIES will manufacture 300mm wafers for ON Semiconductor

until the end of 2022, with the first production of 300mm wafers for ON Semiconductor expected to begin in 2020.

The transaction also includes a technology transfer and development agreement as well as a technology license agreement, enabling ON Semiconductor to convert its wafer processes from 200mm to 300mm and to have immediate access to advanced CMOS capability, including 45nm and 65nm technology nodes.

For more information about ATREG please visit www.atreg.com.

For more information about ON Semiconductor visit www.onsemi.com. ◆

ECTC

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May 26 - May 29, 2020

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COUPLING & CROSSTALK

By Ira Feldman

Electronic coupling is the transfer of energy from one circuit or medium to another. Sometimes it is intentional and sometimes not (crosstalk). I hope that this column, by mixing technology and general observations, is thought-provoking and "couples" with your thinking. Most of the time I will stick to technology but occasional crosstalk diversions may deliver a message closer to home.

KGD Redux?

KNOWN GOOD DIE (KGD) – IS THIS a case of "everything old is new again" or acid reflux from a mature semiconductor industry? **Today there is a greater need than ever to know that a given semiconductor die is good before proceeding to package it.** This particular quest for the holy grail has provided plenty of challenges and indigestion to test engineers, packaging engineers, and product manager alike. Through the years some have even argued that KGD are unobtainable.

The bottom line is that KGDs are important to your business! **KGDs are essential to make today's advanced packaging economical.** With the demise of Moore's Law, the complexity of advanced packaging will increase as companies innovate. As a community of electronics professionals, we need to come together to determine "what is good?" and "how good is good enough?" **We need to restart the debate on the necessity of KGD since it will ultimately improve our tools and processes to economically delivery quality die.** Now is the time to revitalize the discussion at the **20th anniversary MEPTEC KGD Workshop on December 12, 2019!**

Not convinced of the importance of KGD? Let's start with a history lesson and apply the concepts to today's packaging…

In the 'old days' the integrated circuit (IC) manufacturing flow was relatively simple: Wafer Probe followed by Packaging and then Functional (often called "Final") Test. Wafer Probe checked for basic functionality of the IC die to screen out gross failures and to determine if a given die is worth packaging. Functional Test not only tested that the die was assembled correctly in the package but that it met the desired performance characteristics. If device burn-in was required to reduce infant mortality, this was performed using the packaged parts followed by another Functional Test pass to screen out devices that failed prematurely.

In the 1980 & 90s there was a lot of interest in KGD as packaging technology was pushed hard for high performance solutions. The demand for KGD grew in proportion to the rising cost of this high-performance packaging technology - everything from central processing unit (CPU) packaging to multi-chip modules (MCMs). At the time, there were empty CPU packages costing almost as much as the CPU die itself due to increasing clock speeds and thermal management requirements not to mention an increased number of connection 'pins'. And MCMs were being used to build complex system modules using more than one die. I.e. to provide functionality greater than what could be built as a single die. Many of these advanced packaging challenges faded away, removing the demand for KGD, when advanced process nodes permitted architectural solutions like multi-core CPUs to solve the performance needs.

There is a greater need than ever to know that a given semiconductor die is good before proceeding to package it.

Resurgence of complex packaging solutions have reappeared as the economics of Moore's Law have been exhausted. The cost of the latest IC fabrication process nodes with finer geometries have increased exponentially. Therefore, die shrinks using these newer process nodes to produce a smaller integrated circuit (IC) are no longer providing a cost savings. In the new era of "More than Moore", companies are turning to advanced packaging to provide differentiated solutions.

These new types of packaging include an alphabet soup of acronyms including WLCSP, FiWLCSP, FoWLCSP, 2D, 2.5D, 3D, PLP, and more. It seems like a new packaging technology or a variant is announced weekly. **Many of these solutions involve multiple die which screams for KGD since a single bad die renders the entire package as junk.**

Even the simplest (and earliest) of these packaging solutions, Wafer Level Chip Scale Packaging (WLCSP) and the Fan-in (Fi) variation, give test and quality engineers cause for concern. These are both single-die chip scale packaging (CSP) where the "packaging" is processed directly on the wafer. The wafer is taken from the IC fabrication line and has electrical redistribution layers (RDLs) applied. The RDL scale up the electrical connection from the die pitch to printed circuit board (PCB) pitch. A solder ball is then placed on each output pad in the BGA. The Functional Test is done by contacting these solder balls to provide the necessary electrical connections.

What is different about these WLCSP parts is that the **singulation** – cutting, dicing, or cleaving the wafer into individual dies – **is done AFTER** the solder balls have been placed and the parts have been tested while still on the wafer. This is unlike the traditional process flow where the only thing done after Functional Test on the singulated packaged part is a last optical inspection for cosmetic issues and placing the parts into shipping containers. Test engineers then rightfully ask: how do we know nothing has happened to the part after the "final" test? Did the singulation crack or otherwise damage the part?

Due to the high cost of test, including the challenges in handling many small WLCSP parts, it is not economical to do another Functional Test after singulation. Even with special electrical test structures, it is difficult to detect and find cracking or other physical damage to the die unless there are gross failures. Therefore, advanced optical and x-ray inspections have been added to the final inspection process for these parts. For higher value parts, or those with higher reliability requirements, a Functional Test and possibly Burn-in may still be in

order after the singulation even with the resultant increase in cost. As 'packaged parts' WLCSPs would no longer considered to be die. Let alone Known Good Die.

Fan-out WLCSP (FoWLCSP) and Panel Level Processing (PLP) use similar core manufacturing processes to WLCSP. However, both packaging processes transfer die from the original wafer to a carrier substrate making high quality die essential. "Good" die are selected after test and singulation from their original wafer and moved to carrier (wafer or panel). They are spaced further apart to accommodate "fan-out" of the RDL so ultimately the solder balls array is larger than the die size. Optionally, if spaced far enough apart additional dies and passives can be placed on the carrier and interconnected by the same RDL. This allows multiple die to be contained in one package to provide advanced functionality.

2D, 2.5D, and 3D are packaging methods for stacking die onto other die, silicon interposers, or organic substrates. These are also done with transferring die from a wafer to another assembly to become the package. Especially with the high cost of all the elements used, the highest possible die quality is essential since rework is impractical if not impossible. Sometimes the 3D assembly is done using wafer-to-wafer (w2w) bonding which bonds entire wafers together before singulating the individual "stacks". For w2w knowing the individual die quality of each input wafer is essential since the selection of the particular wafers to be bonded will greatly influence the yield.

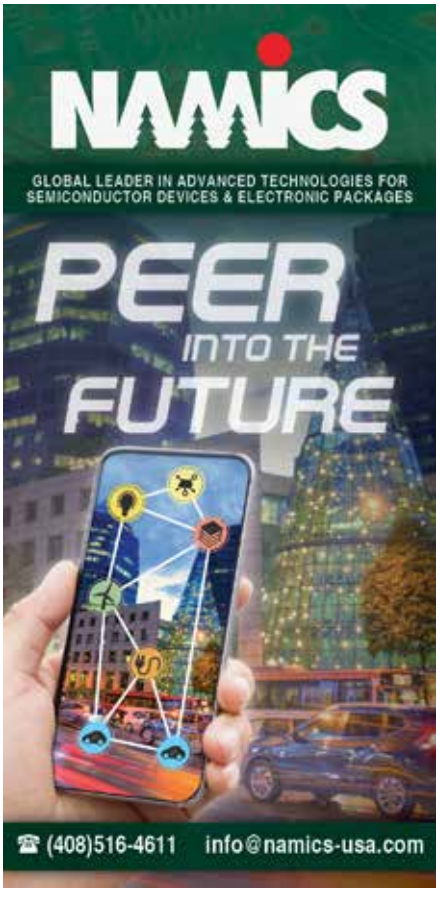
Regardless of the specifics of how each of these advanced packages are configured, having **KGD is required by any packaging technology that selectively moves a "good" die or combines a die with other die or components in a single package.** Very few, if any, of these packaging processes permit rework to replace a non-functioning die. Once the die is committed to the package or stack there are no fixes. Therefore, **KGDs are essential to having a high yield process and avoiding potential latent defects.** Without high yield, advanced packaging will not be financially sustainable to continue development let alone ramp into high-volume production.

Since the industry has largely ignored KGD for over a decade, it is time to revitalize the discussion. Up to the challenge? Need to learn more? **Please join us for the 20th anniversary MEPTEC KGD Workshop on December 12, 2019** at SEMI headquarters in Milpitas, California.

For more of my thoughts, please see my blog http://hightechbizdev.com.

As always, I look forward to hearing your comments directly. Please contact me to discuss your thoughts or if I can be of any assistance. ◆

IRA FELDMAN is the Principal Consultant of Feldman Engineering Corp. which guides high technology products and services from concept to high volume manufacturing. He engages on a wide range of projects including technical marketing, product-generation processes, supply-chain management, and business development.
(ira@feldmanengineering.com)



INDUSTRY INSIGHTS

By Ron Jones
CEO and Founder
Responsible Brands Initiative

Expert Insights Needed for New Compliance Program

THERE IS A GROWING INTEREST in corporate social responsibility (CRS) and sustainability. Consumers want to know more about the products they buy and the manufacturers of those products. It's no longer enough that a sport shoe is comfortable or long lasting, consumers increasingly want to know under what conditions it was manufactured. Consumers are also no longer satisfied that a company is a J.D. Powers winner, they want to know how a company treats their various stakeholder groups and the environment.

Unfortunately, it is very difficult for consumers to get objective and relevant data on a company's CSR and sustainability performance in an easy and timely manner. Combing through financial reports and marketing claims can confuse consumers, and few will take the time. A further complication is that the term "responsible" is used in many ways, not always objectively, which may further distract and irritate consumers. These factors tend to slow consumer purchasing decisions and may cause genuinely responsible companies to miss revenue opportunities

Defining "Responsible" Business Practices

Responsible Brands Initiative (RBI) is working to create a simple means for consumers to tell which companies are responsible in their sourcing and business operating practices. That includes developing an objective framework of metrics against which to assess organizational performance and using those metrics to define what a "responsible" company is.

To increase objectivity of the framework and eventual acceptance of the definition, RBI is reaching out to subject matter experts (SMEs) and gathering inputs on criteria that should be considered. We encourage you to participate by taking a short survey — it will take less than 8 minutes.

By gathering hundreds of inputs from SMEs in different industries and professions, we will gain a solid sense for what matters most. The criteria will be organized into logical groups, and experts in each area will consider the inputs and help distill into the foundation for a scoring system. We look forward to inputs from MEPTEC readers who have keen insights into electronics manufacturing while also being consumers.

> "Each of our stakeholders is essential. We commit to deliver value to all of them, for the future success of our companies ..." from a proclamation signed by almost 200 Industry leaders.
>
> ***Business Roundtable, August 2019***

Objective Scoring System

From the basic criteria, we will construct a scoring system to express how a company operates according to a wide variety of metrics. Our approach goes far beyond consideration of how a company treats the environment. For example, we will also consider how a company treats their various stakeholder groups: employees, suppliers, customers, shareholders and local communities. The end result of the scoring process is the RBI Index™, a numeric value for each company.

Companies that meet the required level of performance, according to RBI member-approved metrics, will be eligible to apply to use the RBI Compliant™ logo and related brand elements. This logo and other brand elements will make it simple and straightforward for a company to communicate its achievements and commitment to consumers and stakeholders while simplifying identification of desired products by consumers. Employing a single, distinctive logo will also make it very easy for consumers to know which brands are responsible.

As the brand is developed, RBI also plans extensive outreach to consumers to educate them about the myriad data behind the RBI Index, the objectivity of scoring and the simplicity of product selection. This will provide an incentive for companies to focus and boost their responsible sourcing and business operations. Companies who qualify and employ the logo will enjoy simplified marketing and gain business from increasingly sophisticated consumers and make the world a better place.

Once in production, data will be gathered from public sources and questionnaires from participating companies. The metrics, framework and RBI Index for a particular company will be transparent to the world. Raw scoring data of a company will be available to the company. Audits will be performed to validate authenticity of scoring information.

Broad, Collaborative Process

Similar to processes used by industry standards organizations, we anticipate several iterations to define and refine criteria and scoring. Each pass will build on previous work and will involve increasing numbers of SME's and consumers. Once the criteria are distilled into a framework, we will be polling experts from multiple industries to help weight the metrics and complete the final draft of the scoring system. Eventually, corporate members of the Responsible Brands Initiative will vote to adopt the metrics and scoring process leading to RBI Index values.

We Need Your Input

As an industry association, RBI collaborates with subject matter experts (both employees of member companies, and interested individuals) in many industries. Involvement of experts from a broad range of manufacturing and service industries will assure the new compliance performance metrics and weighting parameters are balanced and objective. Inputs from customer-facing corporations, non-governmental organizations (NGOs), colleges and universities will assure the RBI Index reflects a broad range of insights.

MEPTEC readers have a unique perspective that combines keen, in-depth insights about electronics manufacturing. Your input at this early stage will have maximum impact and value. Click here to complete a short, 6-7 minute survey. Afterwards, you can register to receive

continued from page 11

results from the surveys. ◆

Responsible Brands Initiative is registered in the State of Oregon, operates as a 501(c)(6) nonprofit corporation, and is independent any single corporation, or government agency.

RON JONES is CEO of Responsible Brands Initiative (RBI), a non-profit that monitors Corporate Social Responsibility and Sustainability performance. Data includes multiple company stakeholders: employees, customers, suppliers, communities, shareholders and the environment. RBI makes the objective and balanced information available to enable consumers to make more responsible choices.

Email ron.jones@responsiblebrands.org for more information.

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Inline Process Control and Inspection: Enabling the Next Generation of Advanced SiP Manufacturing

David L. Adler, Ph.D.
SVXR Inc.

IC PACKAGES ARE BECOMING more complex and difficult to manufacture, with a goal of ever fewer – or even zero – manufacturing defects. These pressures can increase development times, production risks and manufacturing costs. Better inline inspection and process control tools can help. A new x-ray technology, developed specifically for advanced packaging, detects subtle process changes that affect yield and reliability. The system uses high-speed imaging--up to 100x faster than existing x-ray systems – and advanced machine learning techniques to capture process changes and latent defects that impact product yield and reliability. The result is real-time process control and defect detection for advanced packaging.

In his 1965 seminal paper, Gordon Moore predicted an exponential increase in the "number of components per integrated function" that came to be known as Moore's Law. For fifty years, Moore's Law was driven by shrinking transistor size. In the last few years, shrinking transistors has become very expensive. In a departure from Moore's original observation, the least expensive transistor is no longer the smallest transistor. Advanced IC packaging has replaced shrinking transistors as the driving force behind Moore's Law. One package combines multiple IC's into Moore's "integrated function". Moore's Law continues, not at the IC level but rather at the package level.

Getting multiple IC's to function like a single IC requires a lot of connections between IC's. Advanced packaging makes use of direct solder connections, rather than wire bonds, to make these connections (Figure 1). This improves performance by allowing for a high density of short, fast connections between

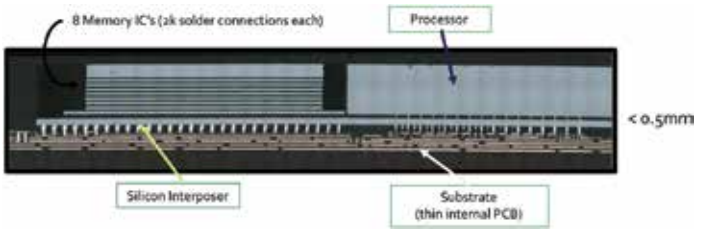

Figure 1. Package complexity is increasing dramatically. 2.5D package shown combines a memory stack with an application processor. This package has well over 100,000 solder connections.

IC's. Some IC packages have close to one million connections, a number that will undoubtedly continue to grow.

As packaging technology evolves, the technology to produce IC packages needs to evolve as well. In particular, the defectivity of the electrical connections must be reduced dramatically. For each increase in the number of electrical connections, the defectivity must drop by the same amount, just to maintain constant yield. In addition, the size of a "critical defect"—one that can cause a failure—gets smaller. Smaller defects are more numerous than large defects. Without improved process control, yields will drop rapidly.

The revolution in IC Packaging thus drives the need for new inspection and

Inspection Item	2D AOI	3D AOI	Strip level 2D Xray
Die Chipping / Crack	Yes	Yes	?
Standing / Tombstoning	No	Yes	Yes
Misplace / Misalign	Yes	Yes	Yes
Missing	Yes	Yes	Yes
Solder Wetting (over, non)	Yes	Yes	Yes
Solder Bridge (short)	Yes	Yes	Yes
SMT / Crack	Yes	Yes	?
Extra Component	Yes	Yes	Yes
Double Component	No	Yes	Yes
Rotated Component	Yes	Yes	Yes
Die Tilt	No	Yes	?
CuP non-wet	No	No	Yes
SMT non-wet or insufficient solder	No	No	Yes
008004 SMT shorting	No	No	Yes
PCB via voids	No	No	Yes
Solder voids	No	No	Yes
Top and Bottom Assembly	2x	2x	1x
Embedded components	No	No	Yes
Stack Die	No	No	?
Die Attach coverage	No	No	Yes

Figure 2. Analysis by large semiconductor company comparing types of defects caught by 2D and 3D automated optical inspection (AOI) and 2D x-ray inspection.

Figure 3. Four types of x-ray systems. Inline inspection for advanced IC packaging requires both high resolution and high speed imaging.

metrology tools, with both greater sensitivity and higher throughput. The primary tool for inline inspection today is Automated Optical Inspection, or AOI. AOI is fast and automated, but cannot inspect solder connections between components (Figure 2). Because x-rays can penetrate through the package, X-ray inspection systems can inspect solder connections inside the package; however, existing x-ray imaging technology cannot meet the requirements for inline inspection of advanced packages.

Inline x-ray inspection is widely used in manufacturing, including electronics (Figure 3). Indeed, many PCB assemblies require 100% x-ray inspection to insure quality and reliability. Thinking of an advanced IC package as a "small PCB assembly", it is natural to ask whether the systems used to inspect populated PCB's can be extended to advanced packages. Until now, the answer was no, they cannot. The technology used in PCB assembly inspection are traditional x-ray systems: they use off-the-shelf components—x-ray source and detector. The throughput of traditional x-ray systems goes inversely as the cube of the resolution: a factor or 10x in resolution, from 25 microns to 2.5 microns, reduces the throughput of the system by a factor of 1000x. This substantially increases the cost of inspection, making it prohibitively expensive for inline inspection for advanced IC packages.

The imaging speed of a traditional x-ray system is limited by the "usable" x-ray power available (Figure 4). An imaging system with 2.5 microns of resolution has an x-ray source with about 2.5 watts of power. Taking images with a 2.5 watt x-ray source is akin to taking photos

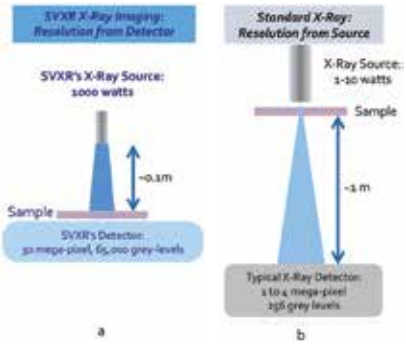

Figure 4. (a) Traditional x-ray imaging systems: the resolution comes from the x-ray source, limiting power to a few watts for high resolution; (b) SVXR's new x-ray imaging system: the resolution comes from the detector, allowing for higher power and larger field-of-view.

by the light of a 2.5 watt nightlight. Exposure times are long, because there isn't much light.

The SVXR X200 uses a new type of x-ray source that has 1000 watts of power. Combining this new source with a proprietary 30-megapixel detector, the X200 is able to take images up to 100x faster than a traditional x-ray system. In addition, SVXR's detector uses astronomy-grade sensors that have much lower noise than traditional x-ray sensors, resulting in very high-dynamic-range images (HDR). This can be especially useful for detecting defects that lack a strong signal, e.g. aluminum wedge-bonded wires.

Figure 5a shows an image from SVXR's X200 inspection system. The FOV is 12 mm x 18 mm. The test sample is a programmed-defect test vehicle for non-wet solder joints. Each unit has 90 solder connections to be inspected (Figure 5b). The image collection time is two seconds. Figure 6a shows the results of the defect detection algorithm, which runs concomitantly with the imaging. Each solder connection is evaluated on many different factors, and a "solder quality" metric is produced. Each solder connection is then labelled as "good", "bad" or "marginal", and a heat map of the part is produced. The X200 results are well-correlated with 3D CT cross-sections of the same connections (Figure 6b).

Figure 7 shows another analysis of the SVXR images, this time on system-in-package (SiP) production parts. The parts were produced using three slightly different process parameters. Lot 1 was produced according to the nominal process,

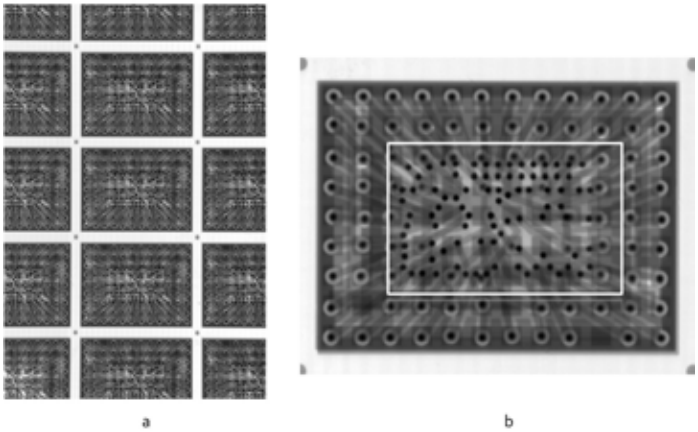

Figure 5. (a) Full field-of-view (12x18 mm) image of non-wet test sample. (b) Close-up image of one IC package. Solder test connections are inside white box.

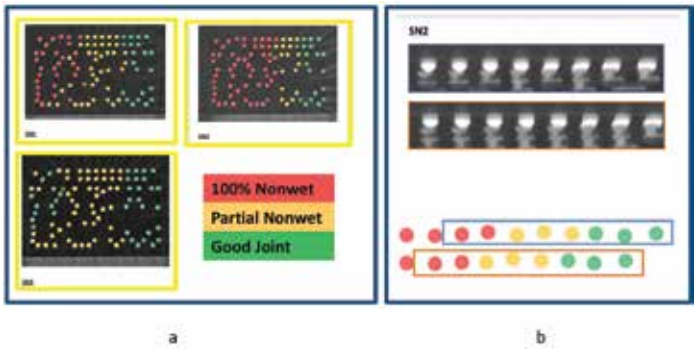

Figure 6. (a) Heatmap showing locations of "Good", "Partial Non-wet" and "100% Non-wet" connections; (b) 3D CT cross-sections of top two rows of part SN2.

but with a standing time before reflow at the upper limit of the acceptable process window; Lot 2 was produced nominally, but with the reflow over at the upper limit of temperature; and Lot 3 was produced at ideal process parameters. Lots 1 and 2 have been linked to higher long-term reliability defects in the field. All lots would pass electrical test, and it is not possible with x-ray of any kind to differentiate between these parts: they look identical to the human eye.

Using advanced machine learning algorithms (ML), we combined data from all the inspected solder connections on each part. We used supervised learning to create the algorithms, and then tested about 170 parts of each lot. The ML algorithms were able to clearly determine which process lot each part had come from. This demonstrates the process sensitivity of the X200, which is needed to provide advanced process control.

The rapid improvement in packaging technology requires a corresponding improvement in process control and defect detection for high-volume manufacturing. Existing optical tools cannot detect solder defects between components; existing x-ray inspection tools are too slow at the required resolution. A new x-ray imaging technology, developed by SVXR, is able to provide both high imaging speed and high resolution, along with a high dynamic range for detecting subtle defects in advanced packages. The high throughput makes the system cost-effective for inline, 100% inspection. ◆

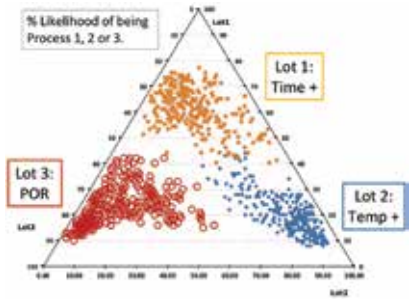

Figure 7. Classification of 3 lots of parts, varying: the staging time before reflow *(lot 1)*; the reflow temperature *(lot 2)*; and the nominal process-of-record *(lot 3)*. The three lots are clearly differentiated by the algorithms.

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Accelerate the Development of Advanced IC Packages Using 3D X-ray Microscopes to Measure and Characterize Buried Features

Thom Gregorich and Allen Gu
ZEISS Process Control Solutions

REDUCTION IN PRODUCT DEVELOPMENT cycle time and improvements in early product manufacturing yields are strategic objectives for many technology-driven firms. At the same time, product complexity is increasing, especially in areas such as IC packaging where the DRAM "wall" and the slowdown in Moore's law are pushing product performance improvements from the silicon and into the IC package. These goals may conflict, however, and firms might be forced to consider trade-offs between product performance and packaging yields.

As shown in Figure 1, for nearly 40 years the IC packaging industry has relied extensively on physical cross-sectioning to view and measure buried interconnects. New technologies such as 3D X-ray microscopes are needed to provide submicron-resolution, semi-automated measurement of buried interconnects in advanced packages. These solutions will help to enable faster time to market by reducing learning cycles through delivery of richer, higher-accuracy engineering data compared to traditional destructive methods.

Acceleration of Package Interconnect Scaling

Dennard Scaling and Moore's Law drove performance improvements in the semiconductor industry for nearly 50 years. In this environment it was often more beneficial to scale features in the silicon than to scale features in the IC package. As a result, package technologies tended to focus on feature sizes that could be manufactured without sophisticated process controls.

However, Dennard Scaling peaked in the early 2000s and Moore's Law has slowed to the point where nearly all leading electronics companies are searching for advanced package-level solutions to improve product performance[1]. These advanced package-level solutions are pushing packages out of their traditional comfort zones and into technologies which require advanced closed-loop process controls. As shown in Figure 2, the minimum practical flip chip pitch was considered to be around 150 μm when IBM began to commercialize C4 flip chip BGA technology in the 1980s. A 150 μm pitch C4 flip chip results in a maximum interconnect density of around 50 I/O per mm^2 and can be assembled with relatively high-yields without complex process controls. In the early 2000s Cu-pillar flip chip was first commercialized; use of Cu-pillar enabled significantly finer interconnect pitch than C4 flip chip because the solder fillet shape was easier to control. A 100 μm-pitch Cu-pillar flip chip has a maximum interconnect density of 100 I/O per mm^2 and can also be assembled with relatively high-yields without complex process controls.

Figure 1. Optical inspection circa 1970.
Courtesy Intel Museum Archives

High Bandwidth Memory (HBM) and Hybrid Memory Cube (HMC) pioneered the mass-production of high-density 50μm pitch Cu micro-pillar interconnects. These micro-pillars feature an interconnect density of 400 I/O per mm^2 and require more sophisticated process controls to maintain acceptable yields. Going forward, future generations of advanced memory integration and logic "disaggregation" technologies such as chiplets will drive flip chip interconnect pitch down to 40 μm, 30 μm, 20 μm and even 10 μm! As the interconnect pitch approaches and scales below 40 μm the following changes are expected[2]:

- The solder cap will become smaller and will evolve into a thin solder coating
- The solder coating on the Cu-pillar will eventually be replaced by Cu-to-Cu diffusion bonding

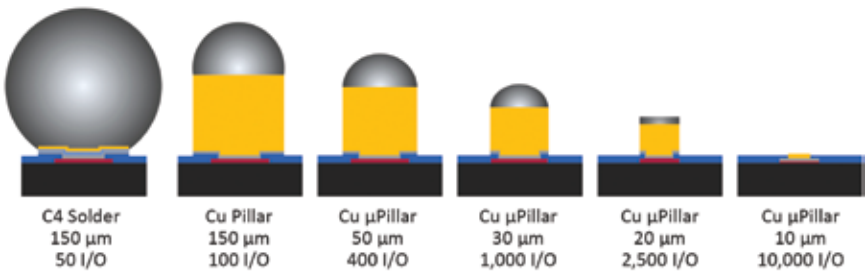

Figure 2. Flip chip interconnect roadmap from C4 solder to direct Cu (150 µm to 10 µm).

- At all levels of pitch evolution, process characterization and process controls will become more and more critical, and will exceed the capabilities of existing package engineering inspection and measurement systems

Comprehensive Process Control Systems in Wafer Fabs

In the late 1980s wafer fabs began to deploy sophisticated optical inspection and closed-loop process control systems[3]. These control systems were vital to realizing the performance improvements predicted by Dennard Scaling and Moore's Law, while at the same time accelerating yield learning (e.g. the speed of improving yield) ultimately speeding-up time to market. Unfortunately, advanced package assembly often relies on bumped interconnects and the optical systems developed for wafer fabs are not usable with these "buried" interconnects. New, advanced inspection and measurement technologies are needed to achieve accelerated yield learning for advanced IC packages as there is a lot at stake.

The Cost of a Packaging Delay

Delays in solving package development problems can result in missed product shipments. While numerous scenarios have been developed for calculating the cost of a product delay, we are going to use a simple model here which assumes that a delayed IC package results in a first-year loss-in-revenue which is proportionate to the length of the delay. As shown in Table 1, the cost of a one-quarter packaging delay for a product would be 25% of the first-year revenue, or $2.5M in the case of a product with $10M in first-year revenue.

1st Year Product Revenue	Lost Revenue Due to 1 Quarter Delay
$10M	$2.50M
$50M	$12.5M
$100M	$25.0M

Table 1. Cost of package delay.

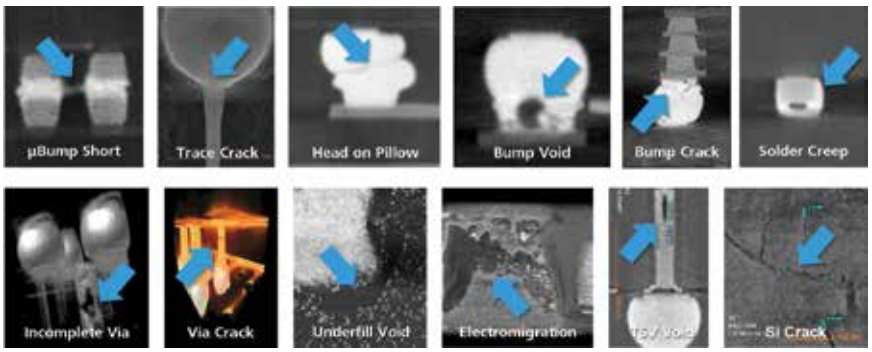

Figure 3. Virtual cross-section images extracted from 3D datasets generated by XRM.

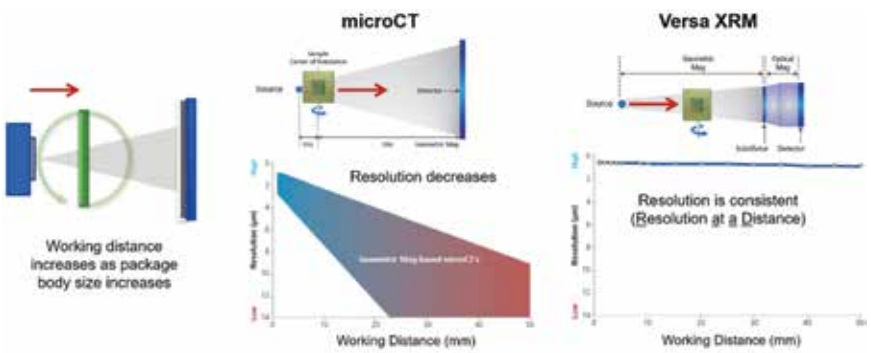

Figure 4. Comparison of X-ray microscope to microCT.

X-ray Microscope: Leading Technology for High-resolution, Non-destructive Package Analysis

For nearly a decade the X-ray Microscope (XRM) has been the leading technology for high-resolution, non-destructive analysis of buried defects in IC packages[4]. XRM imaging is often used in the failure analysis workflow to image suspected locations of electrical failures prior to physical failure analysis. Figure 3 shows examples of the wide range of package defects that can be imaged by an XRM. Because an XRM can provide advanced knowledge of the physical characteristics of the failure, such as size and orientation, it helps improve the success rate of physical failure analysis thereby improving the chance of successfully determining the root cause of the failure. It is for this reason that nearly every failure analysis lab in the world for advanced packages uses an XRM.

X-ray microscopes are often chosen over microCT-based X-ray systems because XRMs do not lose resolution as package body size increases, as shown in Figure 4. For both microCT and XRM systems, the process of generating 3D images is accomplished through computed tomography, which requires samples to rotate at least 180°. Since samples are rotated, they must be moved far-enough away from the source to avoid colliding with it. This increase in distance has an adverse impact on microCT-based systems because resolution degrades as the sample moves away from the source; XRM systems use optics to compensate for the increase in distance and thus do not loose image resolution.

Inspection and Measurement of Buried Features in Advanced IC Packages

Carl Zeiss SMT, Inc. has developed an inspection and measurement system for buried features in advanced IC packages using the proven ZEISS Xradia 620 Versa X-ray microscope. This system, called RepScan, extends the application of the Versa XRM into the areas

Figure 5. 620 Versa RepScan system components.

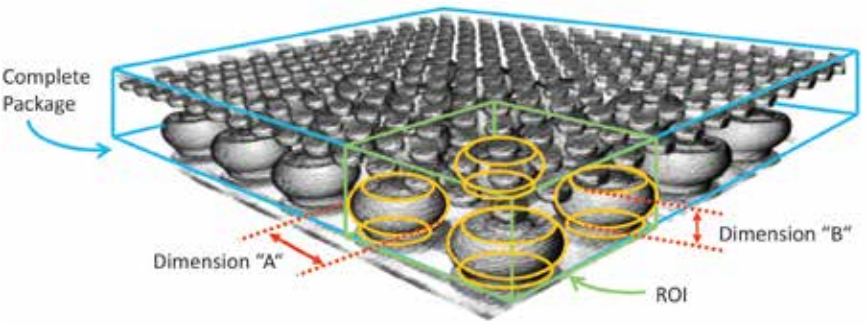

Figure 6. Package Region-of-Interest (ROI) and critical dimensions.

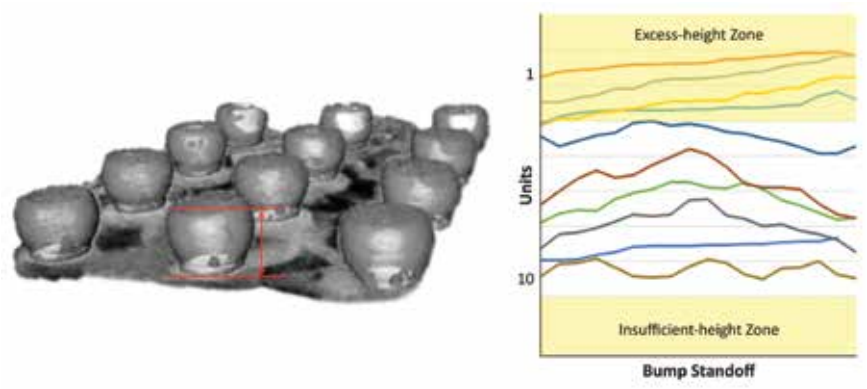

Figure 7. Analysis of flip chip bump standoff.

of process and product development by enabling non-destructive, submicron-resolution semi-automated 3D imaging and measurement of advanced IC packages. RepScan is optimized for characterization of buried high-density package interconnects and includes the following major components, as shown in Figure 5:

- 620 Versa X-ray Microscope
- Versa Autoloader
- Automatic Tomography Acquisition (ATA) System
- Data analytics Workstation
- 3D Data Analytics Software
- Optional Mass Storage System (not shown)

The RepScan system includes a patented Automatic Tomography Acquisition system that enables automated loading, scanning and unloading of identical samples without the need for operator intervention. Scan results may be automatically transferred to a separate workstation where a variety of measurements may be executed semi-automatically. This establishes a new benchmark for non-destructive measurements that support process optimization, product development and QA/QC of complex fine-pitch 3D architectures, including 2.5D interposers, high bandwidth memory stacks with TSVs and microbumps, wafer-level packages with package-on-package interconnects and ultra-thin memory with multiple chips in a stack.

Versa RepScan Case Studies

As shown in Figure 6, RepScan addresses many of the limitations of physical cross-sectioning and offers new capabilities:

- Enables statistically-valid sample quantities with semi-automated, highly repeatable linear as well as volumetric measurements
- Improves the ability to detect anomalies because samples can be imaged and measured in any direction
- Allows for further testing of samples after analysis because the RepScan methodology is non-destructive

Below are three sample case studies which demonstrate the capabilities of Versa RepScan measurement:

- Flip Chip Bond Line Thickness
- Flip Chip Solder Fillet Extrusion
- Flip Chip Solder Bump Wetting

Case Study #1: Flip Chip Bond Line Thickness

Flip chip bond line thickness is one of the most important factors to be considered when designing a bumped joint, as there are electrical, mechanical, thermal as well as underfill considerations. Bond line thickness is generally not uniform across the die due to factors such as warpage and tilt. In addition, as geometries decrease and as processes migrate from mass-reflow to thermo-compression bond, measurement and control of bond line thickness becomes even more critical.

As shown in Figure 7, the 3D X-ray dataset was used to identify the boundary between the solder and the Cu pad/pillar. 3D X-ray images can effectively determine the exact location of this boundary using material segmentation (i.e., the transition from Cu pad/pillar to Sn-based solder).

Case Study #2: Flip Chip Solder Fillet Extrusion

Solder fillet shape in mass reflow is determined by a number of factors including solder volume, pad size, solder wetting, component mass, etc. Ultimately

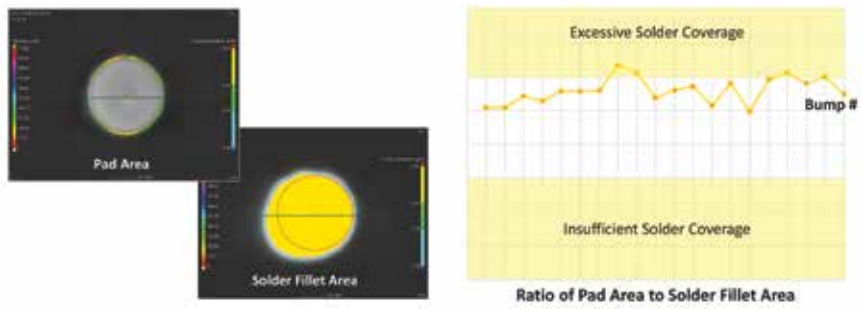

Figure 8. Analysis of flip chip solder fillet extrusion.

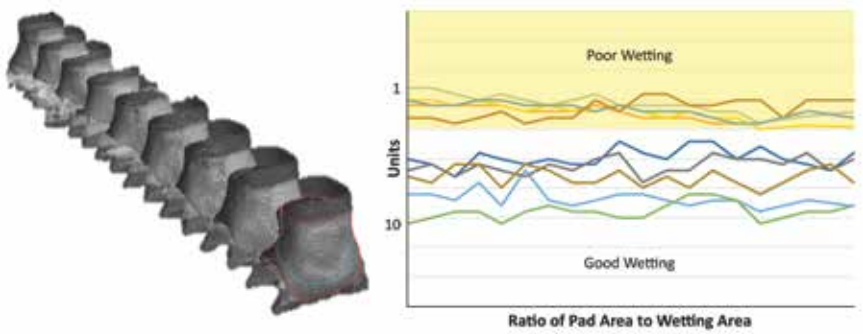

Figure 9. Analysis of flip chip solder wetting.

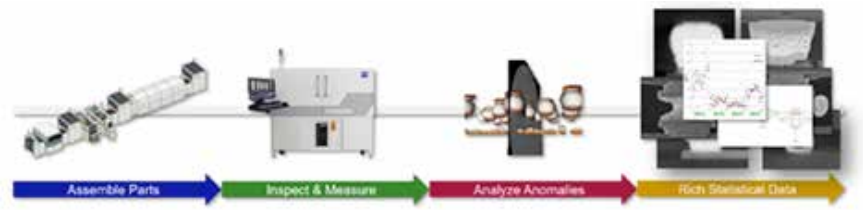

Figure 10. Construction Analysis Workflow.

these factors interact with each other and a solder fillet is created which balances all of the forces. However, as bump and pad sizes are reduced, mass reflow is often replaced by thermo-compression bonding. A key difference between the two soldering methods is that with thermo-compression bonding, bond-line is determined by the position of the bond head and that the device being soldered is not free to "float". As a result, small variations in pad geometry, solder volume, solder wetting and tool setup can result in excessive variation in solder fillet extrusion.

As shown in Figure 8, the 3D X-ray dataset was used to compare the area of the Cu pad/pillar with the maximum area of the solder fillet. The solder fillet shape is determined in all directions on a 2D plane, not just a single direction based on a cross-sectional cut. By comparing the ratio of the solder fillet area to the pad area, we can assess and measure small variations in the bonded interconnect system.

Case Study #3: Flip Chip Solder Bump Wetting

Soldering is a complex chemical process which enables the creation of reliable, low-resistance electrical interconnects between mechanical structures at relatively low (~250°C) temperatures. Good solder wetting is vital to electronics system performance and to reliability; however, wetting itself is difficult to measure. Solder wetting on leaded components can be assessed by the meniscograph (wetting balance) method, but this technique is highly subjective and is not appropriate for small surface-mounted interconnects such as flip chip bumps. As a result, flip chip technology often relies on destructive approaches such as die-shear to indirectly assess the quality of solder wetting.

As shown in Figure 9 (Cu-pillar bump-on-trace), the 3D X-ray dataset was used to calculate the area of the interfaces between the solder and the Cu pad/pillars. As previously mentioned, 3D X-ray imaging is effective at determining the exact location of this boundary because the transition from Cu pad/pillar to Sn-based solder can be detected by the system. Using proprietary algorithms, the areas of these interfaces were compared and used to assess the quality of the solder wetting.

Summary

The use of Versa RepScan enables the extraction of richer statistical data from engineering builds which would have been lost if traditional methods such as mechanical cross-sectioning were used, as shown in Figure 10. Better data extraction results in more accurate statistical analysis and enhanced ability to detect low-level defects, as compared with traditional mechanical cross-sectioning. As a result, products can be developed and launched faster, with fewer cycles of learning and with higher, more stable assembly yields. ◆

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Packaging & Assembly for High-Temperature Electronics

Part IV – Materials Behavior – Mechanical

Dr. Randall K. Kirschman
R&D Consultant for Electronics Technology

PART I OF THIS SERIES INTRODUCED semiconductor devices and their general high-temperature capabilities that must be accommodated by assembly and packaging, followed by a glimpse of assembly and packaging materials and technology in regard to high-temperature operation.

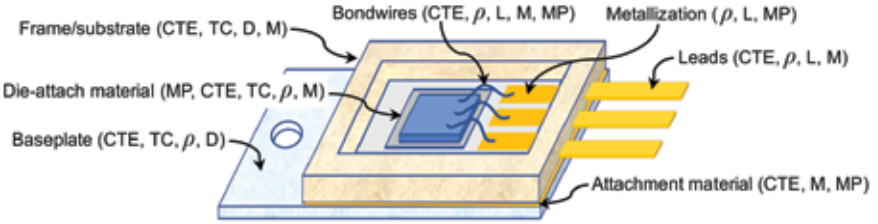
Parts II, III and IV focus on basic behavior of assembly and packaging materials at high temperatures, to 500–600°C, considering the properties indicated in Figure 1. **Part II**, explored *thermomechanical and thermal* properties, and **Part III**, in the previous issue, explored basic *electrical* properties. **Part IV**, in this issue, explores a few relationships between high temperatures and basic *mechanical* properties.

Ceramics and Other Non-Metals

Ceramics for packaging include *alumina* (Al_2O_3), *aluminum nitrid*e (AlN), and *silicon nitride* (Si_3N_4)—all polycrystalline. *Fused quartz* (amorphous SiO_2), *sapphire* (single-crystal Al_2O_3), and *diamond* (single-crystal or polycrystalline C) are additional, non-ceramic, dielectric materials sometimes used in assembly and packaging.

The most relevant mechanical properties include *flexural modulus* (bending stiffness), *flexural* (bending) *strength*, *tensile strength*, and *fracture toughness*. These properties vary with the type of material, but may also vary among different samples of the same material type because of small differences in microstructure[1].

However, with suitable materials choices, variations over the room-temperature to 600°C range can be relatively small. Thus, setting aside the question of adequacy for a particular design, changes with increased temperatures, per se, should be a minor concern. Differences in mechanical properties among these materials, rather than their temperature dependence, are typically of greater relevance.



(CTE = coefficient of thermal expansion, TC = thermal conductivity, ρ = resistivity, L = inductance, D = dielectric constant and loss, M = mechanical, MP = melting point†)

Figure 1. A generalized package and basic materials properties relevant for high temperature operation. Any overcoat/encapsulation is not shown. *(Repeated from Part II and III.)*

On the other hand, properties such as thermal expansion, thermal conductivity, and electrical resistivity vary considerably with temperature, as well as with material type. (*See Parts II and III*) If an assembly is subject to wider temperature cycles as part of high-temperature operation, thermal-expansion differences and associated mechanical properties will be a major factor in materials choices and structural design[1] [Manufacturers' datasheets]. (*See Part II*)

As mentioned earlier, plastics are generally limited to below 250°C. (*See Parts I and II*)

Metals

Considering *structural metals*, e.g. Al, Cu, Ni-Fe, Kovar®, and Alloy 42—even at 600°C the latter three are at $T_H \approx 0.5$ and Cu is within the recommended T_H of $\approx 2/3$.‡ Thus, their changes in mechanical properties should not be a concern over the RT–600°C range. An exception is Al (and thus composites such as Al/SiC and Al/C), which loses strength rapidly and becomes prone to restructuring as its melting point (MP = 660°C†) is approached: e.g. 500°C corresponds to $T_H > 0.8$ for Al.

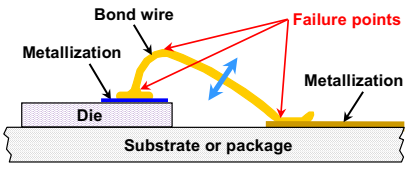


Figure 2. Differences in CTE between bondwires and package coupled with cycling, or heating, can flex and fatigue bondwires to failure (blue double arrow).

What about *bonding wires and ribbons*, e.g. Al, Au, and Cu? The MPs of Au and Cu (≈1100°C) are well above the temperature range considered here ($T_H < 2/3$ at 600°C). Even so, annealing and weakening can take place at temperatures as low as ≈ 300°C in Au bondwires, and at even lower temperatures in Al bondwire, but the remaining strength may well be adequate and no cause for concern.

However, thermal-expansion mismatch can result in metal fatigue and failure from temperature and power cycling (Figure 2). Progression to failure is often self-accelerating because of increasing current crowding and decreasing thermal conductivity. Bondwires of Al (and doped Al)—because of its lower MP—is particularly susceptible to restructuring (Figure 3)[2].

An additional consideration—apart

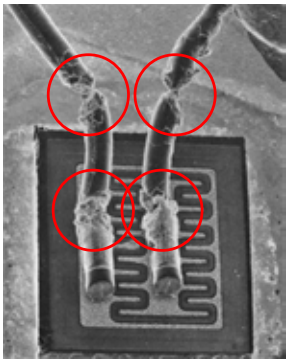


Figure 3. Example of restructuring and failure of Al bondwires[2].

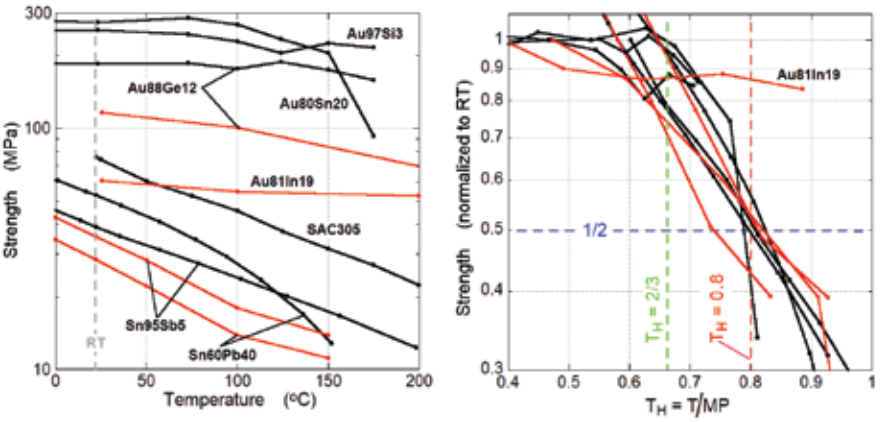


Figure 4. Examples of *tensile strength* (black lines) and *shear strength* (red lines) for solders: strength-vs-temperature *(left)* and normalized strength-vs-T_H for the same solders *(right)*
Tensile strength and shear strength data for a solder may be from different sources.[Data from [4][5][6][7].]‡

from the bond wire itself—is that if the bond wire and metallization are of different materials there is a strong possibility of interactions that could seriously alter the mechanical properties of the bond[3].

Solders

Typically, the most critical mechanical properties are those of solders.‡ Solders are a serious concern for high-temperature packaging and assembly because they are likely to be used at high T_H, i.e. close to their MPs. Moreover, although values of T_H are typically based on *ambient/environmental* operating temperature, high-power semiconductor devices can subject die-attach materials to even higher temperatures and T_H values, intermittently or continuously. When metals are at temperatures near their MPs, the microstructure-mechanical properties relationship becomes complicated; the result is often degradation of performance.

Furthermore, even though solders are an essential ingredient of electronic packaging and assembly, finding basic data on their properties for temperatures much above the "standard" (–55°C to +125°C) temperature range is distressingly difficult! Most high-temperature investigations of solders are of isothermal aging and temperature cycling.

The limitations of solders for high-temperature operation were touched on in Part I; the basic, ultimate limitation being MP. But how close to their MPs can solders be used reliably? T_H can serve as a guide: a solder loses strength rapidly as its temperature approaches its MP, in other words as T_H approaches 1. Figure 4 *left* presents examples of *tensile strength* and *shear strength* for several solders[4][5][6][7]. (Other solders behave similarly.) Shear strength is likely more relevant because joints will primarily experience shear stress from thermal-expansion mismatch. As shown, both tensile and shear decrease with increasing temperature. Figure 4 *right* is an alternative plot of the same data: strength normalized to its RT value *versus* T_H. Plotted in this manner, the different alloys exhibit similar behavior, and exhibit a reduction in strength to ≈ ½ at T_H = 0.8.

Mechanical engineers recommend operation below $T_H \approx 2/3$; however, even the upper limit (+125°C) of "standard" temperature-range electronics can subject Pb63/Sn37 (MP = 183°C) and Pb-free SAC305 and SAC405 (MPs = 217°C) solders to $T_H \approx 0.8$ or higher (Figure 5 blue squares).

Anyway, as temperature increases, these solders are phased out because of their low MPs. Even higher-temperature, high-Pb solders (Pb > 85% MPs ≈ 300°C), and "hard" Au-based, solders: Au80/Sn20 (MP = 280°C), Au88/Ge12 (MP = 356°C), and Au97/Si3 (MP = 363°C), are limited in applicability, depending on how high a T_H designers are willing to risk (Figure 5). The 350–600°C range requires even higher-temperature solders or alternative joining techniques such as sintering of Ag or Cu particles or the various transient joining techniques[8][9]. (*See Part I*)

Additionally, during use, time and temperature cycling will enter the equation: *creep* (permanent, progressive deformation under constant stress) and related *stress relaxation*, driven by CTE mismatch, escalate as a solder approaches its melting point, i.e. at high T_H (Figure 6)[5].

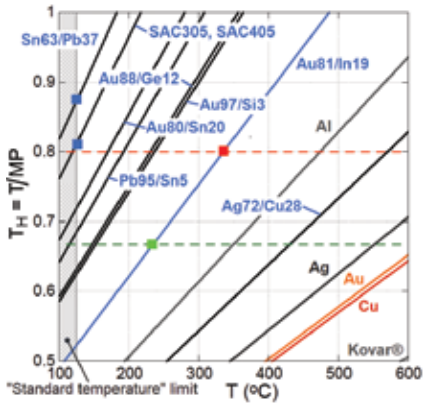


Figure 5. T_H values corresponding to possible operating temperatures for solder/braze alloys and metals used in packaging. Example: Au81/In19 (blue line, MP = 487°C) operated at $T_H \approx 2/3$ is 234°C ■, or at $T_H \approx 0.8$ is 335°C ■.‡

Thus far, only the properties of the solder itself have been considered. Increasing temperature also means more thermal energy available to enable interactions with adjacent materials. The resulting alloying and intermetallic compounds can have a profound effect on mechanical properties, as well as thermal and electrical properties. Although such interactions are usually undesirable, there are exceptions, for example, in the form of the transient joining techniques.

Solder joints are complex and involve myriad factors, which need more attention as temperature is increased. This com-

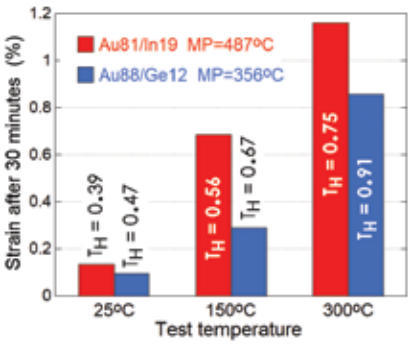


Figure 6. Examples of creep for two alloys under 34.7 MPa stress Data from [5]**; the creep rate increases ≈ 10 x between RT and 300°C.**

plexity is beyond the scope of this brief article. Nevertheless, the basics treated above are a first consideration.

Package/Assembly System

A package or assembly must be viewed as a *system* in which the thermomechanical, thermal, electrical, and mechanical behavior of the various assembled materials cannot be considered in isolation. Consequently, in addition to the properties of a material and possible changes within a material, the often complex relationships and interactions among materials must be considered both during fabrication and during operation, especially as temperature is increased. Too often, when characteristics of materials are considered and compared in reference to high-temperature electronics, only characteristics at *room-temperature* are taken into account, and changes with increased temperature receive scant attention.

Furthermore, this *system* must accommodate all aspects of the use environment in addition to temperature. High-temperature uses may include high vibration and shock (e.g. jet engine, geothermal, automotive, spacecraft, and industrial uses) as well as radiation, electromagnetic stresses, and moisture or other hostile atmospheres. Also, the system may see very low temperatures (e.g. aircraft, vehicles, and spacecraft).

Caution

The data in Figures 4 and 6 are derived from particular materials specimens and are not universally applicable: much depends on materials conditions, fabrication and processing details, test parameters, aging, and history. Thus, the data for other materials and situations may differ considerably from those shown. The purpose of the Figures is to indicate typical trends with temperature rather than provide general numerical values.

Summary

This article and the preceding two articles have examined the inherent and unavoidable high-temperature trends in basic materials properties that designers must face. These articles are not meant to address materials properties in general, but only to consider the consequences of high-temperature operation. Nor do they go deeply into the subject: a great deal more could be said about materials in relation to high-temperature packaging and assembly.

The bottom line is that as environmental/operating temperature is raised, electronics packaging and assembly will be increasingly challenging in terms of thermomechanical, thermal, electrical, and mechanical aspects and the range of suitable materials will narrow. But perhaps the essential question is—in spite of the tendency of materials toward contrariness at high temperatures—whether the particular package/assembly can be designed to meet performance, reliability, and life requirements for the intended application.

Packaging and assembly will continue their key—and often underappreciated—role in extending the temperature range of electronics. Revised designs, alternative materials, and innovative techniques will be needed. Did anyone say that it was going to be easy? ◆

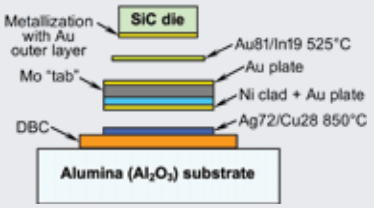
Acknowledgements

I am indebted to Rich Grzybowski (MACOM), Colin Johnston (Department of Materials, University of Oxford), Harold Snyder (Physical Solutions Group), and Paul Vianco (Sandia National Laboratories) for reviewing this article and for valuable suggestions.

Notes

†Melting point (MP) as used here means the temperature above which the material is no longer solid, and thus can be the material's melting-point temperature (for elements or compounds), or eutectic or solidus temperature (for alloys).

Three concerns that increase with temperature are (a) interaction of solder/braze materials with adjacent metals/metallization in a joint, (b) stress from thermal expansion differences, and (c) T_H rising towards unity.



Example of an assembly system for 400°C operation using Ag/Cu and Au/In brazes. (850°C and 525°C are assembly temperatures; drawing is based on description[10])

Above is an example of an attachment system for 400°C operation that addresses these three concerns[10]. A Ag/Cu (eutectic MP = 780°C) braze is followed by a Au/In (eutectic MP = 487°C) braze (step brazing). A Mo tab between the brazed joints serves as a barrier to undesirable metallurgical interactions as well as a buffer between differences in thermal expansion. Even so, a major concern with this arrangement would be stress from the thermal-expansion difference between the DBC (direct-bonded Cu) and the alumina substrate over a wide temperature range[11]; thermal-expansion differences are a major bugbear of packaging and assembly. *(See Part II)*

For 400°C operation the Ag/Cu braze has a comfortable $T_H \approx 0.64$. The Au/In braze would be at a less comfortable $T_H \approx 0.88$, but a transient-liquid-phase (TLP) interaction between the Au/In and the Au metallizations on the die and Mo tab could raise the re-melt temperature and reduce T_H. This latter is an instance of a desirable interaction.

ǂHigher temperature (≈ > 300–400°C, although definitions differ) joining materials are usually referred to as *brazes*. As used in this article, "solder" may include both solders and brazes.

‡An introduction to *homologous temperature*, T_H, appeared in **Part I** (sidebar). In these articles homologous temperatures are based on a material's melting point (MP).

Room temperature (RT) is taken to be +22°C.

SAC305 = Sn96.5/Ag3/Cu0.5; ***SAC405*** = Sn95.5/Ag4.0/Cu0.5. High-temperature electronics may be excluded from Pb-free RoHS, e.g. RoHS Annex III, 7(a), May 2018.

Kovar® is Fe/Ni29/Co17 ASTM F-15 or UNS K94610 (MP ≈ 1430°C). ***Alloy-42***, used for leadframes and seals, is Fe/Ni41-42 ASTM F-30 or UNS N94100 (MP ≈ 1450°C).

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Dr. Randall Kirschman *is based in Silicon Valley and provides consulting related to R&D for electronic devices and circuits, as well as assistance in obtaining funding, particularly for extreme temperatures. He also presents professional development courses covering the principles and practical aspects of low-temperature and high-temperature electronics. (www.ExtremeTemperatureElectronics.com). He received his Ph.D. from Caltech in physics and electrical engineering.*
E-mail: ExtElect@gmail.com

Destructive Wire Bond Pull Testing and its Purpose

William Boyce
SMART Microsystems Ltd.

IN THE PREVIOUS ARTICLE, DESTRUCtive wire bond shear testing was discussed. In this article we will discuss the practice and purpose of the destructive wire bond pull test. The reason that we chose to discuss wire bond pull testing after examining shear testing is that, in concurrence with the development process of a wire bond, we perform pull testing only after shear testing has been performed. The destructive pull test is explicitly what it sounds like. A wire bond loop is pulled until it fails in one of three ways: bond lift, heel break, or mid-span break. The pull test measures the force required to break the wire from tensile force, and the remnants of the wire bond are used to determine the failure mode. Typically used to develop the wire bond process, destructive pull testing is also used as a statistical process control in production bonding. The wire bond pull test is not a replacement or substitute for the shear test, but rather a completely different test with a different purpose and intent. Just like the shear test, the pull test has very specific characteristics that it measures. If we assume that shear testing was used to develop a robust weld at the bond foot, a weld that is stronger than the wire itself, then the pull test should never result in a wire bond lift, as this occurrence would be a considered a rejectable condition and cause for immediate action. We don't just focus on the force required for the wire to fail or break, we are also interested in the failure mode. For a robust and well-defined process, that failure mode would be a heel break or a mid-span break. Unlike shear testing, pull testing is covered in MIL-STD-883. This standard, however, covers wire bond pull testing at only a most basic level.

The destructive wire bond pull test is performed by a complex instrument. The tool accessories and settings are selected based on the theoretical breaking pull force range of the wire loop. Once selected and calibrated, the process involves placing a hook under the apex of the bond loop and exerting an upward force on the bond loop until it fails. At SMART Microsystems we employ a Dage 4000Plus to perform this testing. The loop geometry is very important to deciphering the data from the pull test. The tensile force within the bond wire is a function of the pull force and the angle each wire forms with the substrate, see Figure 1. In fact the resultant tensile force is a trigonometric function of the pull force F and the angle formed by each wire. So if we assume that the weld formed at the foot of the wire is stronger than the wire itself, as it should be based on rigorous shear testing and development, then in theory, the resultant pull force F can vary from zero to two times the tensile strength of the wire based on wire geometry alone. Just as the shear test is intended to properly develop a robust weld between the bond wire and the bond pad, the pull test is intended to develop the optimum wire formation and loop geometry.

Dage 4000Plus

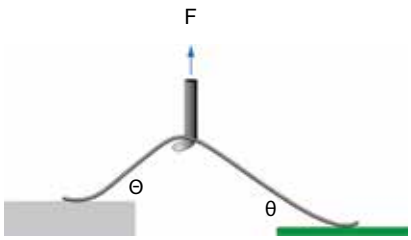

Figure 1.

The destructive wire bond pull test is intended to measure the force required to break the bonded wire using tensile force. It is also possible to perform a non-destructive pull test, but without the results from the wire break, the usefulness of the data collected is drastically decreased. The non-destructive pull test should be used only after a defined and rigorously tested wire bond process has been developed. In destructive pull testing for wire bond development and process control, we record the actual force required to break the bond many times over, but as you may begin to notice it is important to know how that data can be assessed. This developed measurement method specifically relates to the tensile strength of the wire being bonded. We typically explicate our destructive pull data with the use of non-destructive pull force. By placing a small non-destructive pull force on a wire loop to straighten it, we can then measure the geometry, calculate the angles, and with the known tensile strength, calculate the theoretical pull force required for wire breaks.

continued on page 26

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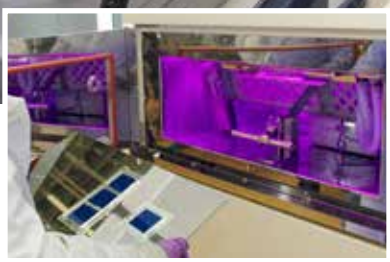

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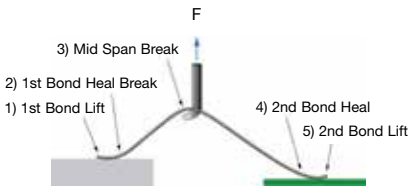
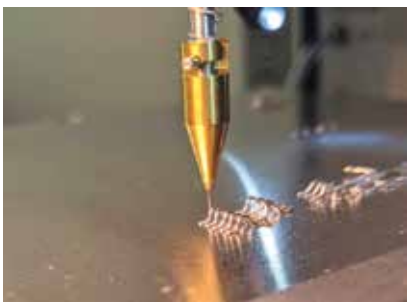


Figure 2.

In addition to actual and theoretical breaking force, we are also interested in the failure mode. Figure 2 indicates how we at SMART Microsystems generally categorize the different failure modes. A wire bond lift is considered a rejectable condition, but with a properly formed wire heel and a roughly 30 degree angle at the wire-substrate interface, we expect the failure mode to be primarily heel breaks with some mid-span breaks. The reason that heel breaks are most common is simply that the heel is the part of the wire that gets deformed the most, and the wire will always break at the weakest point. There are five distinct modes of failure depicted in figure 2. Each one of the failure modes has a group of potential causes associate with them. A bond lift on either bond foot is considered an immediate cause for concern and is a rejectable condition, but nonetheless provides valuable information. A mid-span break near to either the first or second bond is considered to be the most desirable outcome, but can be difficult to achieve with many loop geometries. Heel breaks are the most common failure mode by far, but this could easily indicate an incorrectly formed wire bond foot or improper loop geometry, so although common, this type of failure should never be overlooked.

MIL-STD-883 includes a section on destructive wire bond pull testing that includes the minimum pull strength of different wire diameters. At SMART Microsystems we use MIL-STD-883 as a general guide only. Our upper and lower pull strength limits are developed internally, and are derived from the wire manufacturer's tensile strength for the specific wire being used and the wire geometry. As you'll know from the previous article (MEPTEC Report Summer 2019, Volume 23, Issue 2), we also derive the upper and lower shear limits from the wire tensile strength. Using the wire bond pull test as a process control can be very useful, and each of the failure modes can be a leading process indicator. A pull test breaking strength that is too low or too high can indicate a wide variety of root causes, including change in loop geometry, or even the wrong wire installed in the bonder. A low pull test breaking strength with poor heal formation could indicate a change in settings or a fowled tool, among many other possible root causes. Pull strength should never be considered a single sided limit, it should have defined upper and lower limits.

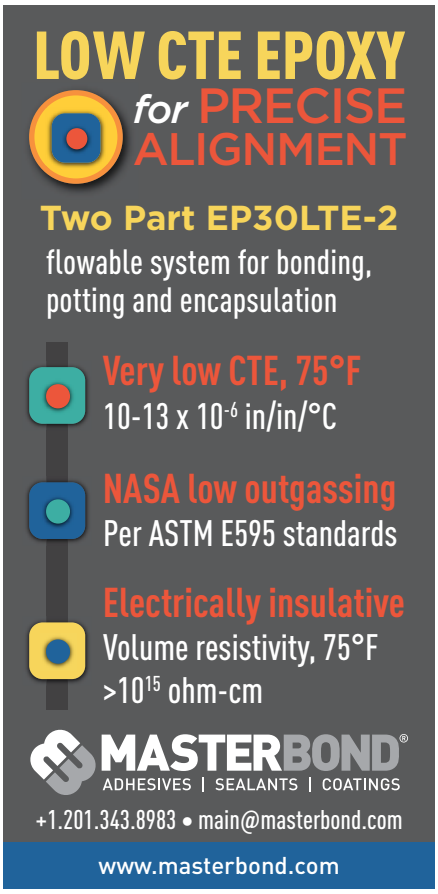


Destructive wire bond pull test in process.

Wire bond destructive pull testing has a valued and indispensable place in the world of wire bonding. It can provide real actionable data to improve, develop, and regulate the wire bond process. Simply stated, pull testing speaks to the quality of the formation of the wire bond loop. The data that it does not speak to is the quality of the weld between the wire and the substrate, which is derived from shear testing. If I could only choose one test for process development it would be the shear test, and if I had only one test to choose for process control it would be the wire bond pull test.

For more information visit our website at www.smartmicrosystems.com. ◆

William Boyce is the Engineering Manager at SMART Microsystems. Mr. Boyce earned a Bachelor of Science in Engineering degree from the University of Rhode Island and has served in the field for over 20 years as a mechanical design engineer, process engineer, team leader, engineering Manager, and Global Engineering Director. In addition to his current role at SMART, he has held positions at General Dynamics, Texas Instruments, Sensata Technologies and TT Electronics. Mr. Boyce has also been a member of the IMAPS New England Chapter for over 10 years as a session chair. He is EIT certified, a Six Sigma Green Belt, and an industry recognized expert in Al wire bonding.



KNOWN GOOD DIE WORKSHOP 2019

Thursday, December 12, 2019

SEMI Global Headquarters, Milpitas, California

With the demise of Moore's Law due to the economics of advanced semiconductor process nodes, the demand for greater cost performance and differentiation has fueled the development of advanced packaging. Having Known Good Die (KGD) is essential for many, if not all, of the current 'crop' of advanced packaging including 2.5/3D die stacking, Fan-out Wafer Level Packaging (FOWLP), System in Package (SiP), Heterogeneous Integration (HI), and Panel Level Processing (PLP). Not to mention bare die used in modules and on flex-circuits such as chip on board (CoB), chip on flex (CoF), and chip on glass (CoG).

It is clear that the various functional areas that necessary to have KGD have made progress since the first KGD conference in Napa in 1994. For example, electronic design automation (EDA) design for test (DFT) tools are generating much higher levels of test coverage that historically was the case.

However, these efforts in isolation may not be sufficient especially since issues may cross more than one functional area. Or worse changes in one area may exacerbate problems in another. What is missing is a forum that will take a higher level and cross-functional view of the challenges of producing KGD.

This event will bring together experts to cover topics such as:

- Metrology and Inspection
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- Business Model
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For questions about event attendance, sponsorships, or exhibiting, please email Susan Kinne **susan@meptec.org**.

FOR MORE INFORMATION AND TO REGISTER ONLINE TODAY GO TO KGDWORKSHOP.ORG

State-of-the-Art Technology Briefs

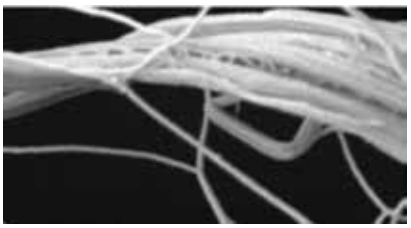
A special feature courtesy of Binghamton University

We are pleased to continue this feature in the MEPTEC Report, brought to us by new Advisory Board member Dr. Gamal Rafai-Ahmed from Xilinx. The State-of-the-Art Technology Briefs contains articles from the Binghamton University S3IP "Flashes." Full text is available upon request through the IEEC Site at: http://www.binghamton.edu/s3ip/index.html.

Computer memory can become faster and cheaper thanks to research into bismuth ferrite (BFO) by University of Arkansas researchers. This material has the potential to store information much more efficiently than currently possible. BFO could also be used in sensors, transducers and other electronics. In current memory technology, information on a computer is encoded by magnetic fields, a process that requires a lot of energy, more than 99% of which is wasted in the form of excess heat. The researchers documented the phenomenon responsible for the enhanced response, which they called an "electro-acoustic magnon." The name reflects the fact that the discovery is a mix of three known "quasiparticles," which are similar to oscillations in a solid: acoustic phonons, optical phonons and magnons. *(IEEC file #11170, Science Daily, 5/2/19)*

Drexel University researchers have created ink for an inkjet printer made from a highly conductive type of two-dimensional material called MXene. The ink can be used to print flexible energy storage components, such as supercapacitors, in any size or shape. Conductive inks have been around for nearly a decade and they represent a multi-hundred million-dollar market that is expected to grow rapidly into the next decade. It's already being used to make the RFID tags used in highway toll transponders, circuit boards in portable electronics and its lines car windows as embedded radio antennas and defrosting. *(IEEC file #11149, Science Daily, 4/17/19)*

Paul Scherrer Institute researchers have produced a new type of composite material with shape memory that is activated by magnetic fields. While previous shape-memory materials can assume a temporary shape and recover their original shape on increasing the temperature, this new material consists of a polymer with droplets of embedded magnetorheological fluid, and retains a given shape when positioned in a magnetic field without the need for heat. This unique characteristic makes it suitable for applications in biomedicine, aerospace, as well as wearable electronics and robotics. *(IEEC file #11242, Materials Today, 7/1/19)*



MIT engineers have fabricated polythene films that conduct heat at 62W/mK, which is as good as steel, better than alumina, and much better than normal polythene which is an insulator. These properties of polymers can create new applications and new industries and may replace metals as heat exchangers. The film consists of nanofibers running along the film with crystalline and amorphous regions. In the film, thermal conductivity is anisotropic – mostly along the fibers and not through the film. *(IEEC file #11157, Electronics Weekly, 5/2/19)*

University of Washington researchers have created a multiwavelength vat-polymerization process that takes advantage of the wavelength-specific cure properties of certain chemicals. This development moves additive-manufacturing (AM) towards the creation of multi-material components in one process step, By projecting two or more wavelengths of light (using spatial digital light projection methods) into a vat filled with a mixture of resins, acrylates, epoxies, polymers, or other organic and inorganic liquid chemicals that cure with different wavelengths (in the visible, ultraviolet, or infrared), a 3D rendering of a multi-material object can be produced in one process step. *(IEEC file #11201, Laser Focus World, 6/4/19)*

Columbia University researchers have developed an ion-gated transistor with relatively high transconductance and speed that can be used in analog or digital circuits such as EEG front-end "integrated" circuits. The researchers devised and tested what they maintain is the first biocompatible, ion-driven transistor that's fast enough to enable real-time signal sensing and stimulation of brain signals. Their ion-gated transistor (IGT) uses mobile ions within a conducting polymer channel to allow both volumetric capacitance via ionic interactions through the bulk of the channel, as well as shortened ionic-transit time. The transistor can be used either as a single device or "microfabricated" to create the equivalent of integrated circuits. *(IEEC file #11202, Medical Design, 6/3/19)*

MARKET TRENDS

Hyperion Research forecasts that the worldwide market for high-performance computing (HPC) server systems will reach $19.6 billion in 2022 growing at a 9.8% CAGR to. Accompanying this growth is a strong trend toward the use of liquid cooling to manage the fast-rising heat levels generated by increasingly large and more densely packed HPC servers. HPC data centers have often had to rely on liquid cooling systems borrowed from other industries, and this mismatch may have exacerbated "data center hydrophobia." Fortunately, current growth in spending for HPC liquid cooling systems has begun to attract purpose-built solutions designed to handle the extreme cooling demands of HPC systems more effectively. *(IEEC file #1116?, Electronic Cooling, 4/23/19)*

POSTECH researchers have developed a flexible and wearable vibration responsive sensor. It can recognize voice through vibration of the neck skin and is not affected by ambient noise or the volume of sound. The vibration sensor utilizes the acceleration of skin vibration and that voice pressure is proportional to the acceleration of neck skin vibration at various sound pressure levels from 40 to 70 Decibel Sound Pressure Level. The device which consists of an ultrathin polymer film and a diaphragm with tiny holes. This research can be further extended to various voice-recognition applications such as an electronic skin, human-machine interface, wearable vocal healthcare monitoring device. *(IEEC file #11245, Science Daily, 6/24/19)*

The R&D investment around stretchable electronics, including the integration of electronics into clothing via conductive inks, exploration of new substrate options and materials to enable improved strain tolerance, and reviews of design approaches to enable stretchable electronics to be more easily integrated in a reliable and reproducible way. Many players develop new material options, particularly around conductive inks and substrates, in order to address these needs. This also links onto many different component types that can be developed from these core materials, all enabling a full toolkit of stretchable electronic parts which designers can begin to integrate into products. The rise in interest and discussion of stretchable electronics has been closely linked to a parallel rise in interest around "wearables" or "wearable electronics". *(IEEC file #11252, Printed Electronics World, 7/2/19)*

RECENT PATENTS

System and method to enhance solder joint reliability (Assignee: Western Digital Technologies) - *Patent No.- 15/715863* – A reliability cover that is disposed over at least one of an integrated circuit package and a Si die of the integrated circuit package is disclosed. The integrated circuit package is mountable to a printed circuit board via a plurality of solder balls. The reliability cover is configured to reduce a difference in a coefficient of thermal expansion between the integrated circuit package and the printed circuit board, and between the Si die and a substrate of the integrated circuit package by a threshold value.

Transverse circuit board to route electrical traces - (Assignee: Google LLC) *Patent No.- 10,257,933* – An electronic device including a transverse circuit board to route electrical traces is provided. In some embodiments, the electronic device includes: a housing; a first printed circuit board (PCB) that is fixed relative to the device housing; an integrated circuit that is connected to the first PCB; a second PCB that is situated in a transverse position relative to the first PCB, a plurality of electrical traces; and a securing component that secures the second PCB in the transverse position relative to the first PCB.

Stackable optoelectronics chip-to-chip interconnects - (Assignee: Banpil Photonics) *Pub. No.- US10254476* – An optoelectronics chip-to-chip interconnects system, including at least one packaged chip to be connected on the printed-circuit-board with at least one other packaged chip, optical-electrical (O-E) conversion mean, waveguide-board, and (PCB). Single to multiple chips interconnects can be interconnected provided using the technique disclosed in this invention. The packaged chip includes semiconductor die and its package based on the ball-grid array or chip-scale-package. The waveguide board includes the conductor transferring the signal from O-E board to PCB and the flex optical waveguide stackable onto the PCB to guide optical signal from chip-to- chip.

Film type semiconductor package - (Assignee: Samsung Electronics) *Patent No.- 10,256,174* – A film type semiconductor package includes a film substrate; a metal pattern extending a first length in a first direction on the film substrate, having a first width in a second direction perpendicular to the first direction the first length being larger than the first width, and includes a plurality of through holes spaced apart from each other in the first direction; a semiconductor chip including a plurality of pads; and a plurality of bumps spaced apart from each other in the first direction, bonded with the metal pattern, and overlapping the plurality of through holes and connected to the pads.

BINGHAMTON UNIVERSITY

BINGHAMTON UNIVERSITY *currently has research thrusts in healthcare / medical electronics; 2.5D/3D packaging; power electronics; cybersecure hw/sw systems; photonics; MEMS; and next generation networks, computers and communications. The S3IP Center of Excellence is an umbrella organization comprising five constituent research centers. More information is available at* ***www.binghamton.edu/s3ip.***

Integrated Electronics Engineering Center (IEEC) - The IEEC is a New York Center of Advanced Technology (CAT) responsible for the advancement of electronics packaging. Its mission is to provide research into electronics packaging to enhance our partner's products, improve reliability and understand why parts fail. More information is available at ***www.binghamton.edu/ieec.***

Center for Autonomous Solar Power NorthEast Center for Chemical Energy Storage (NECCES) - NECCES is working on the limitations to batteries reaching their ultimate potential. Recently they have placed emphasis on a new cathode and a new anode. The LixV0P04 cathode can attain over 300 Ah/kg compared with around 160 Ah/kg for the commercial LiFeP04 cathode. The SnyFe/C composite anode has a more than 50% higher capacity than today's graphite-based anodes. More information is available at ***www.binghamton.edu/necces.***

Analytical and Diagnostic Laboratory (ADL) - The ADL provides an array of analytical and diagnostic tools located in a single facility to address the needs of faculty and industry in understanding materials, structures and failures that are found in electronics packaging. The ADL supports the 5 research centers previously mentioned. The facilities of the ADL are available to our industry partners. More information is available at ***www.binghamton.edu/adl.*** ◆

IC Packaging World Converges Again in Las Vegas for ECTC 2019

Sam Karikalan
Broadcom, Inc.

THE MEMORIAL DAY WEEK BECAME action packed again for all things packaging, as the key stake-holders of the global microelectronics packaging industry gravitated to Las Vegas, NV for the 69th IEEE 2019 Electronic Components and Technology Conference (ECTC). The 69th ECTC was held in The Cosmopolitan of Las Vegas during May 26-29, 2019, full of technical sessions and social events on all days from early morning through late evenings.

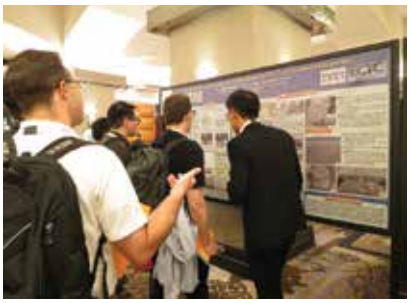
Attendance Among the Highest

With 1563 attendees always crisscrossing its hall-ways, session rooms and the exhibit hall, this year's ECTC lived up to its reputation of being the premium global annual event of the packaging industry. This year's attendance is the second largest in ECTC's 70 year history. 358 papers were presented in 36 oral sessions and 5 interactive presentation sessions, on key topics such as Packaging Technologies, Materials & Processing, Interconnections, Assembly & Manufacturing, Applied Reliability, Thermal/ Mechanical Modeling & Characterization, High-Speed & Wireless Components, Emerging Technologies and Photonics.

The top 10 well-attended oral sessions of ECTC 2019 had each 100+ attendees in them. As seen in the past few years, the session on "Wafer Level Fan-Out Process Integration" looked like a mini conference of its own with over 350 attendees! Besides the Fan-Out packaging technology, other popular topics were 3D & Heterogeneous Integration, Flip Chip Packaging and Packaging for High Bandwidth, 5G & mmWave.

Record Attendance for PDCs

The 69th ECTC received 516 registrations for its 18 Professional Development Courses (PDC) held on Tuesday, with



Enormous interest in papers presented in the Interactive Presentation Sessions.

Luncheon Keynote Speaker, Prof. John Rogers ***(left)*** **with the ECTC General Chair, Prof. Mark Poliks.**

7 of them being offered brand new this year. This is the highest ever attendance at ECTC's PDCs, which is a 7% increase over that in San Diego in 2018 and 34% increase over that in Las Vegas three years ago. There were also five special / plenary / seminar sessions with invited speakers presenting on emerging topics such as Transient Electronics, Photonics, Sensors and Packaging for Autonomous Driving, and Packaging for Next Generation Smartphone Performance.

For the first time ever in ECTC, a special session on Tuesday evening featured presentations from the winners of a competition on "Future (Visions) of Electronic Packaging" organized by the IEEE Electronics Packaging Society. Speakers from Georgia Tech and TU Dresden kept the audience very excited with their vision on technologies such as "Brain on a Chip". Tuesday at the conference also saw an all-day Workshop on "Heterogeneous Integration Roadmap", organized by the IEEE Electronics Packaging Society and its collaborating organizations such as SEMI, IEEE Electron Devices Society, IEEE Photonics Society and the ASME EPPD Division. The 2019 edition of this roadmap can be found online at https://eps.ieee.org/technology/heterogeneous-integration-roadmap/2019-edition.html.

Bio-Packaging Helping Humanity

Prof. John A. Rogers of Northwestern University delivered the keynote address at the Wednesday ECTC Luncheon. He spoke on "Soft Electronic and Microfluidic Systems for the Skin" and highlighted how his team's work in that area is making a huge difference in the quality of life for infants in the neo-natal care units of hospitals in the Chicago area and their parents, with all the bulky and scary wired sensors on the baby's bodies being replaced by soft, flexible and thin wireless sensor modules for continuously monitoring the vitals.

The highlights of the 69th ECTC, including the presentation material from invited speakers, can be found online at http://ectc.net/about/69highlights.cfm.

While ECTC Executive Committee sincerely thanks all the attendees, authors, sponsors and exhibitors for their profound contributions to the success of the 69th ECTC, it also invites all authors to submit their abstracts for the 70th ECTC that will be held in Lake Buena Vista, FL next year in May. The deadline for submission of abstracts is Oct. 6, 2019. The Call for Papers can be found online at http://ectc.net/authors/files/70-ECTC-First-Call.pdf and the abstracts can be submitted at http://ectc.net/abstracts/index.cfm. ◆

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Grip Ring Shippers


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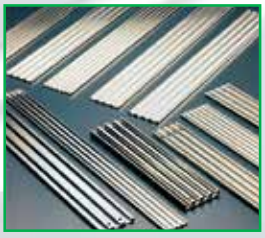
Boat Magazines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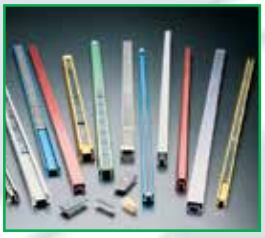
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