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Changing Market Requirements
Bring
New Challenges and Opportunities

Herb Reiter

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MEPTEC* Luncheon, February 13, 2019

*: **M**icro**E**lectronics **P**ackaging and **T**est **E**ngineering **C**ouncil

AGENDA

Introduction

Key Market Data and Requirements

Multi-die ICs and Advanced Packaging

EDA Tools, Flows and Libraries

Summary

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Herb Reiter's Alliance Management Work

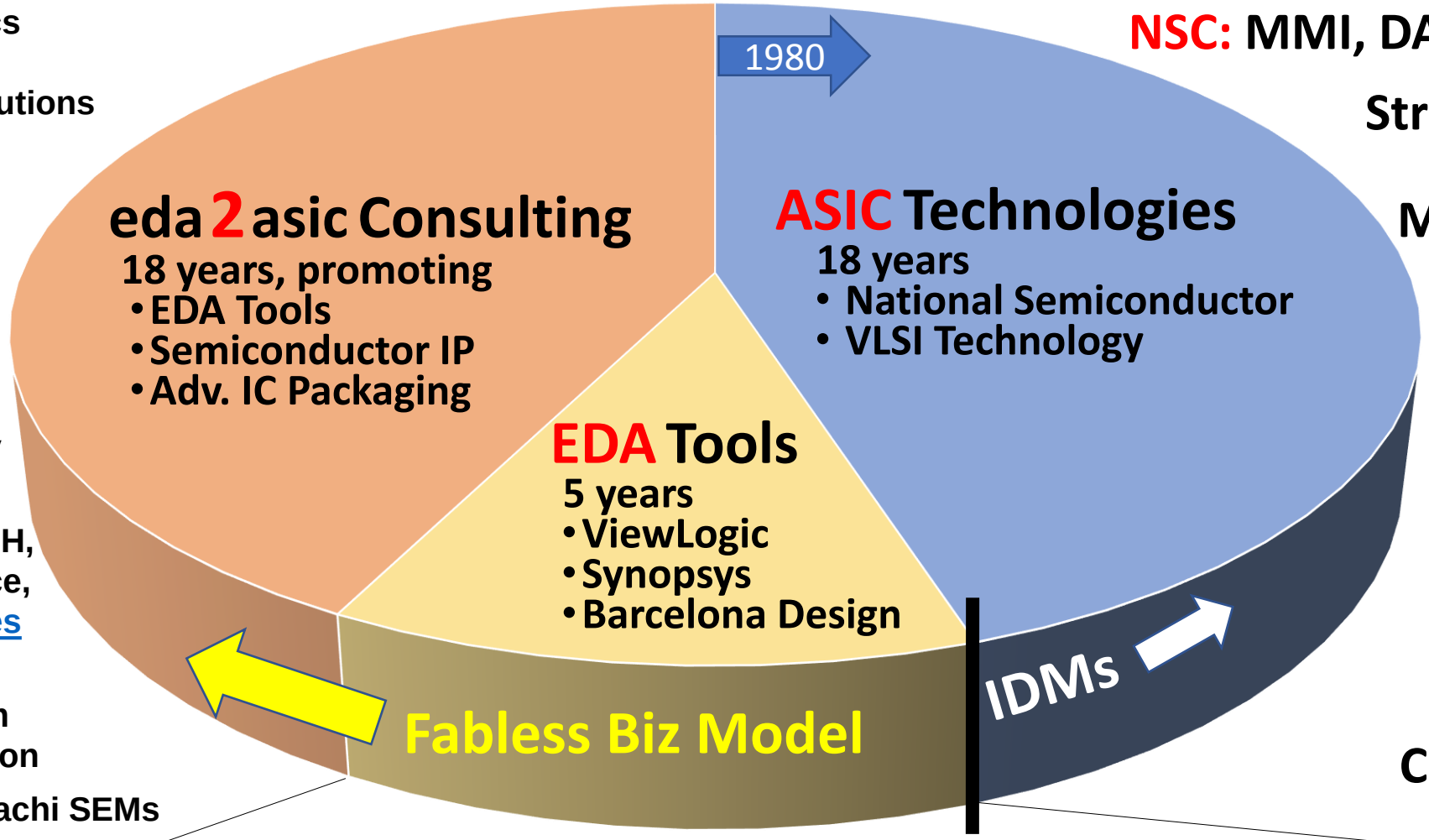
EDA: Synplicity
Mentor Graphics
Berkeley DA
Handshake Solutions
CiraNova
ReShape
Flomerics
Gradient DA
Takumi
Mephisto DA

IP: S3 Group
GDA Techology

Adv. Packaging
GSA, SEMATECH, Si², ESD Alliance, Xperi, 3D InCites

SOI: Soitec
SOI Consortium
Innovative Silicon

Equipment: Hitachi SEMs



NSC: MMI, DATA I/O, Prolog, Structured Design

Motorola, Daisy, Mentor, Valid

VLSI: Philips, ARM, ES2, EM, ZMD Dresden, IBM Endicott, Canal+ in France

TSMC, UMC, Chartered // IBM, TI, LSI, Lucent, Fujitsu, NEC, Toshiba, Mitsubishi

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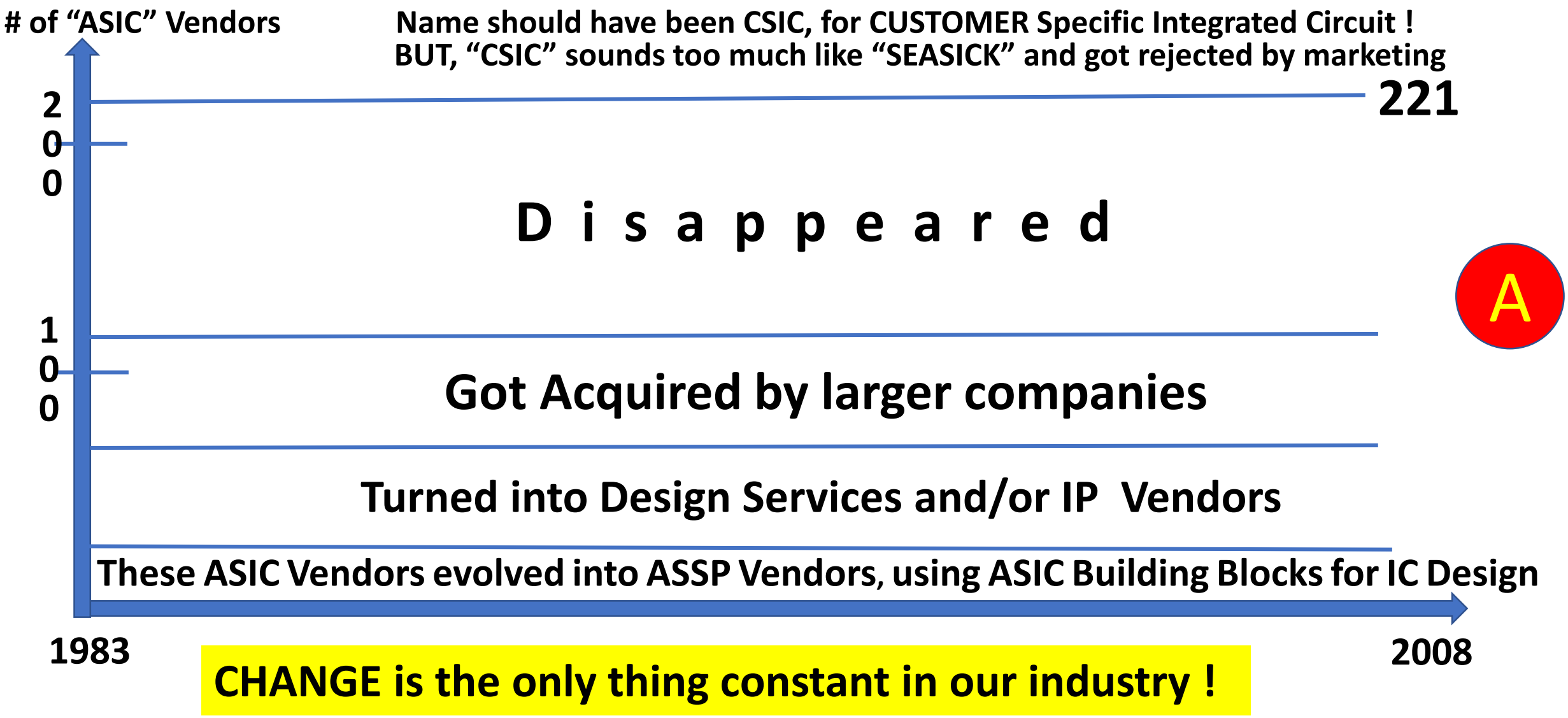
Herb's 25 Years in the ASIC Business



CHANGE is the only thing constant in our industry !

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Key Market Trends

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ECOSYSTEM for Electronic Products & Semiconductors

Major Market Segments demanding Electronic System Solutions
Communication/5G, Computing, Industrial, Consumer/VR/AR, IoT, Automotive, Mil/Aero, …

Electronic System Vendors
Samsung, Apple, Dell, Lenovo, Huawei, BBK, HP, LG, WD

Semiconductor Vendors
Samsung, Intel, SK Hynix, Micron, Qualcomm, Broadcom, TI, Toshiba, WD, NXP

Wafer Fabs
TSMC, GF, UMC, Samsung, SMIC,..

OSATs
ASE, Amkor, JCET, …

Semiconductor IP & EDA
ARM, SNPS, CDNS, Mentor,…

IC Design Services
eSilicon, Open Silicon,…

Materials and Equipment for Manufacturing, Metrology and Test
DowDupont, 3M, BASF, Henkel,… // AMAT, TEL, LAM, EVG,…// KLA, Nanometrics,…// Advantest,…

Streamlining of ECOSYSTEM-wide cooperation is needed to create attractively-priced electronic products AND decent profit margins!!!

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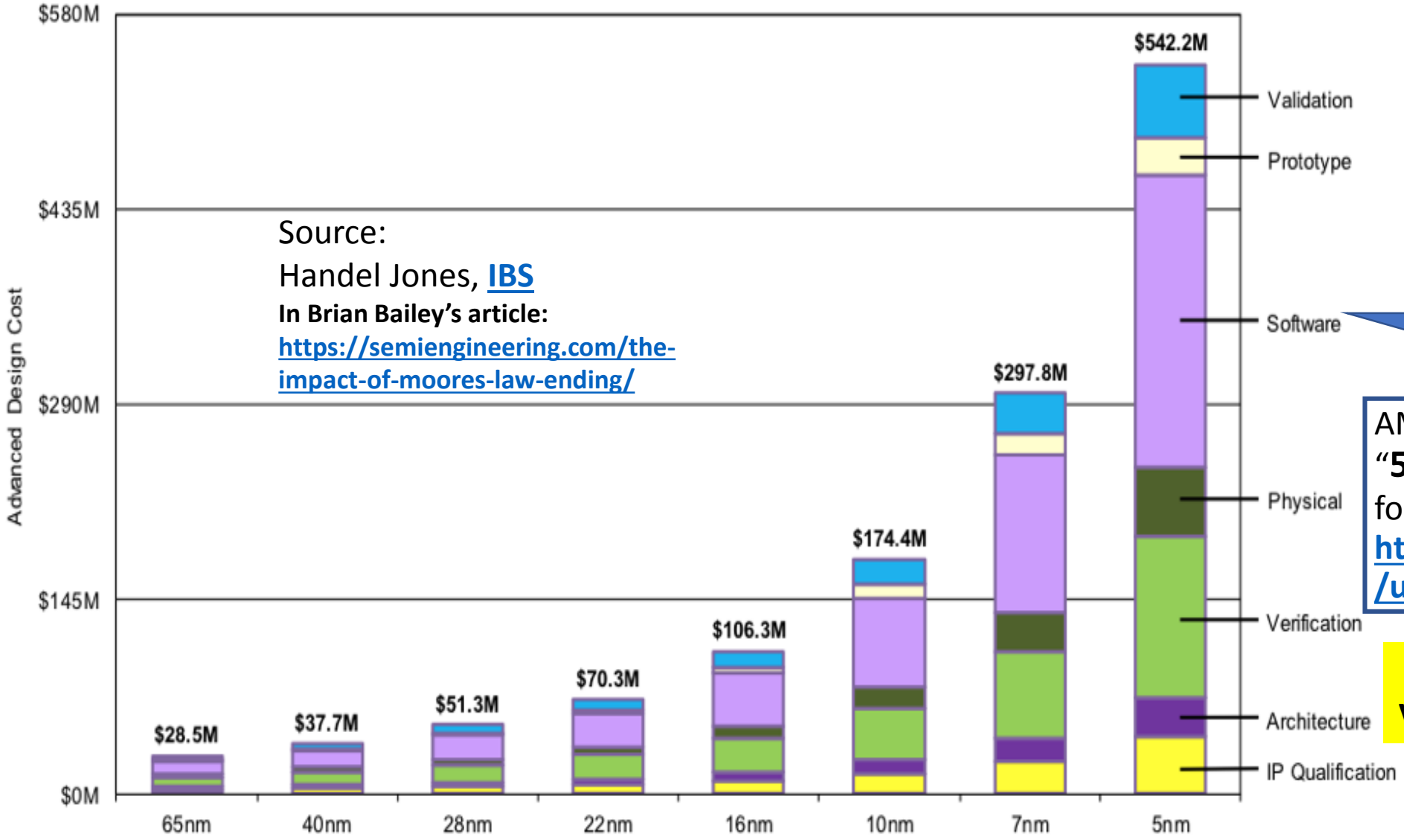
Following Moore's Law Costs Time and Money



Source:
Handel Jones, IBS
In Brian Bailey's article:
https://semiengineering.com/the-impact-of-moores-law-ending/

Design Cost

Years to develop, Next Node's Gain

AMAT's Natarajan, 2/5/'19:
"**5 years** to the next node, for ~ **20%** performance **gain**."
https://semiengineering.com/unsticking-moores-law/

Only economical for VERY high volume designs!

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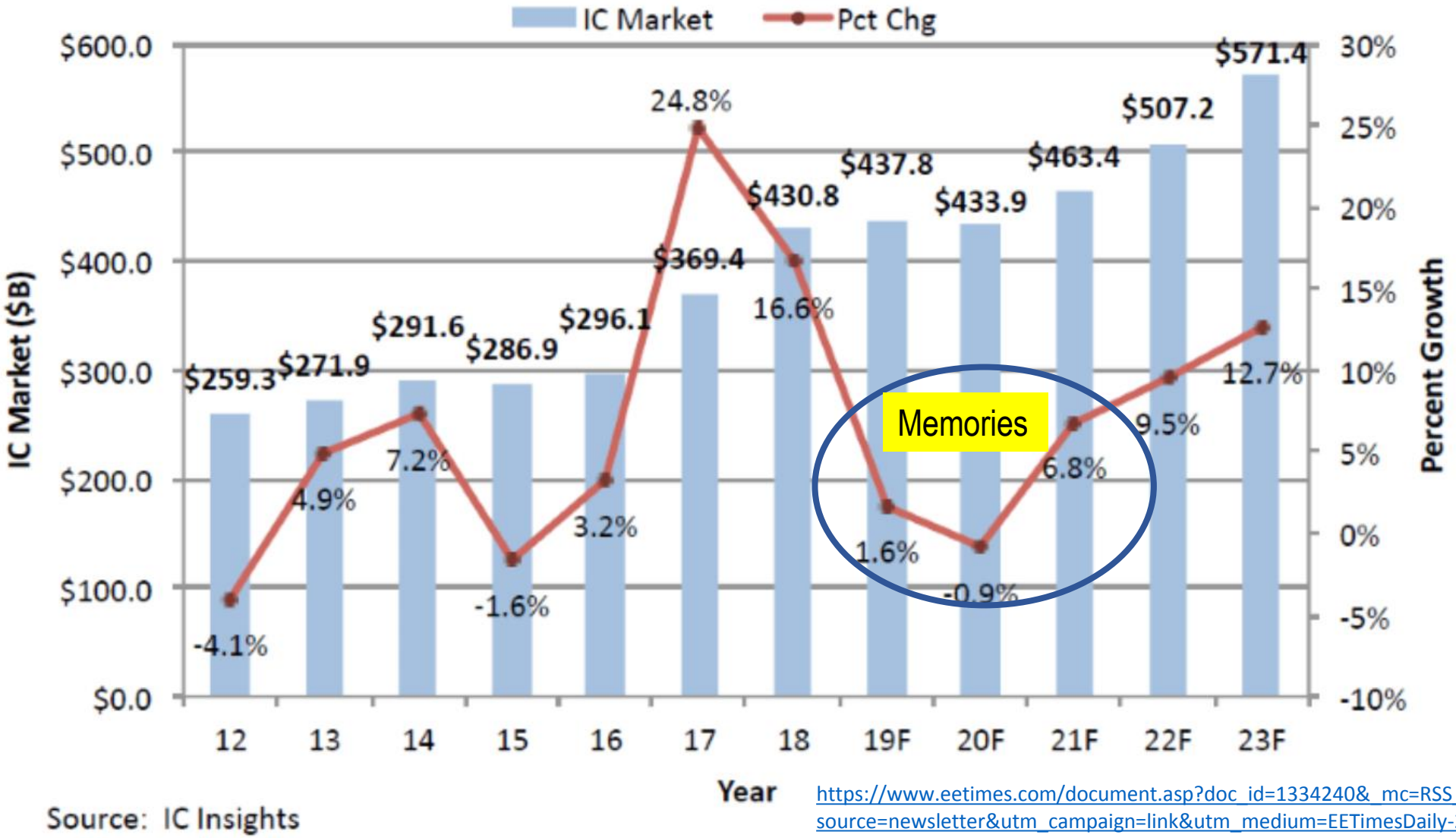
IC Market Growth Rates



Source: IC Insights

https://www.eetimes.com/document.asp?doc_id=1334240&_mc=RSS_EET_EDT&utm_source=newsletter&utm_campaign=link&utm_medium=EETimesDaily-20190125

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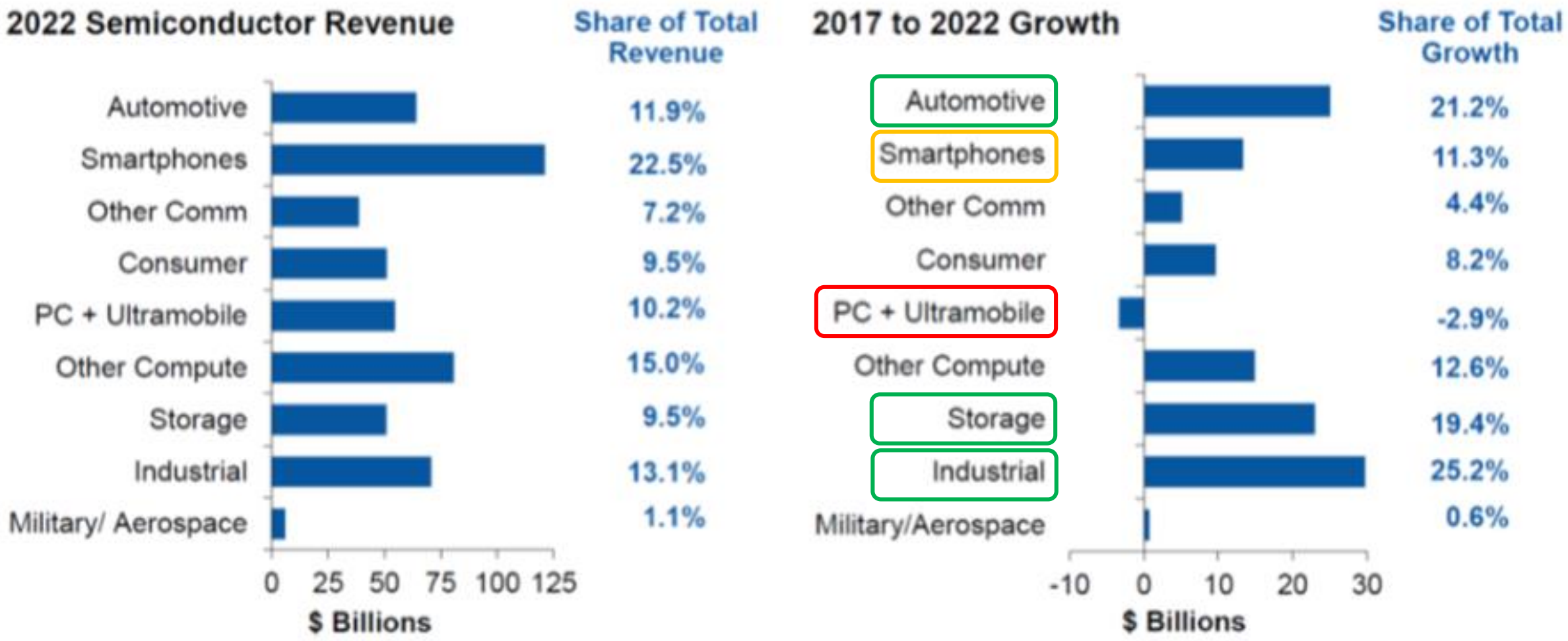
Gartner's Revenue Growth Forecast Through 2022



Growth shifting toward commercial applications!

(Presented by Bob Johnson at ISS2019, updated Q4, 2018)

Gartner

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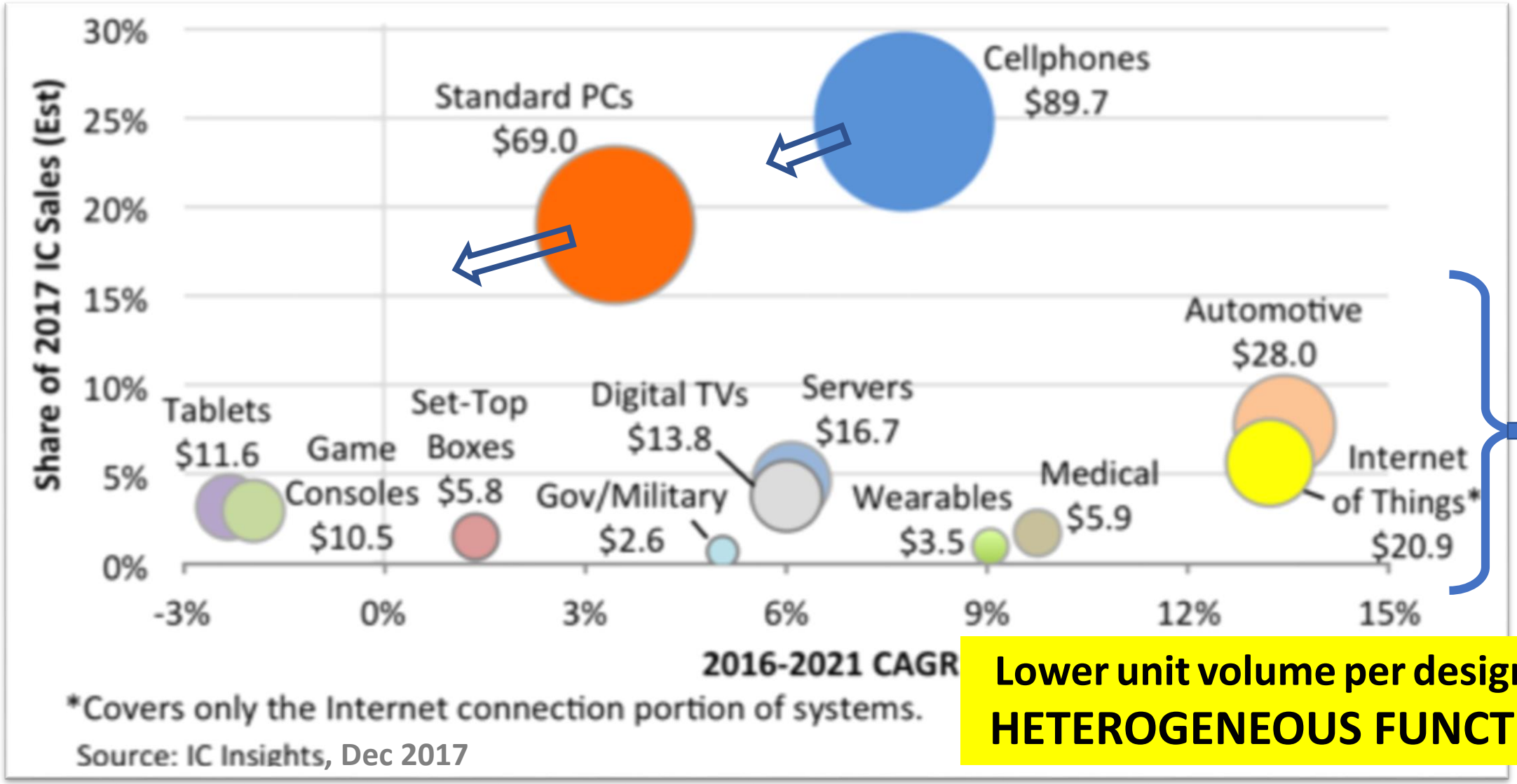
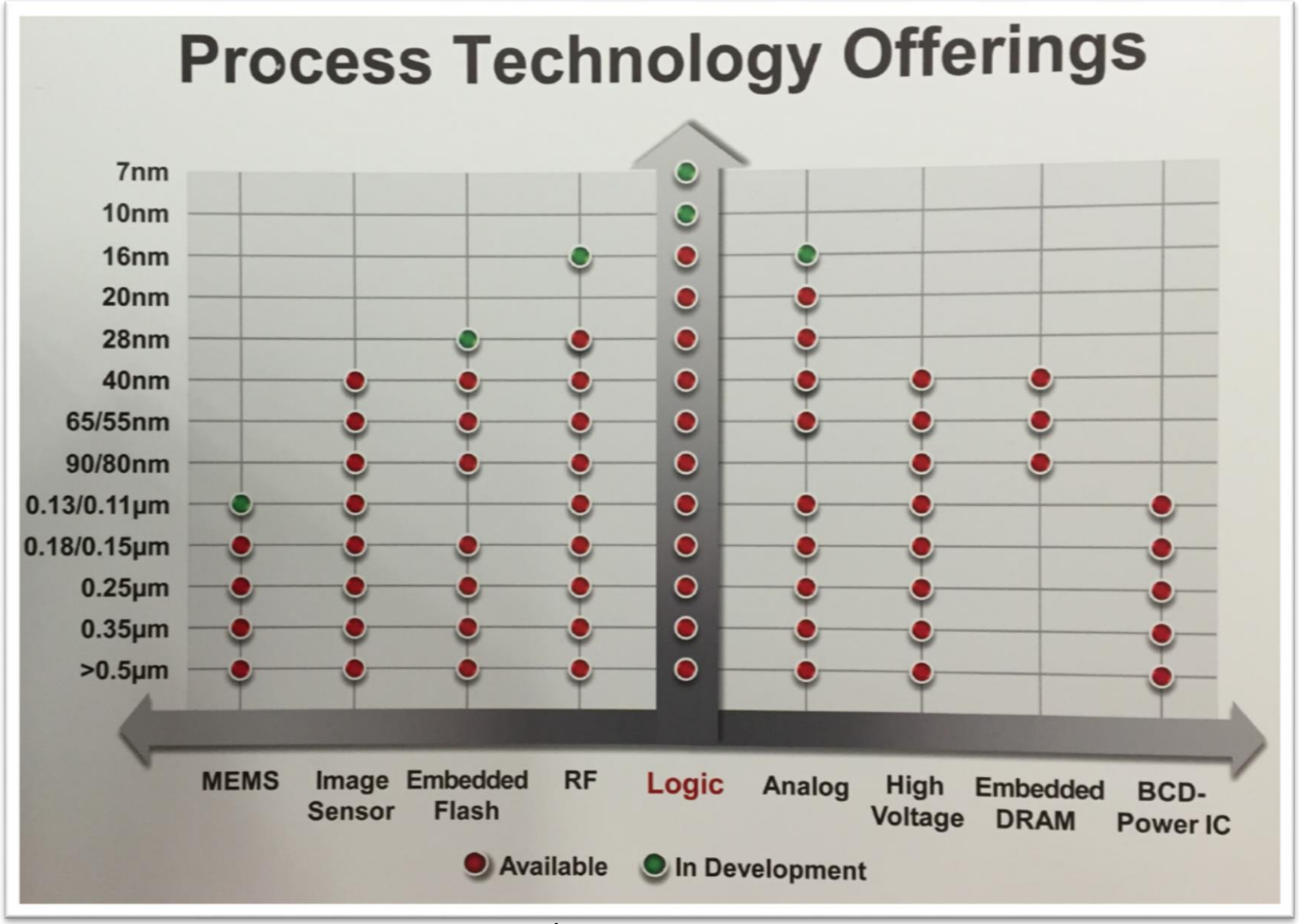
IC End-Use Markets ($B) and Growth Rates



Lower unit volume per design and HETEROGENEOUS FUNCTIONS

http://www.icinsights.com/news/bulletins/Automotive-And-IoT-Will-Drive-IC-Growth-Through-2021/

Availability of Heterogeneous Functions



Source: TSMC Booth at DAC 53 in Austin, June 2016

B

SoC Process extensions for HETEROGENEOUS integration are always 2, 3 or more nodes behind Digital Logic !

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--- China ---

Source: The Economist, Dec 1, 2018
This headline article is at:
https://www.economist.com/leaders/2018/12/01/chip-wars-china-america-and-silicon-supremacy

This article looks at history, outlines our current challenges with China and suggests:

- **Work with allies to push back on unfair practices**
- **Foster domestic innovation**
- **Prepare for a world with pervasive and powerful Chinese chips**

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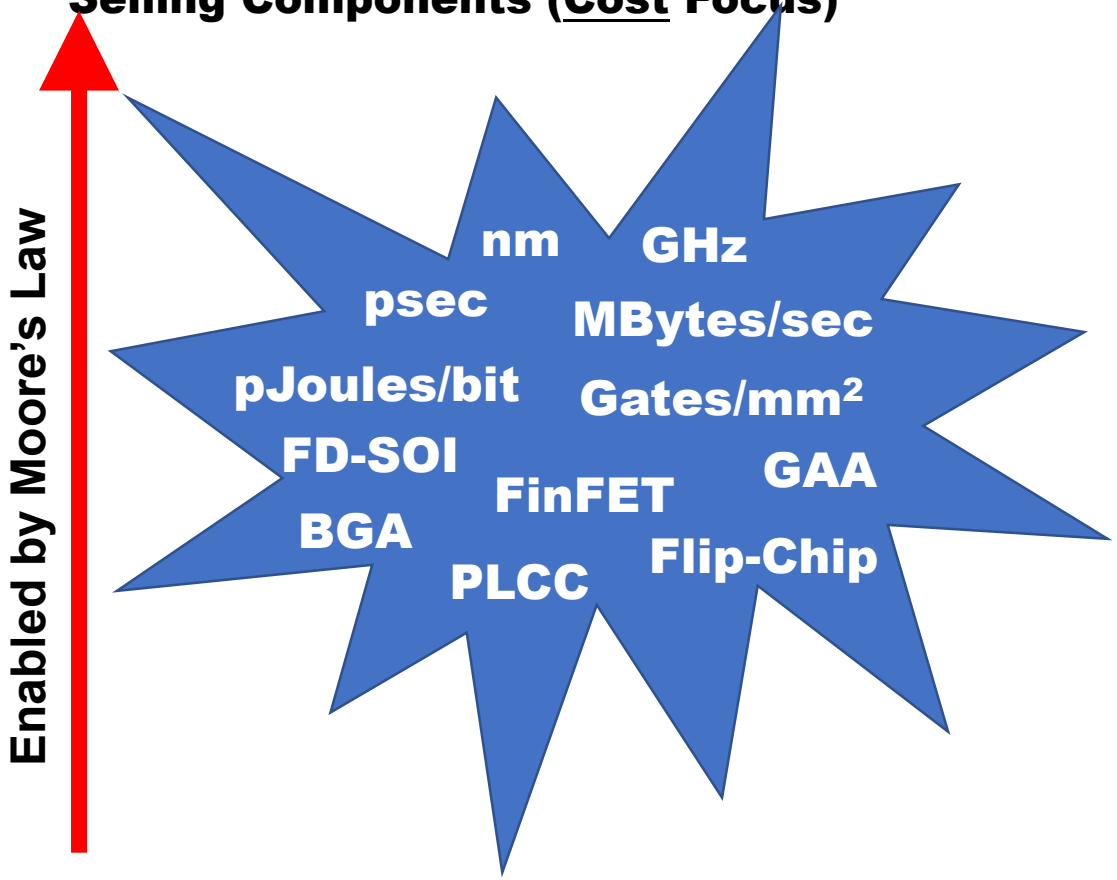
Customers Demand System-level Solutions

OLD: Technology Driven

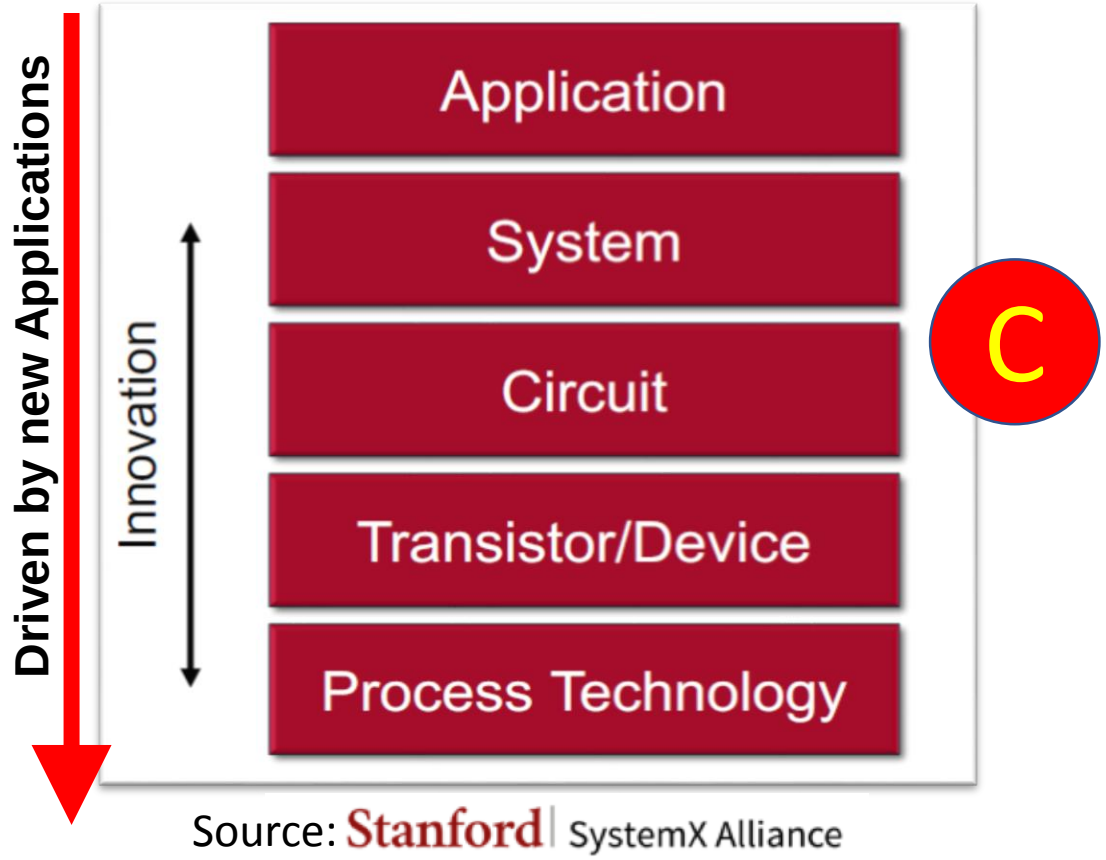
Selling Components (Cost Focus)



IC -> Pkg -> Board -> Rack -> SYSTEM

NEW: Applications Driven

Selling valuable SYSTEM Building Blocks



Source: Stanford | SystemX Alliance

Application-specific requirements drive supply chain

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Market Requirements are Changing Significantly

CRITERIA	Traditional, technology driven	New, applications driven
Revenue Drivers	Few: PCs, Laptops, Smartphones	Many, Diverse: IoT, 5G, AI, Auto, FHE,…
Updating Flexibility	Only Software Updates practical	System Upgrades ➔ H/W Updates Too
Typical Life-time Volume	**100,000s to Many Millions**	**100s to 100,000s, Rarely More**
Functionality	Primarily Logic and RAM	**Logic, RAM, NVM, RF, MEMS, Sensors**
Formfactor / Power Diss.	Small / Low	Smaller / Very Low, Energy Harvesting
NRE / Time / Manpower	**~500,000,000 / 1-3 Yrs / 200+ Eng.**	**< Million / Months / 5-10 people**
Unit Cost Sensitivity	VERY HIGH, **Cost**-driven	MUCH LOWER, **Value**-driven
Standards Support	Established Worldwide	Emerging, Regional, Appl. Specific
Ecosystem/User Experience	Mature / Well Trained Users	Emerging / **Education Needed**

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100 Million “Computers on Wheels” by ~2030 …

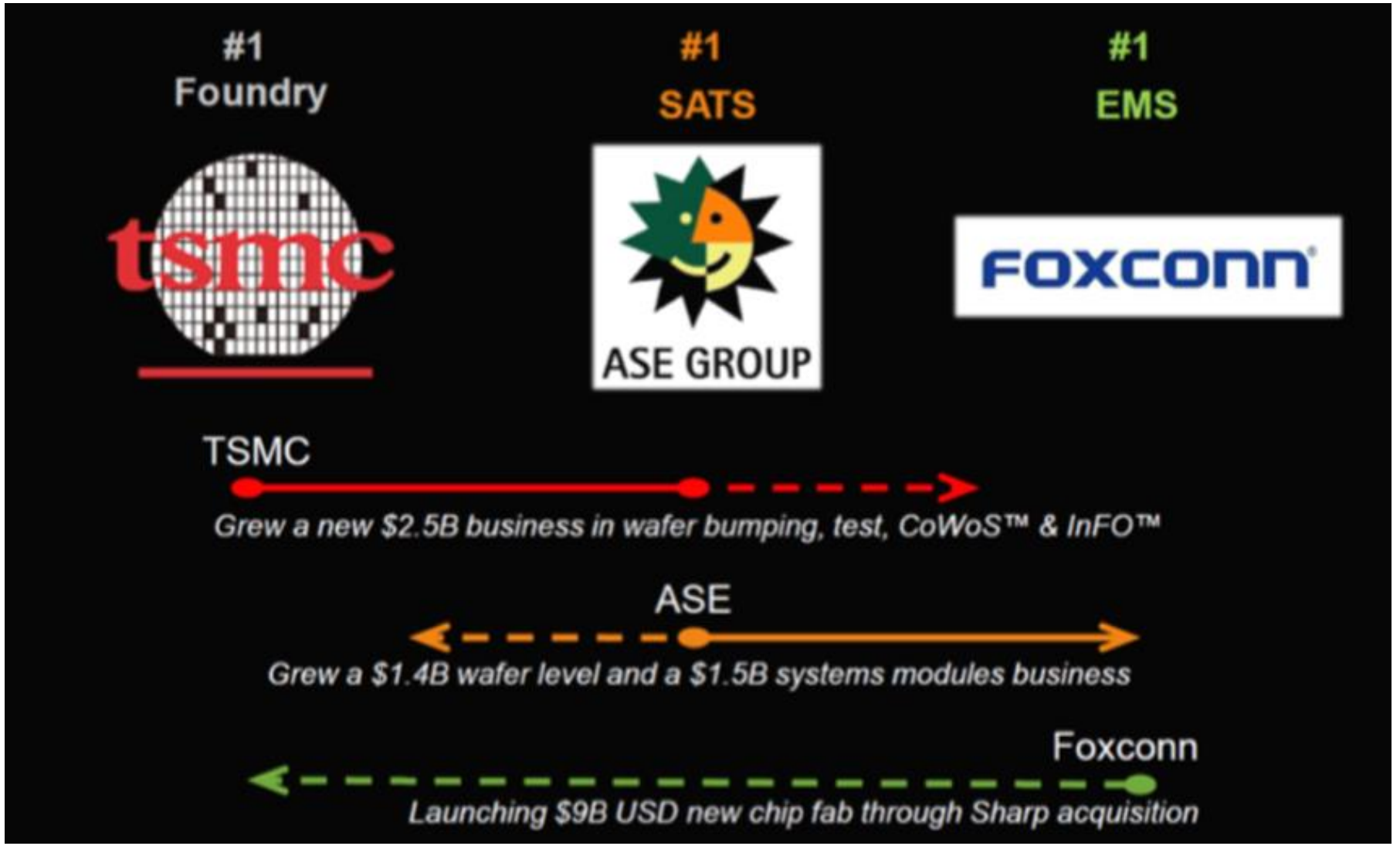
Opportunities for :

- **Logic**
- **Memory**
- **Misc sensors**
- **Actuators**
- **ADCs / DACs**
- **Displays & drivers**
- **Several radios**
- **LEDs & drivers**
- **Power electronics**
- **OFF-THE SHELF AND CUSTOM IC PACKAGES**

https://www.machinedesign.com/motion-control/could-5g-be-missing-puzzle-piece-self-driving-cars?NL=MACD-001&Issue=MACD-001_20190206_MACD-001_515&sfvc4enews=42&cl=article_1_b&utm_rid=CPG05000000219930&utm_campaign=23153&utm_medium=email&elq2=37acfbd8bf8a410d971c464e65b3b678

Digital Functions **Heterogeneous Functions** **PACKAGING ALTERNATIVES**

Examples for “Re-Integration” Towards IDMs



Traditional silos re-integrate. Examples from industry. (Presented by Tim Olson, DECA Technologies) at ISS2019

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The 3D-IC Dream ~10 Years Ago

Lower System COST

Smaller FORM-FACTOR

Higher PERFORMANCE per WATT

BUT:

PI & HEAT MANAGEMENT

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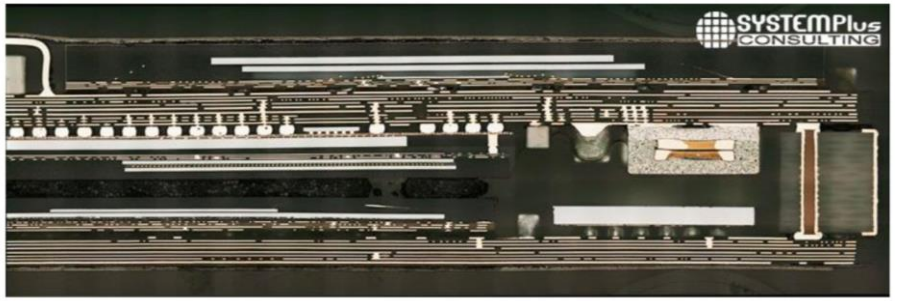
System-level Solutions in a Package

SOURCE: Electronic Design Article, Part 1, Sept 2018 "Path to Systems: Opportunities and Challenges for Next-Gen Semiconductor Integration"

https://www.electronicdesign.com/embedded-revolution/path-systems-opportunities-and-challenges-next-gen-semiconductor-integration



Second generation of TSMC's Integrated Fan Out (InFO) Packaging for the Apple A11 processor for the iPhone X

SOURCE: YOLE Newsletter, February 2018

HIGH DENSITY AND HIGH BANDWIDTH CHIP-TO-CHIP CONNECTIONS WITH 20µm PITCH FLIP-CHIP ON FAN-OUT WAFER LEVEL PACKAGE

IMEC Paper at IWLPC 2018

Value creation moves from single-die ICs to multi-die advanced packages !!! WHY?
Heterogeneous Functions, NRE, Unit Cost, Performance/Watt, Form-factor, Reliability,…

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Technology Benefits, Challenges and Concerns

2D-SoCs

- "That's how we always designed ICs", **BUT**
  - *NRE's are exploding*
  - *Time to Market => Years*
  - *Mixing heterogeneous functions extremely costly*
  - *Bug fixes very expensive*
  - *Reliability @ ≤7nm*
  - *IP availability & cost*
  - *Sole source Si supply*
  - *Customization difficult*
  - *Design reuse difficult*

2.5D-ICs

- Lower total power
- Enables modularity
- Mostly: Logic & HBM, **BUT**
  - *Si Interposer: $$, ≤20 cm²*
  - *Thin die warpage, stress*
  - *Organic I/Po ➔ larger L/S*
  - *Glass I/Po still not mature*
  - *TSVs processing & area: $$*
  - *Thermal management*
  - *Interaction between dies*
  - *Power and Signal Integrity*

3D-ICs

- Lowest total power
- Unlimited B/W, **BUT**:
  - *Primary use memories*
  - ***Thermal management***
  - *Interaction between dies*
  - *W-2-W ➔ same die size*
  - *Testability, redundancy*
  - *Yield management*
  - *Vertical bus standards*
  - *NO planning, design & verification tools yet*
  - *Monolithic 3D for logic ?*

Also: Design and Manufacturing of Wafer and Panel-level single and multi-die packaging is rapidly maturing!
Announced WLP/PLP platforms: TSMC's InFO // Samsung's ePLP // Nepes' RCP // Shinko's MCeP

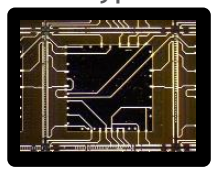
Two Decades of Direct Bonding Proliferation

ZiBond® Direct Bonding
Direct Bond w/o Interconnect

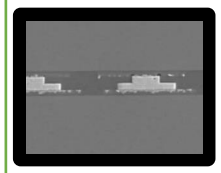
DBI® Hybrid Bonding
Direct Bond w/ Interconnect

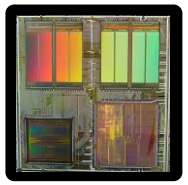
'00
Ziptronix founded:
Spun-off from RTI to commercialize bonding technology

'03
3D IC ZiBond
FPGA-memory
Prototype



'07
Ni DBI Hybridized
Image Sensor
8 Micron Pitch

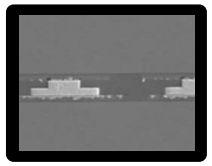




3D SoC ZiBond
Handheld Router Prototype

'09
Raytheon
Licensed DBI
Oct 2009

Cu DBI
2 Micron Pitch



Cu DBI Prototype
10 Micron Pitch

'10

'11
SONY
Licensed ZiBond
Sept 2011

'12
Tezzaron
Licensed ZiBond/DBI
Nov 2012

QUALCOMM
IO Semi→ Silanna
→ Qualcomm
Licensed ZiBond
Feb 2012

'13
SRI International
Licensed
ZiBond/DBI
Aug 2013

NOVATI TECHNOLOGIES, INC.
Licensed ZiBond/DBI
Jan 2013

'15
SONY
Licensed DBI
Mar 2015

TESSERA
Acquisition
August 2015

'16

'17
OmniVision
Licensed
Feb 2017

UMC
Licensed ZiBond
& DBI Aug 2018

SMIC
Licensed DBI
Mar 2017

TELEDYNE DALSA
Everywhereyoulook™
Licensed DBI
Dec 2016

Fraunhofer
Licensed ZiBond/DBI
Sept 2016

Significantly Improved Thermal Management

Courtesy of Javi DeLa Cruz, Xperi

Wide Range of 2.5/3D-IC Applications Using Hybrid Bonding

TSV interposer

Silicon Interposer

CoWoS

Foveros

TSV

3D Stacked memory

TSV + Hybrid Bonding

3D SoC

With TSV

With Or Without TSV

Hybrid Bonding

Embedded in substrate

SHINKO

Unimicron

i-THOP

FC-EIC

EMIB

Without TSV

With substrate

RDL interposer

FOCoS

SWIFT

Without substrate

InFO

SLIT

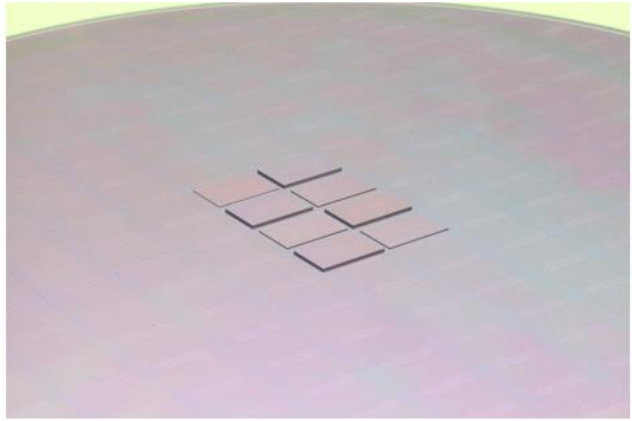
TGV

FUJITSU G-ALCS

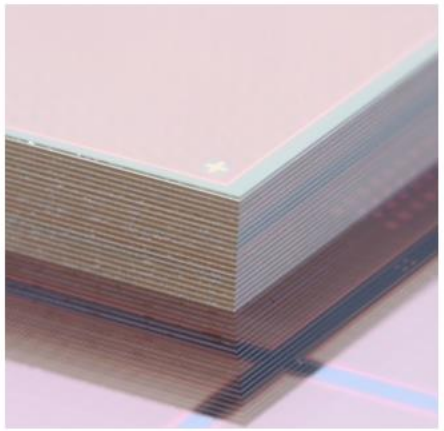
DBI® Die-to-Wafer Readiness

- **Some devices do not lend themselves well to wafer-to-wafer bonding**
- **Throughput 10x faster than TCB**
- **Only viable way to achieve 16-high HBM3 stacks with height restriction**
- **Production ready process available for tech-transfer**

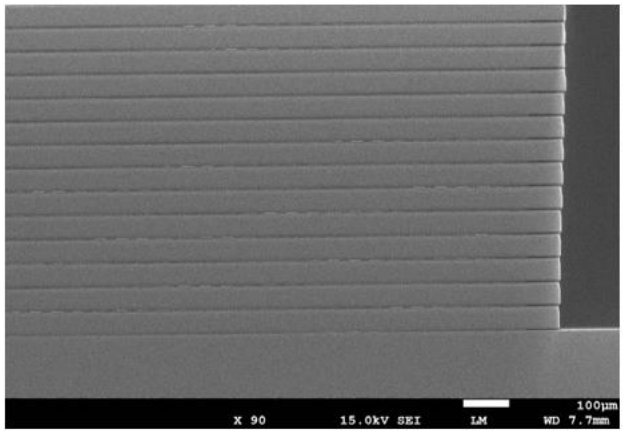
2-die, 3-die and 4-die
Stacks on host wafer



20-die stack
on host wafer



Cross-section of
20-die stack



XPERI

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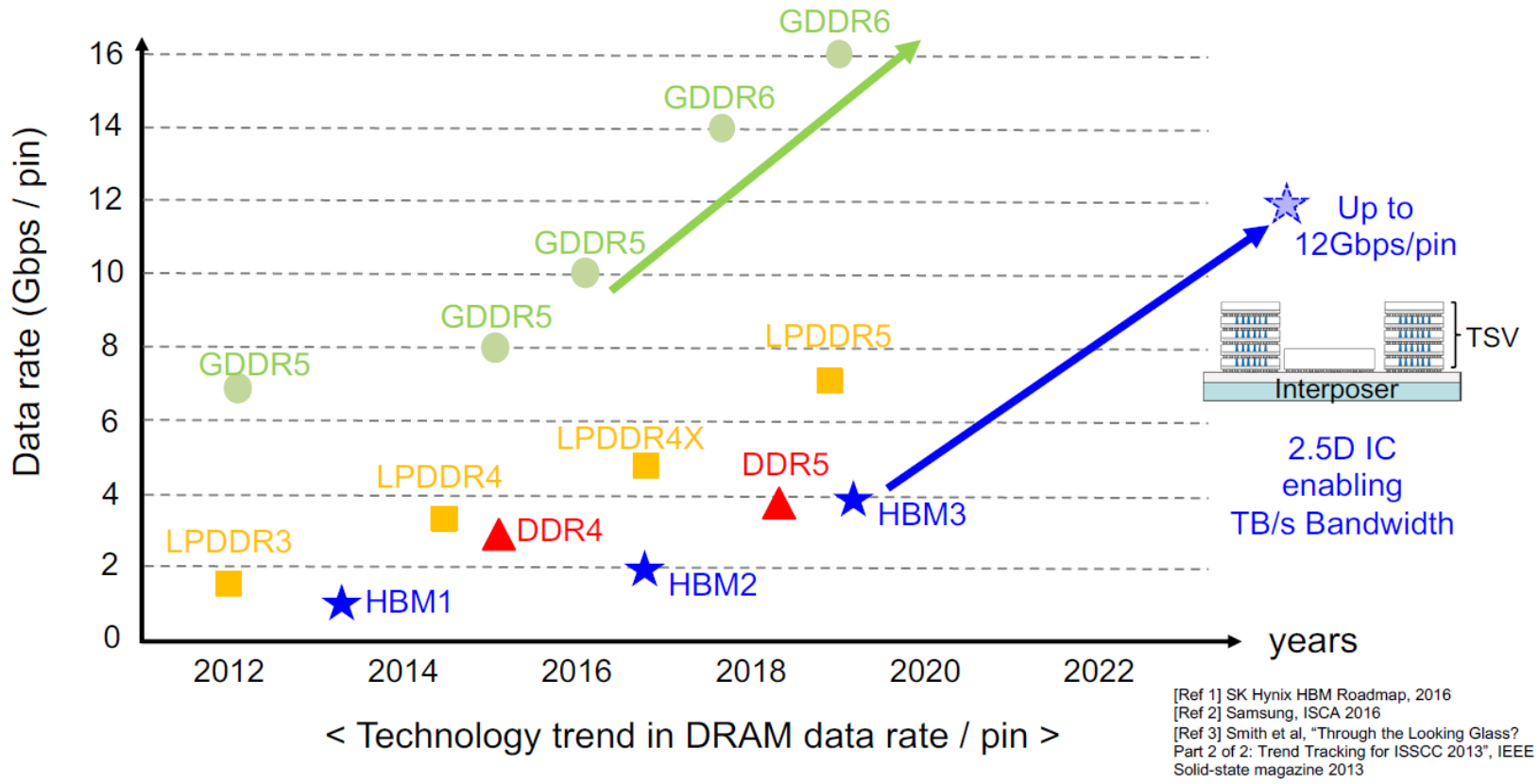
Data Rate Trends in Gbps per Pin



[Ref 1] SK Hynix HBM Roadmap, 2016
[Ref 2] Samsung, ISCA 2016
[Ref 3] Smith et al, "Through the Looking Glass? Part 2 of 2: Trend Tracking for ISSCC 2013", IEEE Solid-state magazine 2013

- Data rate of high-speed channel in DRAM is continuously increasing for higher bandwidth
- Maintaining signal integrity in the high-speed channel is crucial for higher data bandwidth

Source: Youngwoo Kim, Post-Doc at KAIST's Terabyte Labs. Presented at DesignCon 2019

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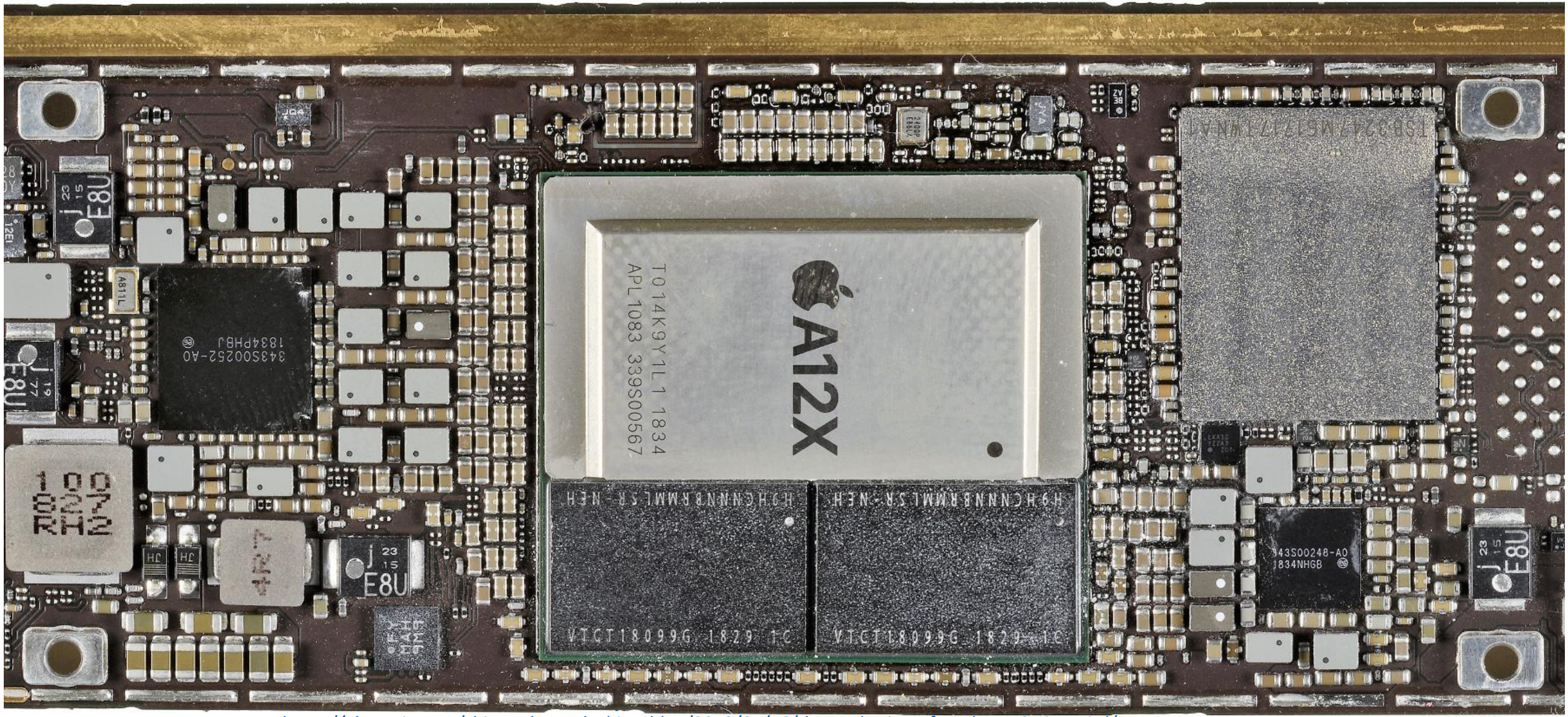
Apple's iPAD Pro with A12X Applications Processor

Passives, Passives, Passives and a few ICs



https://electroiq.com/chipworks_real_chips_blog/2019/01/16/the-packaging-of-apples-a12x-is-weird/#

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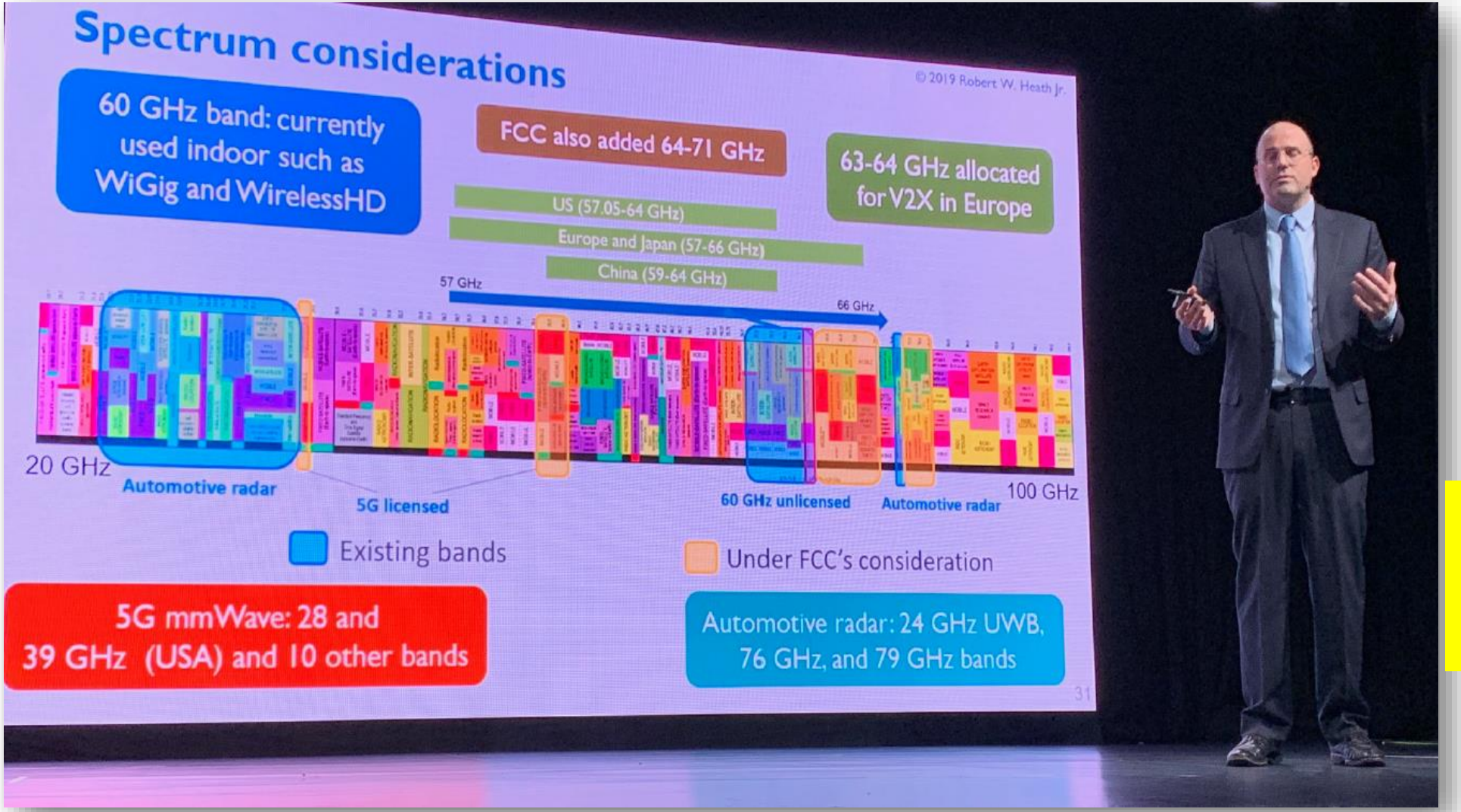
5G, Lidar,… Need High Frequency IC Packaging Materials



INSERTION LOSS diminishes signals and heats up IC

UC Austin's Professor Heath highlighting the high frequencies needed for 5G technology. DesignCon 2019

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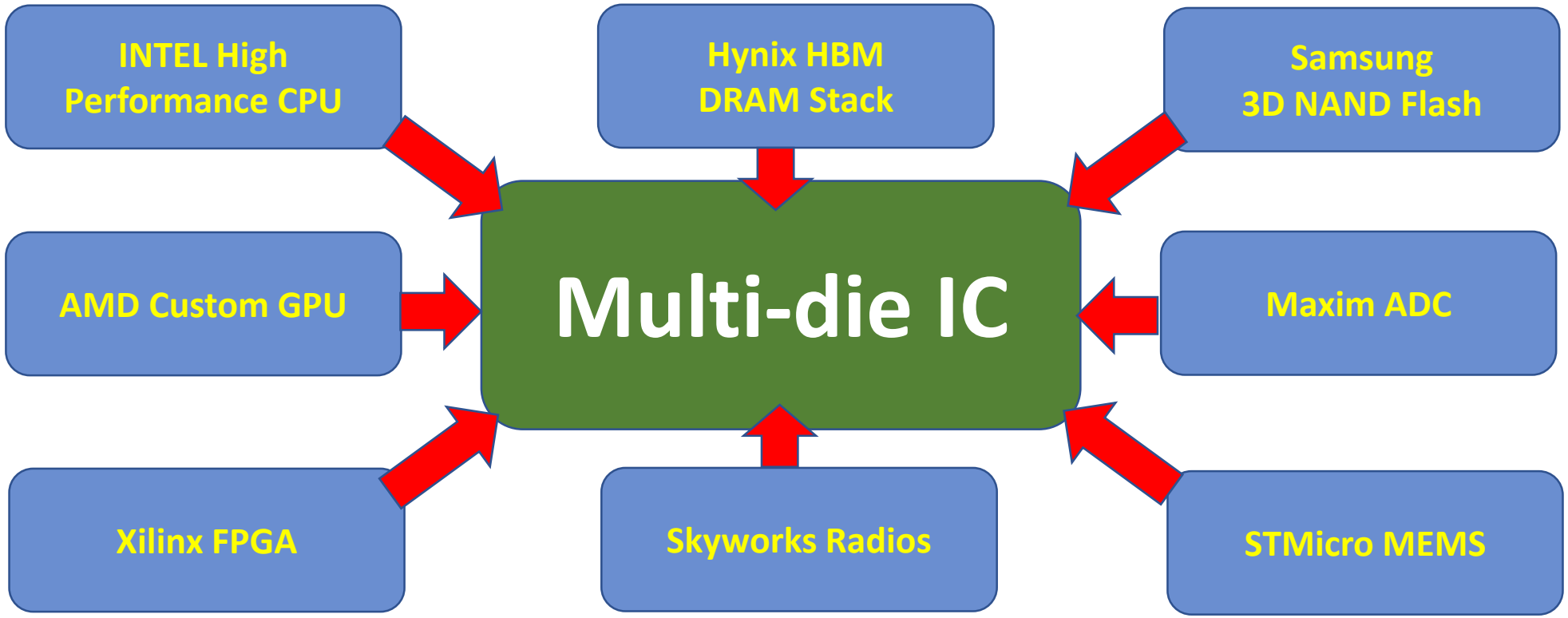
Heterogeneous Integration of CHIPLETs ("LEGO Blocks")



AND: Resistors, Capacitors, Inductors,
Image/ Temp / Pressure / Vibration Sensors,
Batteries, Energy Harvesters, …

Assembly & Test Houses have an inherent advantage (vs Fabs) when a mix of dies from multiple foundries is needed!

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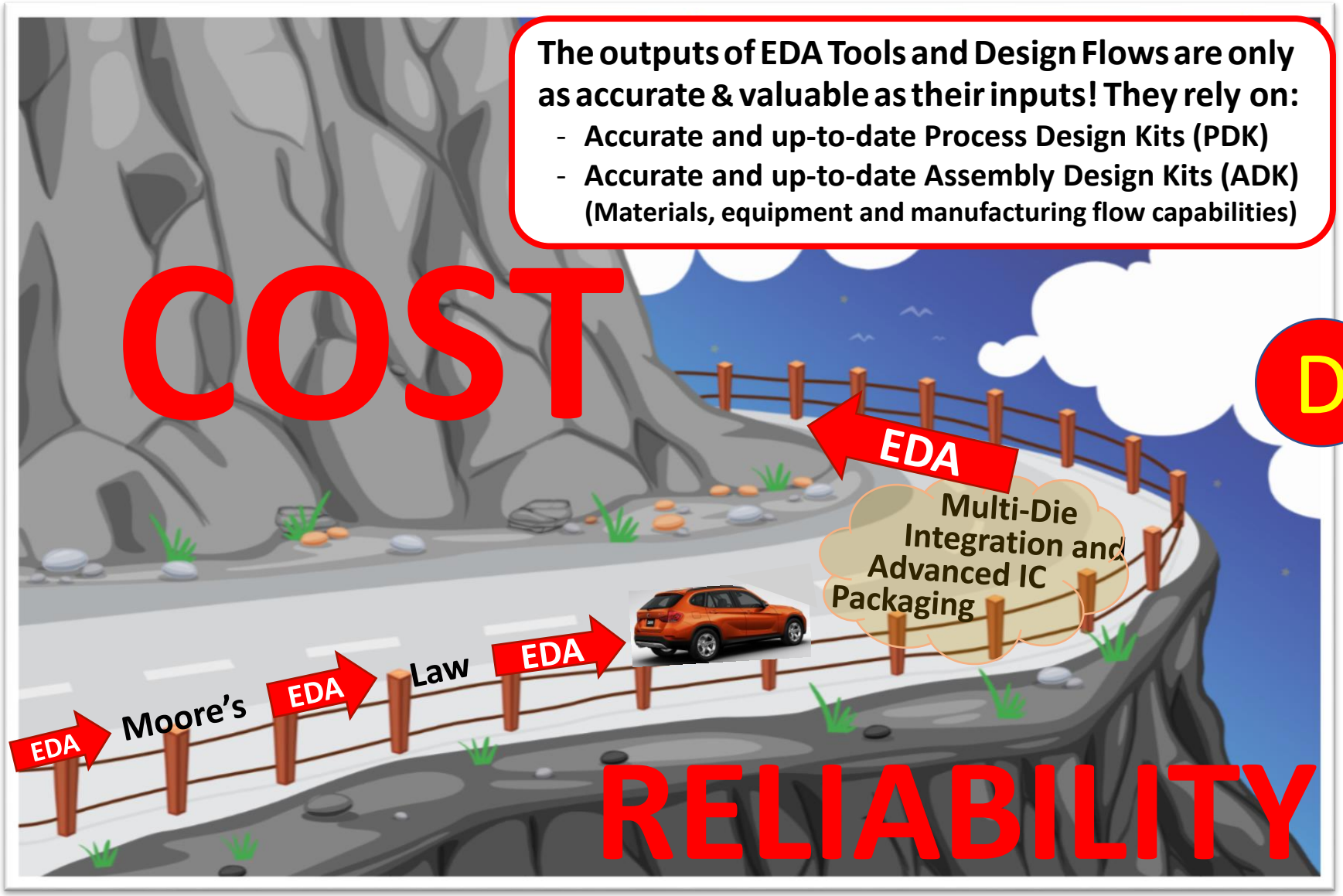
Importance of EDA Tools, Design Flows, PDKs & ADKs

- EDA Tools & Flows and
- Encrypted PDKs & ADKs enable – versus 2D SoCs:

✓ Higher Design Productivity
✓ Tighter Design Margins
✓ Better Testability
✓ First Time Success
✓ Lower Development Cost
✓ Shorter Time to Market
✓ Better Reliability
✓ Faster Production Ramps
✓ Higher Production Yields
✓ Lower Unit Cost
✓ Higher Profits
✓ Easier IP & Design Reuse



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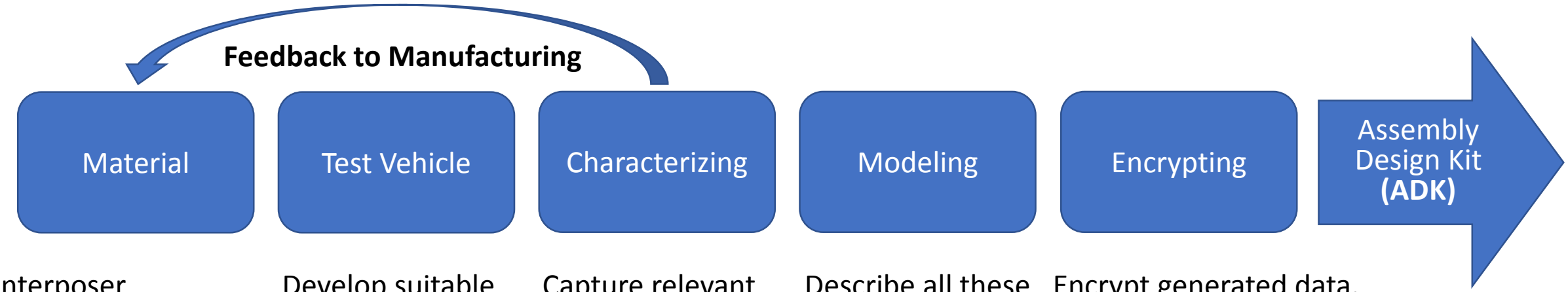
Characterization of IC Packaging Materials for ADK*



Interposer
RDL, Vias, Power Planes
Underfill
Bond wires
Micro balls, C4 balls
Copper studs
Pkg Substrate
RDL, Vias, Power Planes
Molding Compound
UBM
Heatsink, PCB, etc…

Develop suitable test structure(s) & methodologies to capture all relevant material characteristics for rigid and flex

Capture relevant characteristics, e.g.
- Operating temp range
- Aging mechanisms
- Thermal conductivity
- Expansion coefficient
- Young's modulus
- Poisson ratio
- Dielectric loss
- Behavior if stretched, compressed, bent, twisted, warped,…
- Chemical resistivity

Describe all these materials behavior with equations, graphs, tables, … Get accurate and up-to-date inputs for EDA tools

Encrypt generated data, so that only authorized EDA tools can interpret suppliers' proprietary information. Convey all material capabilities and constraints to the IC & package designers for planning, design and exhaustive verification.

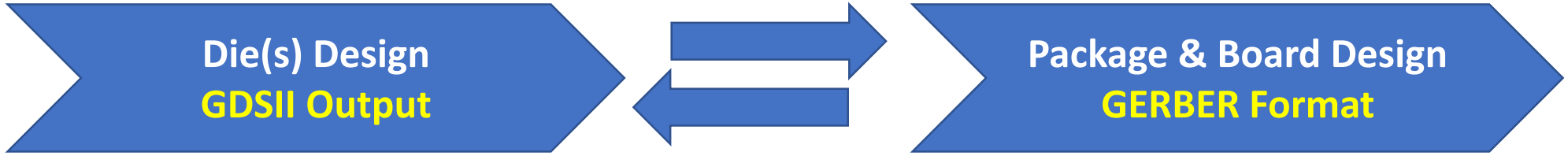
ACCURATE materials characterization and modeling ➔ ACCURATE simulation results

*ADK = Package **Assembly Design Kit**

Multi-die IC Reference Design Flow

EDA and Packaging experts develop jointly – with customer(s) inputs:

- **Die – Package – Board bi-directional Reference Design Flow:**
  - Recommends tools for design planning, implementation and verification steps for multi-die ICs
  - Describes hand-of criteria from designers to manufacturing partner's assembly and test team
  - Outlines logistics and inputs needed for wafer-probe, interim and final test
  - Suggests how and who to cooperate with in EDA as well as at the assembly and test partner(s)
  - Lists additional info sources: Web-pointers, industry standards, white papers, books, …
  - Describes best practices for data exchange between die(s) and package; encourages CO-design

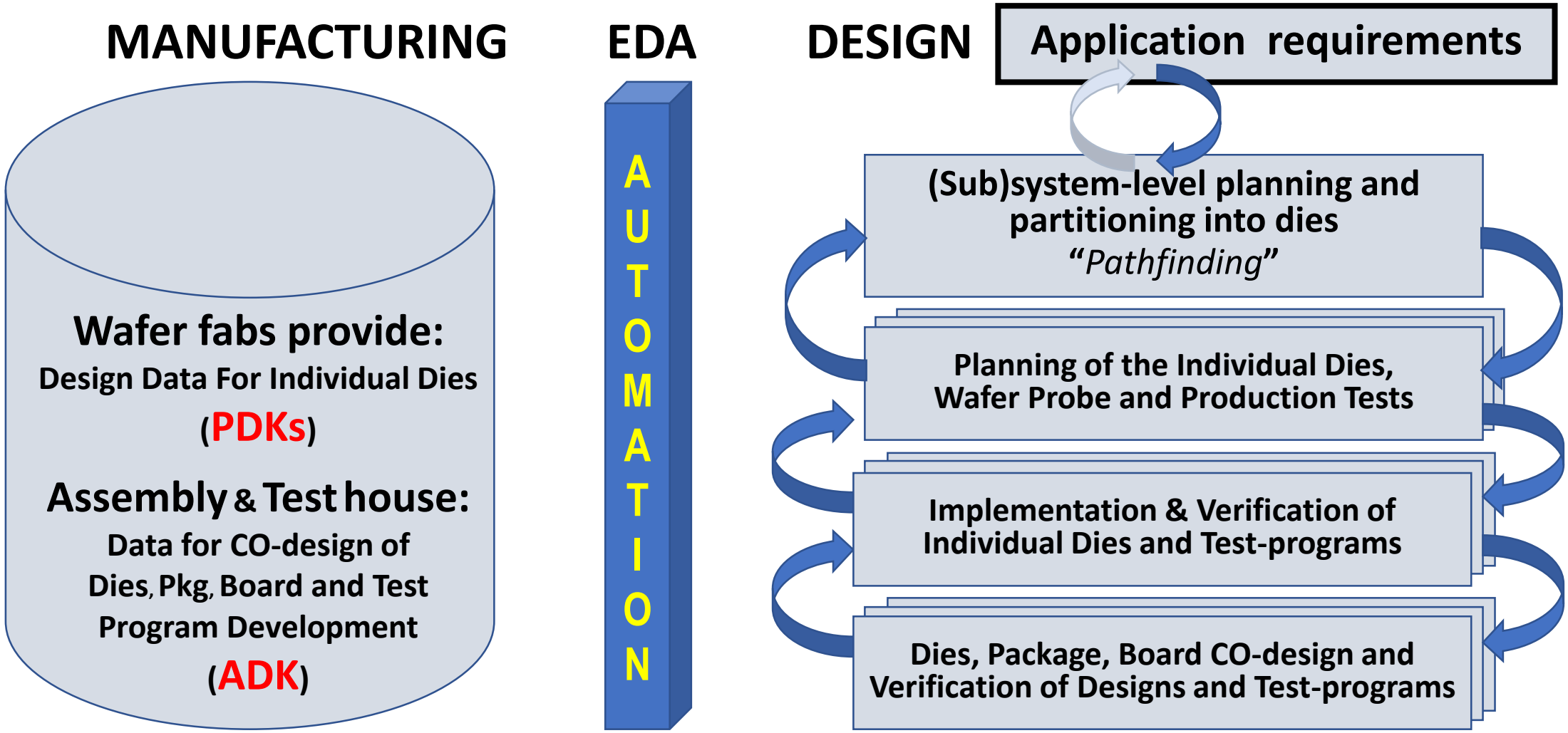


Workstations and PCs with mostly LINUX-based Design Tools

PCs with Windows-based Design Tools

Maturity of design & manufacturing steps influences when to automate which design step(s) !

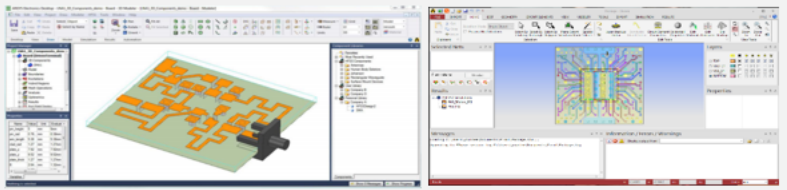
Multi-die IC EcoSystem Cooperation (1)



No more trial & error prototyping loops → → → Iterations are moving to the design space!

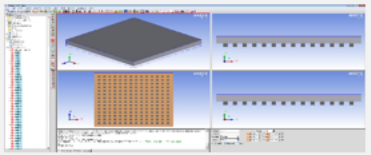
ANSYS Chip Package System Eco System for Power/Thermal/Signal Integrity : Reproducing Silicon/System Validation Environment

HFSS 3DLayout **SIwave**



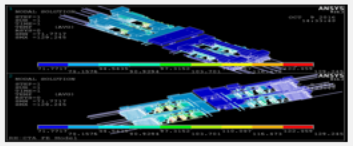
System Design Parasitic Extraction

Icepak



Chip & Package Aware HTC Generation

ANSYS Mechanical

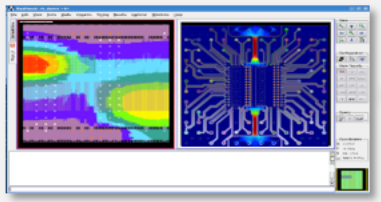


Interconnect Joule Heating Generation

CPM CSM CTM

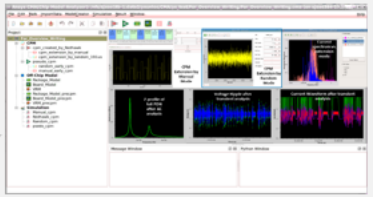
System Aware Chip Power Integrity | **Chip Aware System Power Integrity** | **Chip & System Level Signal Integrity** | **CPS Thermal Aware Reliability Analysis**

RedHawk-CPA



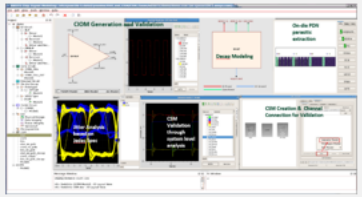
Chip&PKG Co-analysis & Visualization

ANSYS CMA



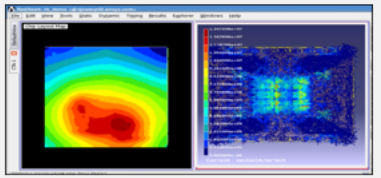
Full PDN CPM Generation & Simulation

ANSYS CSM



Full Chip IO Model Generation & Simulation

RedHawk-CTA (Fasttherm for Self-Heating)

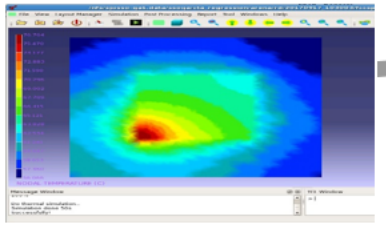


. System & chip aware package thermal analysis
. CPS thermal aware power EM
. CPS thermal aware self-heating with wire & device temperature

For Early Stage CPM

PowerArtist

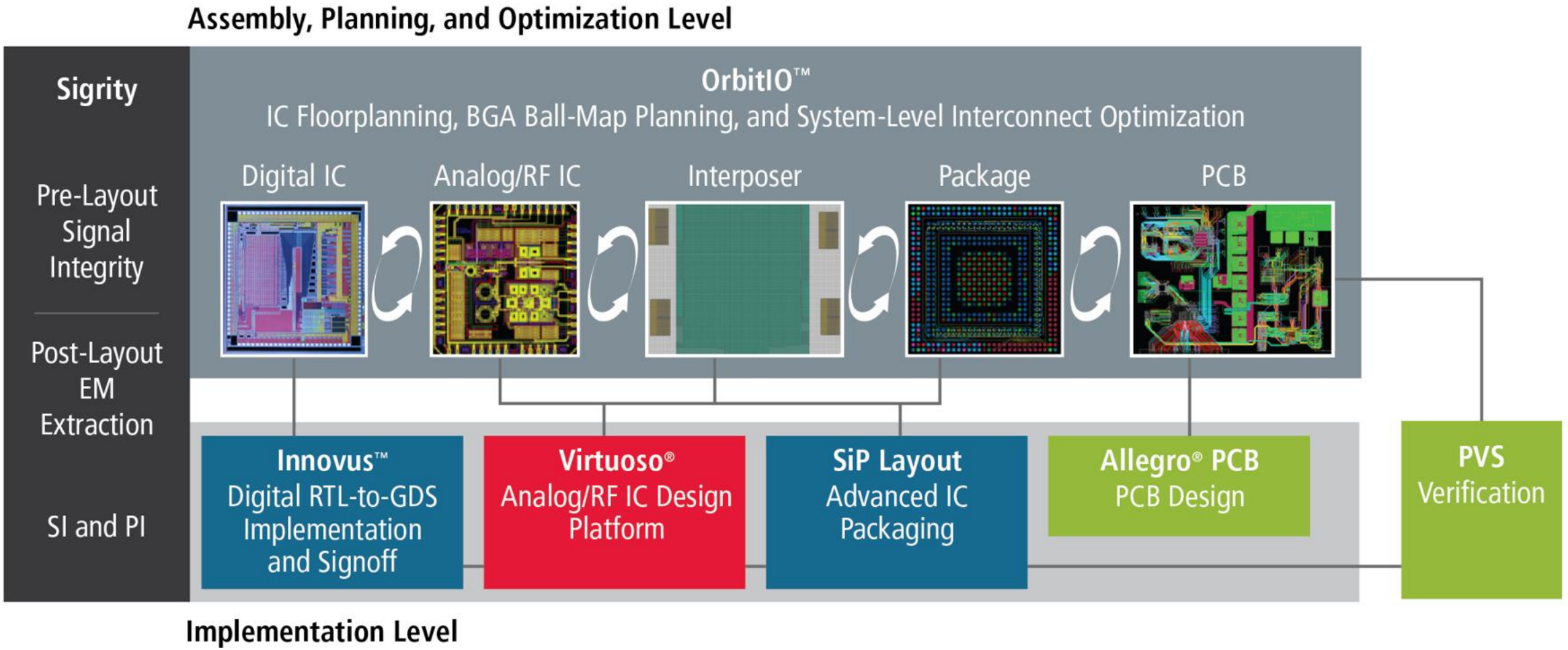
RTL Power Estimation & Optimization



Package Thermal Profile Generation

Standalone CTA

IC/Interposer/Package/PCB Cross-Domain Solution System Planning

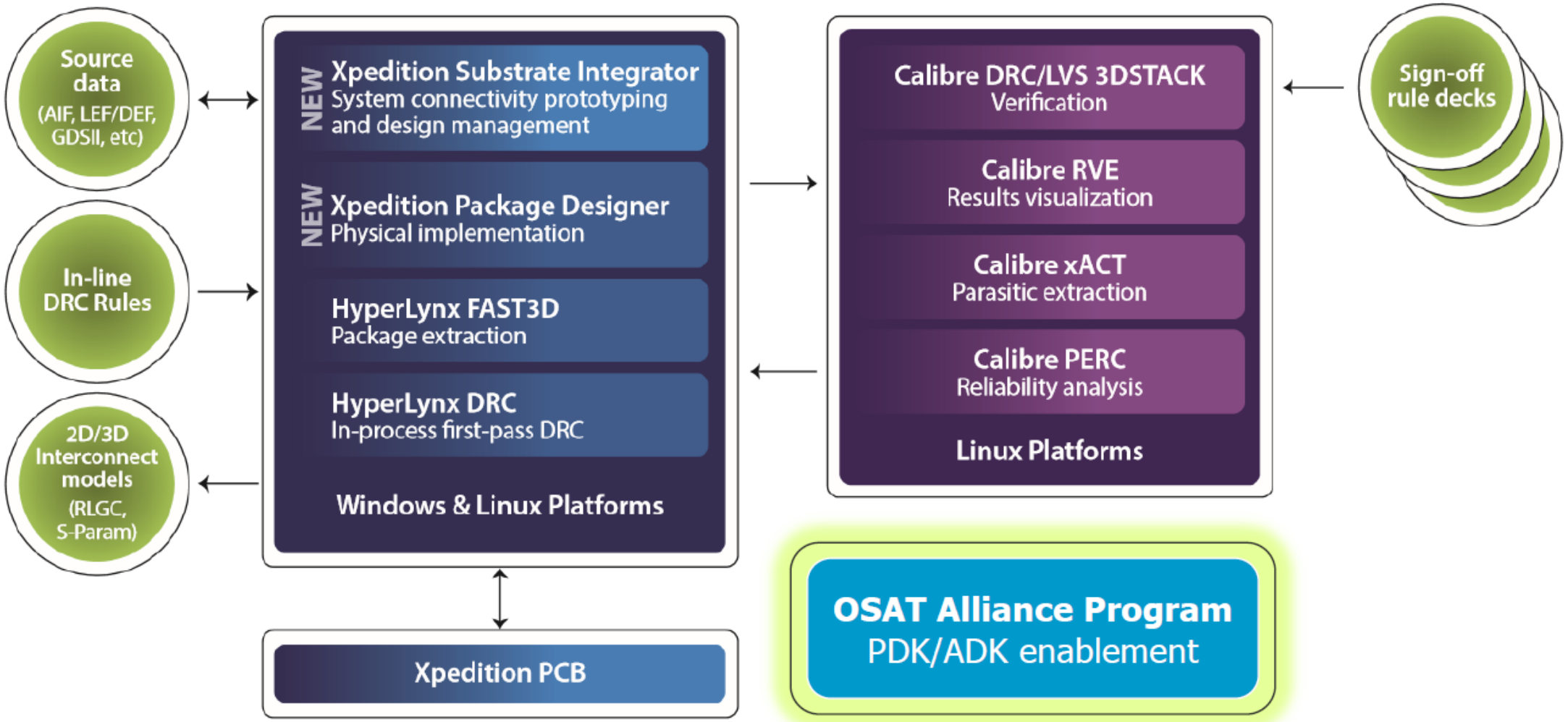


Courtesy of Bill Acito and John Park, Cadence Design Systems

https://www.3dincites.com/2018/11/eda-design-tools-flows-targeting-wlp-featured-at-iwlpc-2018/

cadence®

Mentor current design flow for Advanced Packaging

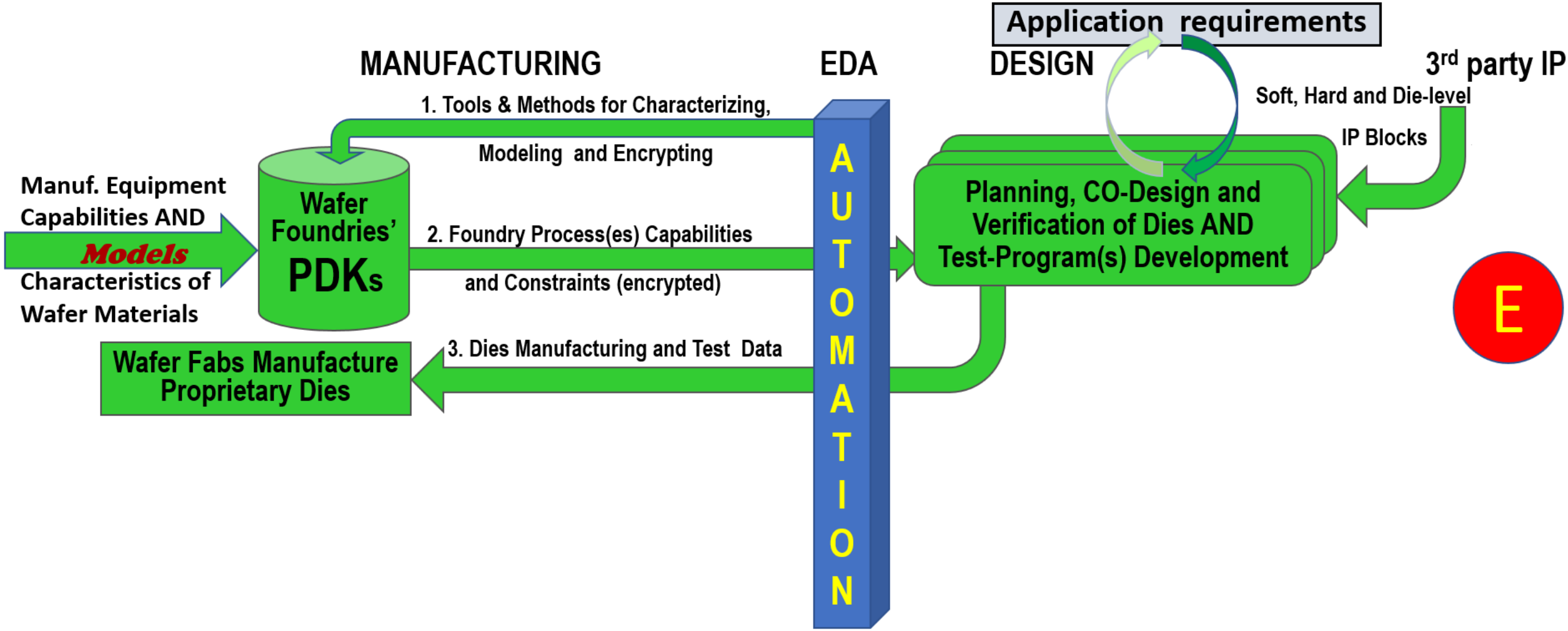


Courtesy of Keith Felton from Mentor, A Siemens Business

https://www.3dincites.com/2018/11/eda-design-tools-flows-targeting-wlp-featured-at-iwlpc-2018/

eda2asic

Multi-die IC EcoSystem Cooperation (2)



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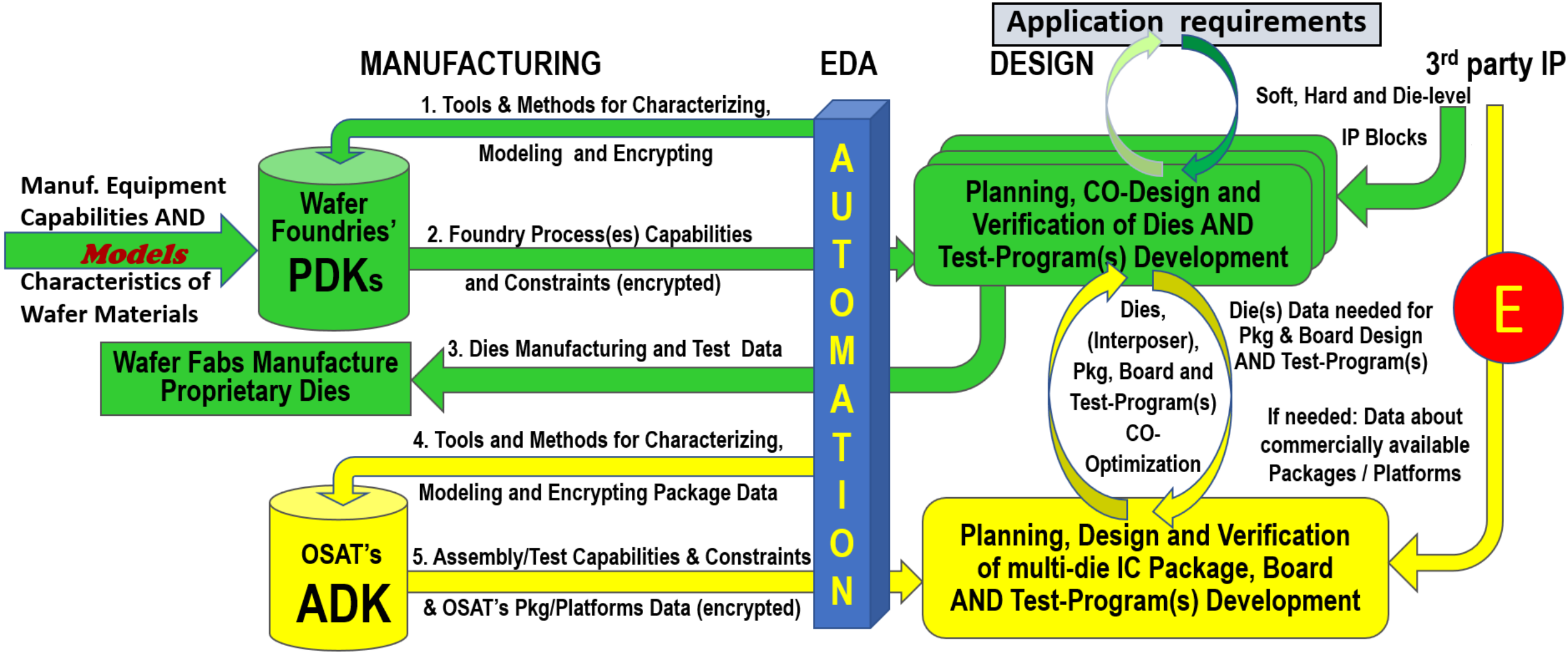
Multi-die IC EcoSystem Cooperation (2)



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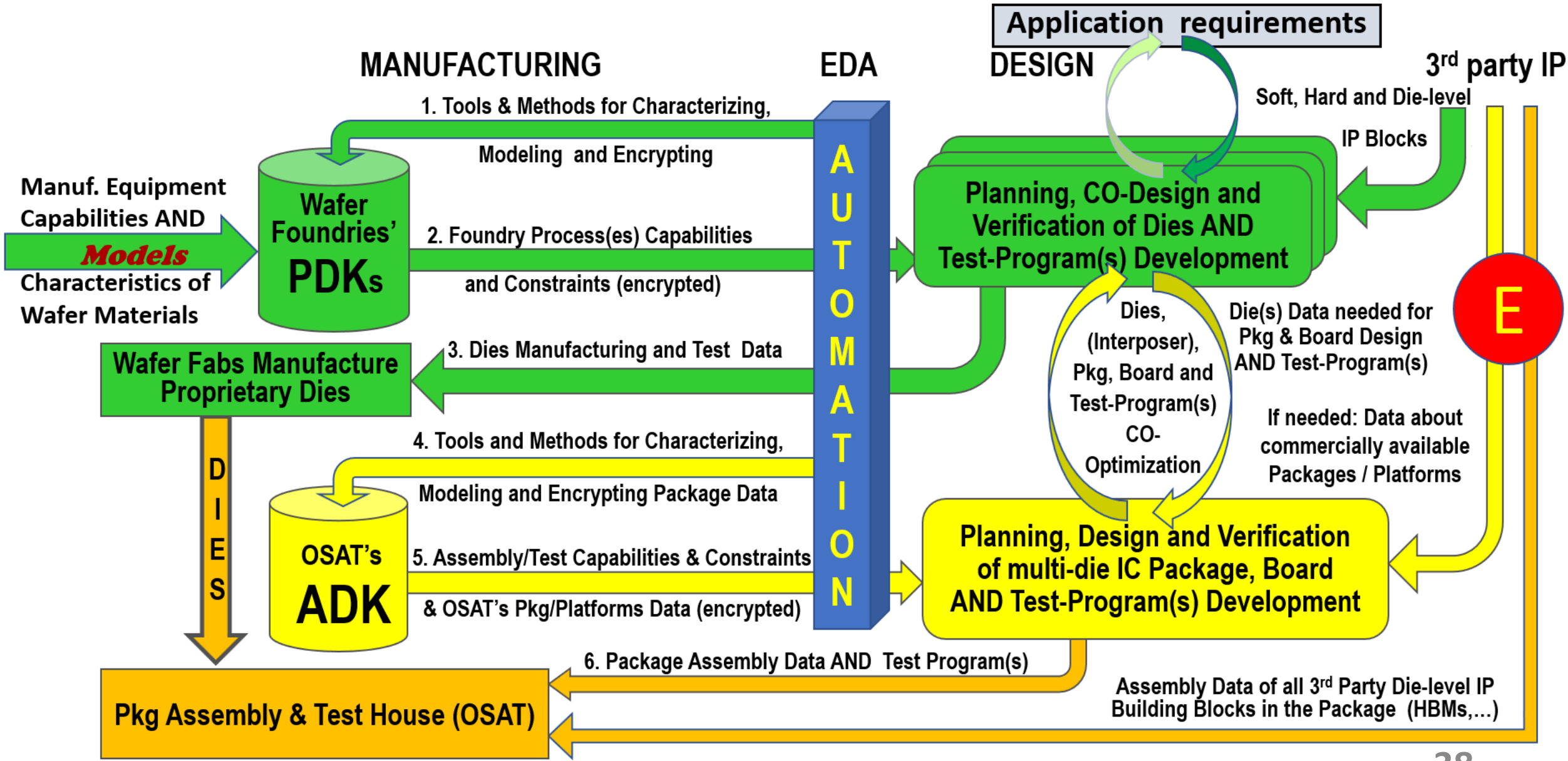
Multi-die IC EcoSystem Cooperation (2)



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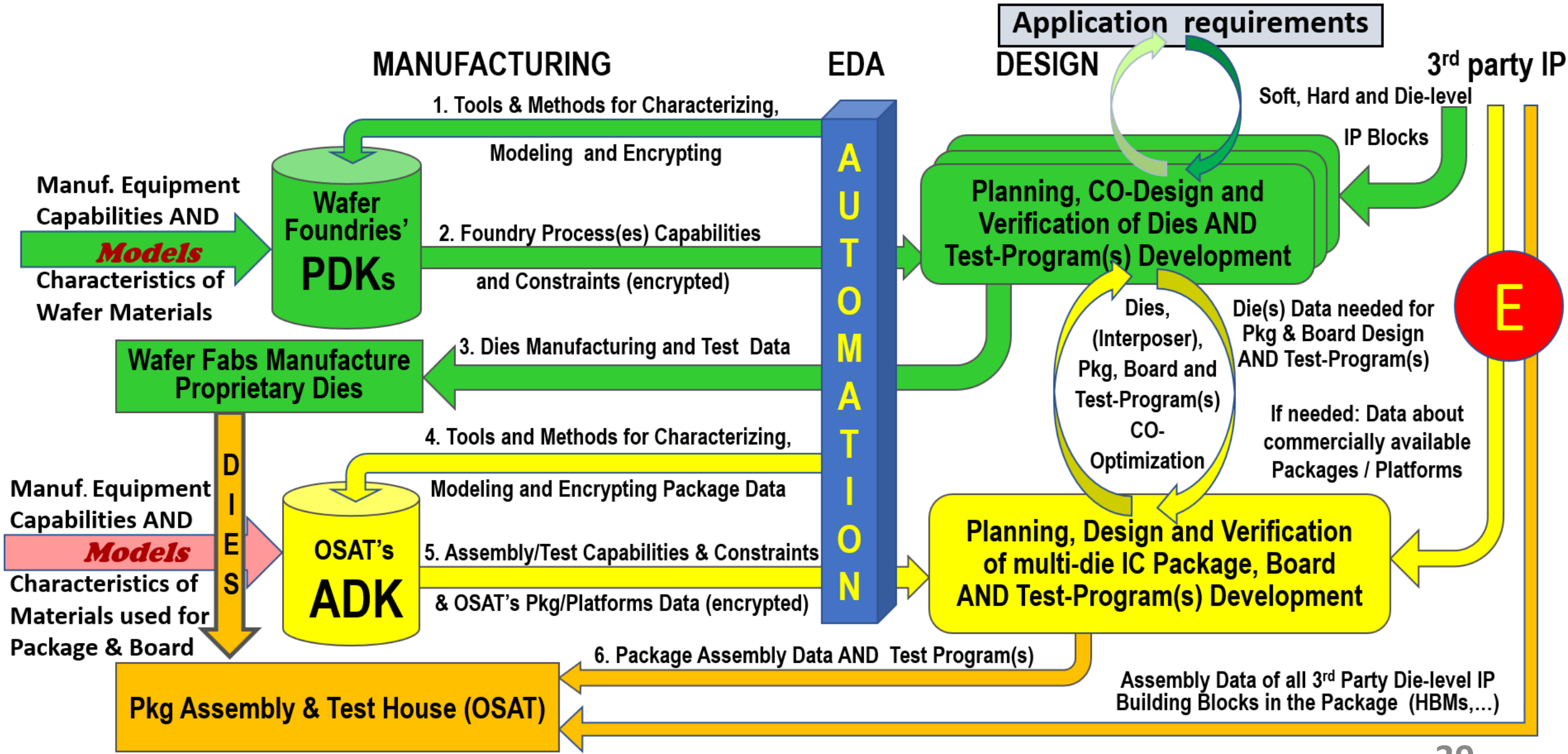
Multi-die IC EcoSystem Cooperation (2)



Multi-die IC Ecosystem Cooperation (3)

OSATs need to expand relationships with multiple

- CMOS, GaAs, SiGe, SiC, InP, GaN, SOI,… advanced and traditional wafer foundries
- CHIPLET sources to integrate die-level IP building blocks into multi-die ICs
- MEMS and Sensors suppliers as well as wafer-probe & test experts
- Interposer suppliers (silicon, organic, high-res Si) and low-cost litho for substrate
- Miniature passives (RLC) suppliers and Flexible Hybrid Electronics (FHE) partners
- EDA vendors to
  - model and encrypt your materials and equipment capabilities for ADK
  - develop reference design flows for your off-the-shelf platforms
  - improve IC test programs, self-test capability, built-in redundancy
  - utilize Software as a Service (SaaS) business model = rent EDA tools by the minute

eda2asic

Flexible Hybrid Electronics (FHE) and Medical Wearables

AGENDA

Introduction

Key Market Data and Requirements

Multi-die ICs and Advanced Packaging

EDA Tools, Flows and Libraries

Summary

Summary

- 50+ years of following Moore's Law has reached many economical and technical limits
- % growth and margins of smartphones are declining –> no longer innovation drivers
- Lower volume, customer specific solutions offer higher value and better profit margins
- Closer and structured supply chain cooperation is needed to meet customer requirements
- Designers, Wafer-fabs, Assembly & Test Houses (OSATs) need to become equal partners
- Multi-die ICs offer modularity, enable heterogeneous integration, lower NRE & risk
- Multi-die ICs increase Performance/Watt, but power density & thermal challenges increase
- Study system requirements; leverage your core competence; offer unique solutions

It's not the strongest of the species that survives, nor the most intelligent. It is the one that is most adaptable to change.
Charles Darwin

Automotive Ecosystem Evolution

The Semiconductor Ecosystem is likely to develop in a very similar way --- in the next few decades !

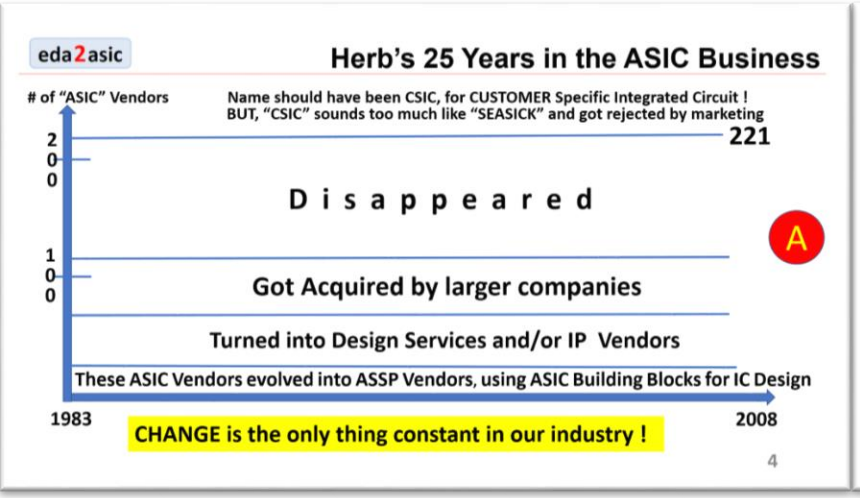
➔ **Leveraging modularity, flexibility, $ savings, time to profit...**

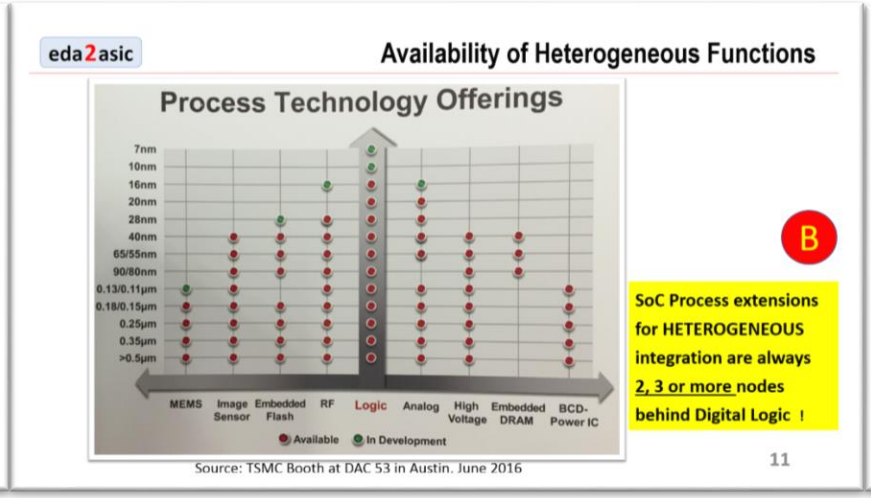
~1900: Ford designed and manufactured **every Model T component** and assembled all the pieces in house

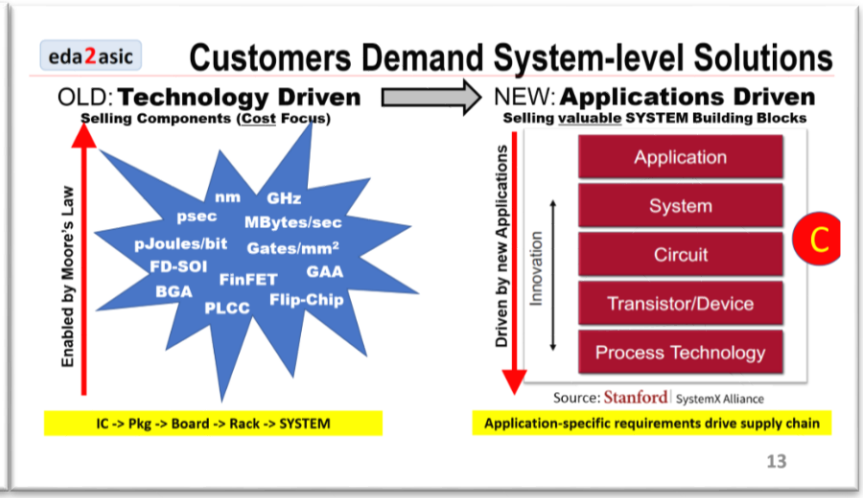
100 Years

~2000: Ford's eco-system partners design and mass-produce most of the Ford Focus components!

Ford designs and manufactures **ONLY core components** and assembles / markets / sells the final product.



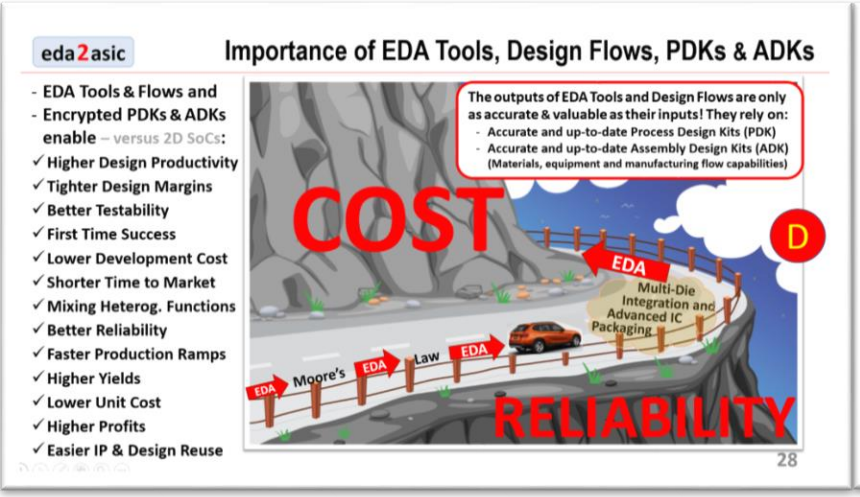


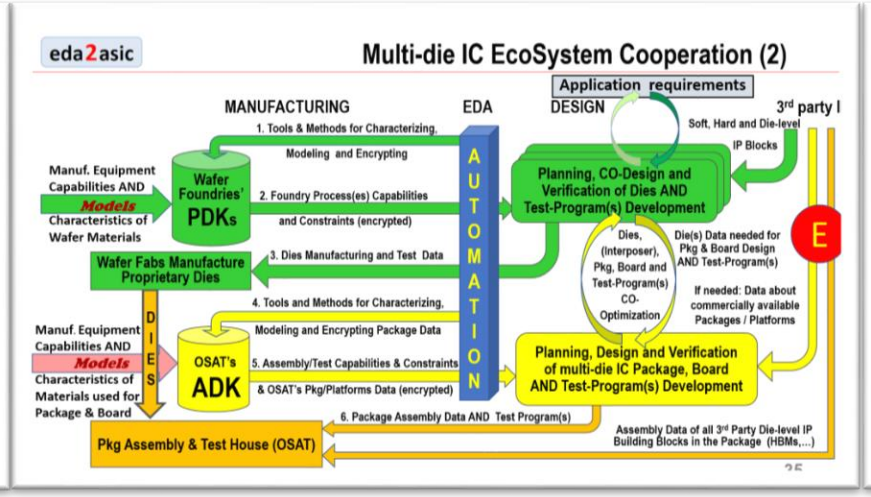


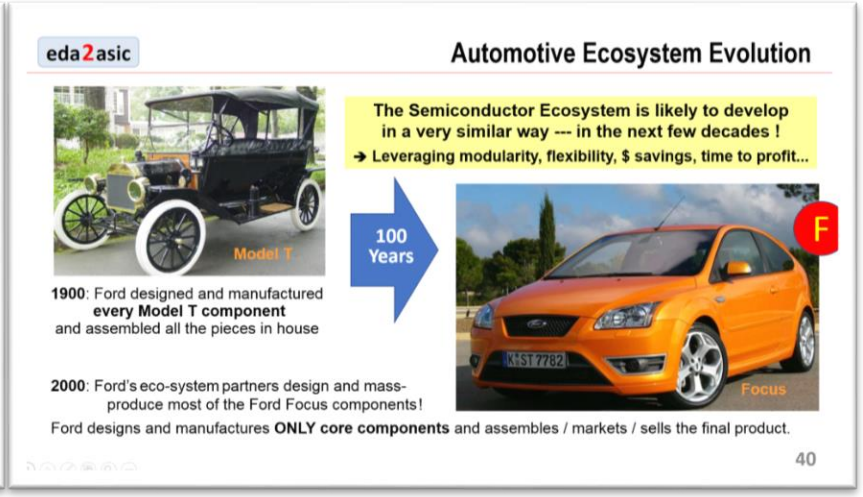
Technology AND Business Model = SUCCESS

HETEROGENEOUS Functions ➔ Multi-die IC

APPLICATIONs drive the requirements







Walk the fine line between COST & REL with EDA

It's COMPLICATED

Nobody spends an annual salary on a car any more

Thank You !

Please read…

BEFORE deciding your 2019 strategy, please click here and read:

- Brian Bailey's "Chip Dis-Integration" at
  https://semiengineering.com/chip-dis-integration/

- Ed Sperling's "Advanced Packaging Confusion" at
  https://semiengineering.com/advanced-packaging-confusion/

- Mark LaPedus' "Extending the IC Roadmap" with An Steegen's comments at
  https://semiengineering.com/extending-the-ic-roadmap/

- *Brian Bailey's "Design for Advanced Packaging" at*
  https://semiengineering.com/design-for-advanced-packaging/

- Herb Reiter's "The Great Divide Between Semiconductor Design and Manufacturing"
  https://www.3dincites.com/2016/08/the-great-divide-between-semiconductor-design-and-manufacturing/